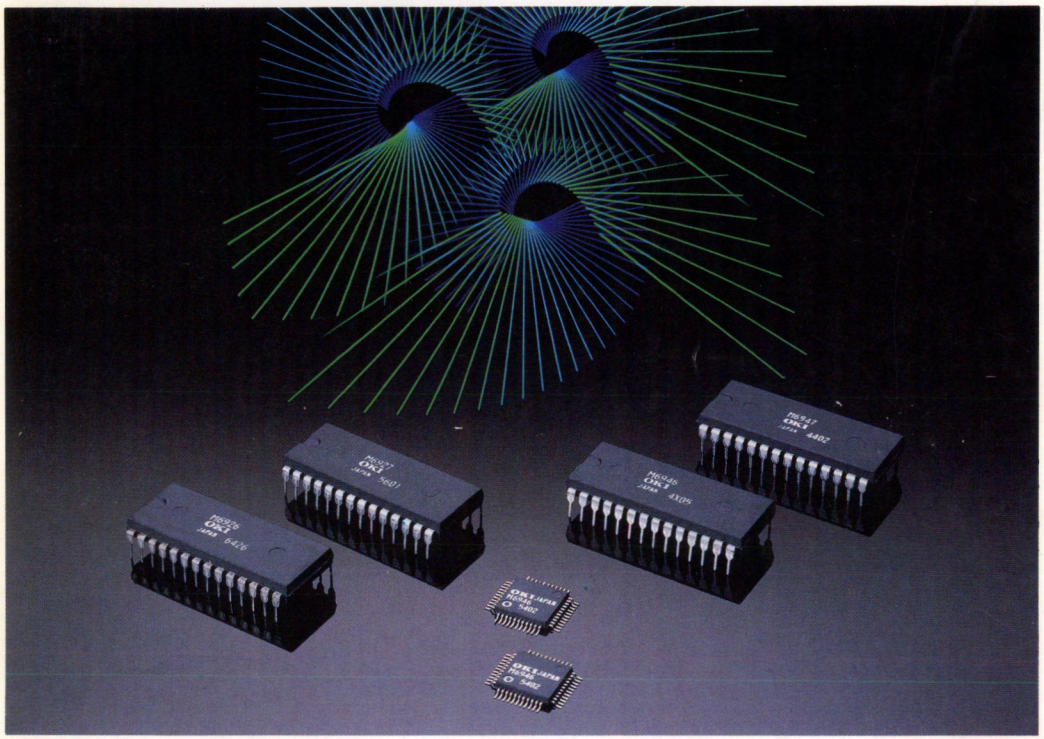
OKI

TELECOM LSI DATA BOOK



TELECOM LSI DATA BOOK 1987

CONTENTS

I
PRODUCT LINE-UP

PRODUCT LINE-UP

Type No.	Function	Features	Power		Package	Process	Applications
			Supply (V)	Consumption (mW)			
MSM6926	Single Chip FSK Modem, 300 bps Full Duplex	· CCITT V. 21 · Modulator, Demodulator, Filters and Carrier Detect	+5,+12	90	28 Pin DIP 44 Pin FLAT	CMOS	· POS terminal · CAT system · Handy data terminal · Modem phone · Tele-writing system · Vending machine · Tele-meter system · Coin telephone
MSM6946	Single Chip FSK Modem, 300 bps Full Duplex	· Bell 103 · Modulator, Demodulator, Filter and Carrier Detect	+5,+12	90	28 Pin DIP 44 Pin FLAT	CMOS	
MSM6927	Single Chip FSK Modem, 1200 bps Half Duplex	· CCITT V. 23 · Modulator, Demodulator, Filters and Carrier Detect	+5,+12	90	28 Pin DIP 44 Pin FLAT	CMOS	
MSM6947	Single Chip FSK Modem, 1200 bps Half Duplex	· Bell 202 · Modulator, Demodulator, Filters and Carrier Detect	+5,+12	90	28 Pin DIP 44 Pin FLAT	CMOS	
MSM6948	Single Chip MSK Modem, 1200 bps	· Modulator, Demodulator, Filters and Digital P_{LL} · Carrier Frequency: 1500±300 Hz	+5	15	18 Pin DIP 24 Pin FLAT	CMOS	· Wireless communication · Cordless telephone · Pager
CHIP SET	1200 bps Full Duplex Modem	· Bell 212A · Hayes Compatible · Adaptive Equalizing Function CHIP SET: MSM6928-06, MSM6950, MSM61057, MSM80C31, MSM27C64, MSM81C55A	±5.0	600	–	CMOS	· Stand alone modem · Modem card
CHIP SET	2400 bps Full Duplex Modem	· CCITT V. 22 bis Bell 212A · Adaptive Equalizing Function CHIP SET: MSM6928-07, MSM6950, MSM61077, MSM80C51-98/99	±5.0	400	–	CMOS	· Stand alone modem · Modem card
MSM6928-06	DSP for OKI's 1200 bps FDX Modem Chip Set	· Demodulator · Carrier P_{LL}, Timing P_{LL} · Adaptive EQL · Carrier Detect	+5.0	150	42 Pin DIP 60 Pin FLAT	CMOS	OKI's 1200 bps FDX Modem Chip Set
MSM61057	Gate Array for OKI's 1200 bps FDX Modem Chip Set	· Asynchronous/Synchronous and Synchronous/Asynchronous Converters · P_{LL}	+5.0	50	40 Pin DIP 60 Pin FLAT	CMOS	
MSM6928-07	DSP for OKI's 2400 bps FDX Modem Chip Set	· Demodulator · Adaptive EQL	+5.0	150	42 Pin DIP 60 Pin FLAT	CMOS	OKI's 2400 bps FDX Modem Chip Set
MSM61077	Gate Array for OKI's 2400 bps FDX Modem Chip Set	· Asynchronous/Synchronous and Synchronous/Asynchronous connecters · P_{LL}	+5.0	50	60 Pin FLAT	CMOS	

I

I

Type No.	Function	Features	Power		Package	Process	Applications
			Supply (V)	Consumption (mW)			
MSM6950	Analog Front End for 1200 bps/2400 bps FDX Modem	· Analog Functions for CCITT V.22, V.22 bis and Bell 212A · 8-bit D/A and A/D Converter	±5.0	100	42 Pin DIP 56 Pin FLAT	CMOS	· V.22 modem · V.22 bis modem · Bell 212A modem
MSM6949	Analog Front End for 4800 bps/9600 bps HDX Modem	· Analog Functions for CCITT V.26, V.27 and V.29 · 8-bit D/A and A/D Converter · Band Limiting Filter, AGC	±5.0	140	64 Pin Mini DIP	CMOS	· V.26 modem · V.27 modem · V.29 modem
MSM6052	4-bit MCU with On-Chip DTMF Generator	· 2,048x14-bit ROM · 640x4-bit RAM · 3x4 Input Port · 3x4 Output Port · 1x4 Input/Output Port	+2.5~ +6.0	3.6 (3V) 20 (6V)	28 Pin DIP 40 Pin DIP 44 Pin FLAT DIE	CMOS	· Telephone · Answering machine · Security system · Modem phone · Feature phone
MSM6052-01 MSM6052-20	Tone/Pulse Repertory Dialer	· 500 Digit Memory (54 Numbers) · Last Number Redial: 32 Digit · Make/Break Ratio Selectable · Dial Pulse Ratio Selectable · Off-hook Memory Storing	+2.5~ +6.0	3.6 (3V) 20 (6V)	28 Pin DIP	CMOS	
MSM6052-05 MSM6052-10	Tone/Pulse Repertory Dialer	· 500 Digit Memory (54 Numbers) · Last Number Redial: 32 Digit · Make/Break Ratio Selectable · Dial Pulse Ratio Selectable · On-hook/Off-hook Memory Storing · 4-bit Parallel Data Input	+2.5~ +6.0	3.6 (3V) 20 (6V)	44 Pin FLAT 40 Pin DIP	CMOS	
MSM6052-11	Tone/Pulse Repertory Dialer	· 500 Digit Memory (54 Numbers) · Last Number Redial: 32 Digit · Make/Break Ratio Selectable · Dial Pulse Ratio Selectable · On-hook Memory Storing	+2.5~ +6.0	3.6 (3V) 20 (6V)	28 Pin DIP	CMOS	
MSM6052-25	Tone/Pulse Repertory Dialer	· 505 Digits Memory (52 Numbers) · Last Number Redial: 32 Digit · Make/Break Ratio Selectable · Dial Pulse Ratio Selectable · Off-hook Memory Storing	+2.5~ +6.0	3.6 (3V) 20 (6V)	28 Pin DIP	CMOS	

Type No.	Function	Features	Power		Package	Process	Applications
			Supply (V)	Consumption (mW)			
MSM5070	Tone/Pulse Dialer with Redial	· Last Number Redial: 31 Digits · Make/Break: 33/67	+3.5~ +6.0	55	18 Pin DIP	CMOS	· Telephone · Answering machine · Security system · Modem phone · Feature phone
MSM5071	Tone/Pulse Dialer with Redial	· Last Number Redial: 31 Digits · Make/Break: 40/60	+3.5~ +6.0	55	18 Pin DIP	CMOS	
MSM6224	Tone Dialer	· MK5087 Compatible	+2.5~ +8.5	25 (MAX)	16 Pin DIP	CMOS	
MSM6234	Tone Dialer	· MK5089 Compatible · Easy Interface with MCU	+2.5~ +8.5	25 (MAX)	16 Pin DIP	CMOS	
MSM6932 MSM6933	COMBO CODEC	· MSM6932: μ-Law · MSM6933: A-Law · Serial Data Rate: 64K bps~2048K bps	±5.0	65	16 Pin DIP	CMOS	· PABX · Key system · SLIC · PCM system · ADPCM system · Digital telephone · Voice recognition · Digital voice recorder
MSM6962 MSM6963 MSM6982 MSM6983	COMBO CODEC	· MSM6962, MSM6982: μ-Law · MSM6963, MSM6983: A-Law · Serial Data Rate: 512/1024/1536/1544 / 2048 K bps	±5.0	55	16 Pin DIP 28 Pin PLCC	CMOS	
MSM6996-H MSM6997-H	COMBO CODEC	· MSM6996H: A-Law · MSM6997H: μ-Law · Serial Data Rate: 64K bps~2048K bps · 600Ω Drive Capability	±5.0	65	16 Pin DIP	CMOS	
MSM6996-V MSM6997-V	COMBO CODEC	· MSM6996V: A-Law · MSM6997V: μ-Law · Serial Data Rate: 64k bps~2048k bps · 600Ω Drive and Analog Loop Test Capability	±5.0	65	16 Pin DIP	CMOS	
MSM6998 MSM6999	COMBO CODEC	· MSM6998: A-Law · MSM6999: μ-Law · Serial Data Rate: 64k bps ~ 2048k bps · 600Ω Push-pull Drive and Analog Loop Test Capability	±5.0	70	16 Pin DIP	CMOS	
MSM6814 MSM6815	COMBO CODEC with Time Slot Assignment	· MSM6814: μ-Law MSM6815: A-Law · Time Slot Assignment: 32 Time/Frame Maximum · Serial Data Rate: 512/1024/1536/1544/ 2048k bps	±5.0	70	22 Pin DIP 28 Pin PLCC	CMOS	
MSA4710	BSH LSI for SLIC	· Battery Feed, Supervision and Hybrid Function · Loop Current Capability: 20~80 mA · Longitudinal Balance: 53 dB	−48, ±5.0	120	28 Pin DIP	Bipolar	· PABX · SLIC
MSA4722-1	RINGING SWITCHES for SLIC	· Ringing, Line Test Function · Breakdown Voltage: 350V · ON Resistance: 6Ω · DC Current Capability: 250mA	±5.0	40	22 Pin DIP	Bipolar	

I

Type No.	Function	Features	Power		Package	Process	Applications
			Supply (V)	Consumption (mW)			
MSM6912	PCM Voice Channel Filter	· Transmit BPF: 0.3~3.4 kHz · Receive LPF: 0~3.4kHz	±5.0	50	16 Pin Ceramic DIP	CMOS	· PABX · Digital switching system · Multiplexer
MSM6913	8-bit Serial-parallel Converter	· 8-bit Serial-parallel/ Parallel-serial Conversion · Maximum Operating Frequency: 9 MHz	+5.0	250 (MAX)	24 Pin DIP	CMOS	
MSM6914	Highway Switch Matrix	· Matrix Size: 16-bit x 4-bit x 3-layers · Maximum Operating Frequency: 9 MHz	+5.0	650 (MAX)	120 Pin Ceramic PGA	CMOS	
MSM77C-20	Digital Signal Processor	· Instruction Cycle: 250 ns · Instruction ROM: 512 x 23-bit · Data ROM: 512 x 13-bit · Data RAM: 128 x 16-bit · Multiplexer: 16 x 16 = 31 bits	+5.0	120	28 Pin DIP 44 Pin PLCC	CMOS	· Modem · Voice synthesizer · Voice recognition
MSM6992	High Speed Floating Point Digital Signal Processor	· Data Form: Floating Point 16E6x16E6→16E6 Fixed Point 16 x 16→31 · Instruction Cycle: 100 ns/125 ns · ROM: Internal 1k x 32-bit External 64k x 32-bit · RAM: Internal 128 x 22-bit x2 External 64k x 22-bit · Data Word Length: 22 bit	+5.0	400	132 Pin PGA	CMOS	· Modem · Voice Recognition · Echo canceller · ADPCM
MSM6807 MSM6817	Baseband Filter for Cellular Mobile Phone	· Voice BPF, Pre-emphasis, De-emphasis and Smoothing Filter · MSM6807 : AMPS MSM6817 : TACS	+5.0	30	32 Pin FLAT	CMOS	· Wireless Communication · Cellular phone
MSM6808 MSM6818	Split Filter for Cellular Mobile Phone	· 10k bps/8k bps SPL Modem Timing Extractor · Filters for SAT and SPL modem · DTMF Tone Generator MSM6808 : AMPS MSM6818 : TACS	+5.0	40	44 Pin FLAT	CMOS	
MSM74017	Modem for Cellular Mobile Phone	· SPL Modem · Built in Data P_{LL} · Built in SAT P_{LL}	+5.0	20	56 Pin FLAT	CMOS	
MSM6960	P_{LL} Frequency Synthesizer	· 10 bits Programmable and 7 bits Swallow Counter · Selectable Reference Divider: 2^9 or 2^{10}	+5.0	20	24 Pin FLAT	CMOS	· Wireless Communication

Type No.	Function	Features	Power		Package	Process	Applications
			Supply (V)	Consumption (mW)			
MSM6252	FIFO Memory	· 64 Words x 4-bit First-in First-out Memory · F3341 (Fairchild) Compatible	+5.0	80	16 Pin DIP	CMOS	· Digital transmission system · LAN
MSM6920	Single Chip DTMF Decoder for PABX	· Receive Signal Level: –5~–32 dBm · Voice Hit Protection Filter	+5.0, +12.0	80	28 Pin DIP	CMOS	· PABX · Key system · Dial-in equipment
MSM6945	Single Chip DTMF Decoder for Terminal	· Receive Signal Level: –5~–48 dBm · Echo Control Circuit:	+5.0, +12.0	80	28 Pin DIP	CMOS	· Security system · Answering machine · Telecontrol system ·Dial-in equipment
MSM6980	32k-bit/sec ADPCM CODEC	· OKI's Original 24k bps and 32k bps ADPCM Algorithm · 9600 bps Data Transmission Capability · Selectable Coder and Decoder Functions	+5.0	70	42 Pin DIP	CMOS	· Digital transmission system

I

II
PACKAGING

PACKAGING

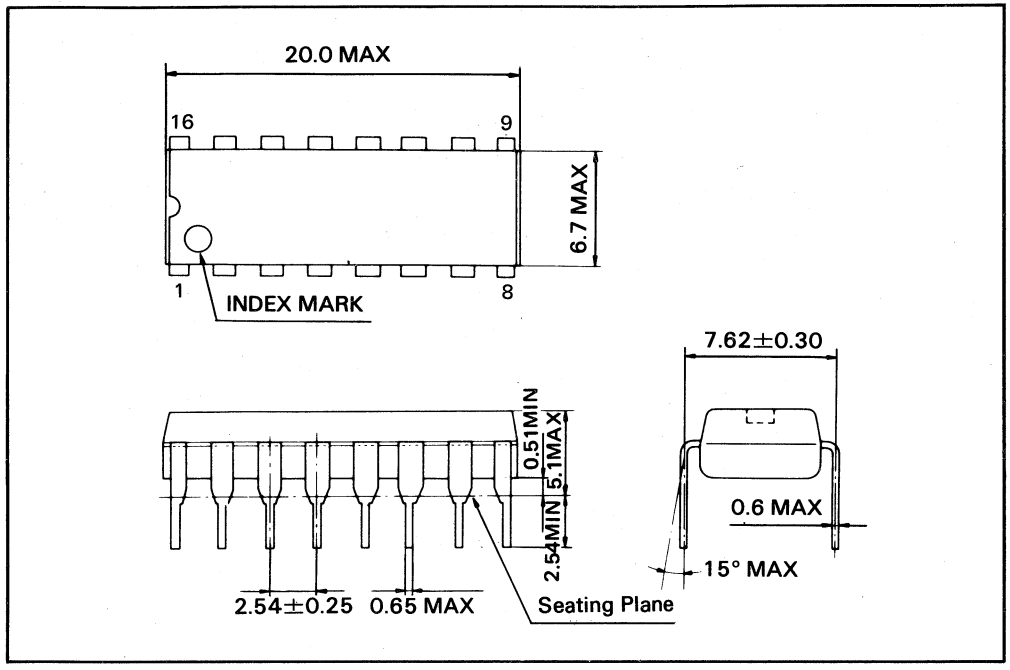
Product Name	No. of Pins	PACKAGE						
		RS	AS	AS	GS	JS	ES	SS
		PLASTIC DIP	CERAMIC DIP	PGA	PLASTIC FLAT	PLASTIC LCC	CERAMIC CC	MINI-SIZE PLASTIC DIP
MSM6926	28	○						
	44				○			
MSM6946	28	○						
	44				○			
MSM6927	28	○						
	44				○			
MSM6947	28	○						
	44				○			
MSM6948	18	○						
	24				○			
MSM6928-06	42	○						
	60				○			
MSM61057	40	○						
	60				○			
MSM6928-07	42	○						
	60				○			
MSM61077	60				○			
MSM6950	42	○						
	56				○			
MSM6949	64							○
MSM6052	28	○						
	40	○						
	44				○			
MSM6052-01	28	○						
MSM6052-05	44				○			
MSM6052-10	40	○						
MSM6052-11	28	○						
MSM6052-20	28	○						
MSM6052-25	28	○						
MSM5070	18	○						
MSM5071	18	○						
MSM6224	16	○						
MSM6234	16	○						
MSM6932	16	○	○					
MSM6933	16	○	○					
MSM6962	16	○	○					
MSM6963	16	○	○					
MSM6982	28					○	○	
MSM6983	28					○	○	
MSM6996H	16	○	○					
MSM6997H	16	○	○					
MSM6996V	16	○	○					
MSM6997V	16	○	○					
MSM6998	16	○	○					
MSM6999	16	○	○					

II

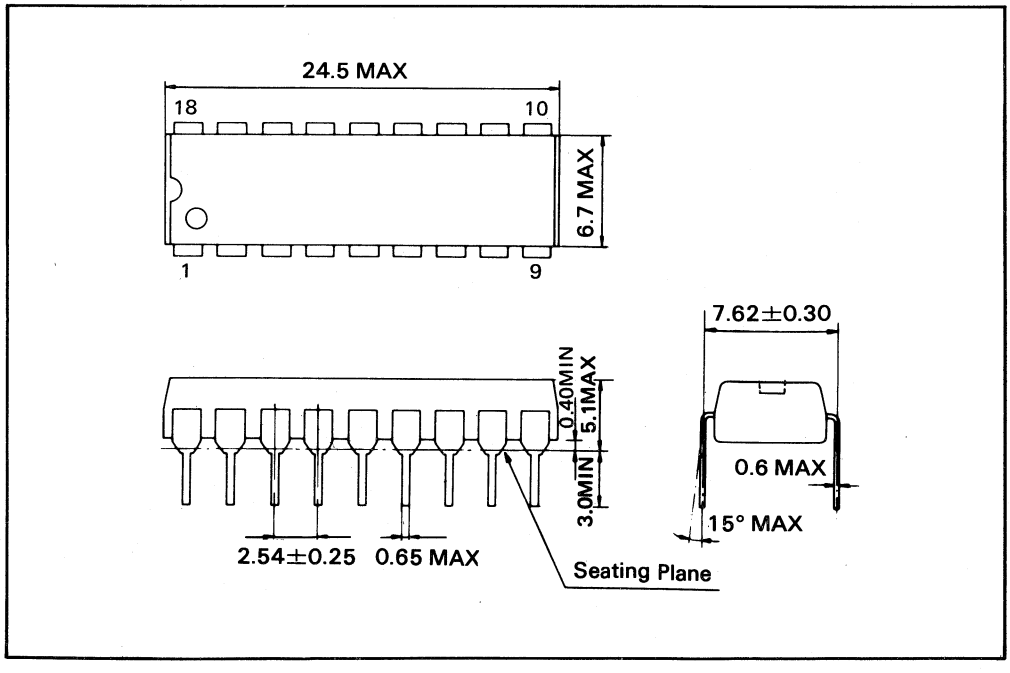
Product Name	No. of Pins	PACKAGE						
		RS PLASTIC DIP	AS CERAMIC DIP	AS PGA	GS PLASTIC FLAT	JS PLASTIC LCC	ES CERAMIC CC	SS MINI-SIZE PLASTIC DIP
MSM6814	22	○	○					
	28					○		
MSM6815	22	○	○					
	28					○		
MSA4710	28	○						
MSA4722-1	22	○						
MSM6912	16		○					
MSM6913	24	○						
MSM6914	120			○				
MSM77C20	28	○	○					
	44					○		
MSM6992	132			○				
MSM6807	32				○			
MSM6817	32				○			
MSM6808	44				○			
MSM6818	44				○			
MSM74017	56				○			
MSM6960	24				○			
MSM6252	16	○						
MSM6920	28	○						
MSM6945	28	○						
MSM6980-03	42	○						

II

• 16 PIN PLASTIC DIP

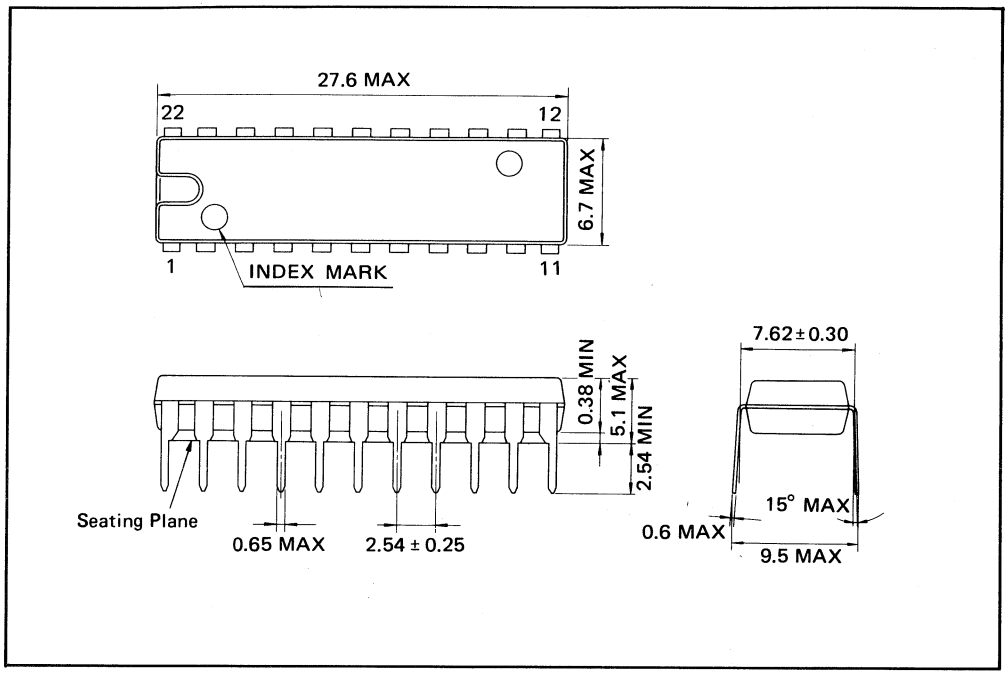


• 18 PIN PLASTIC DIP

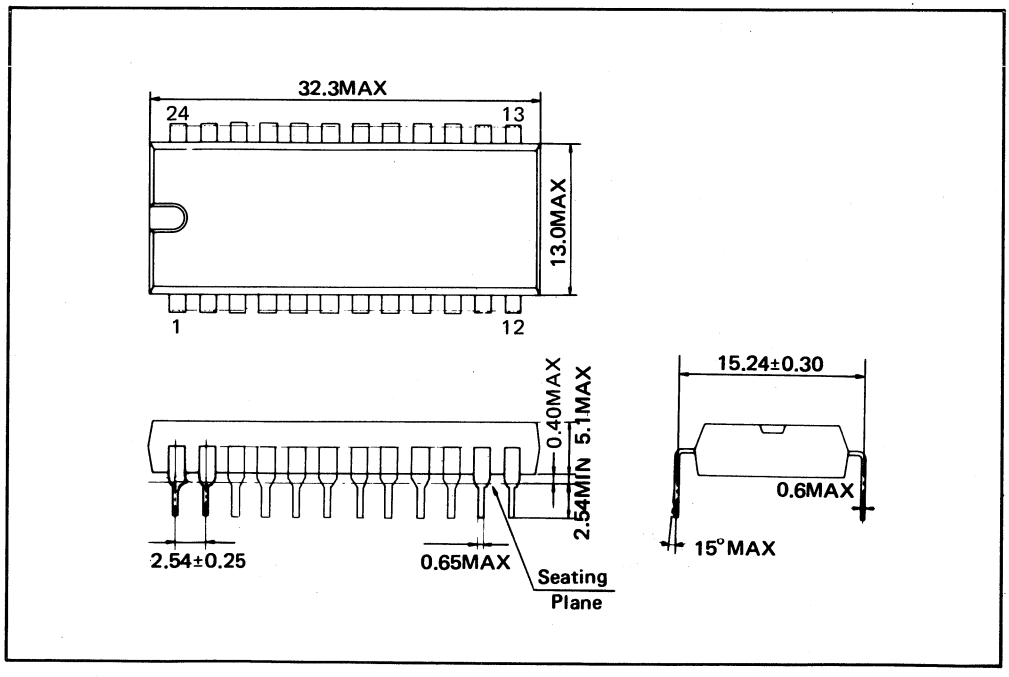


II

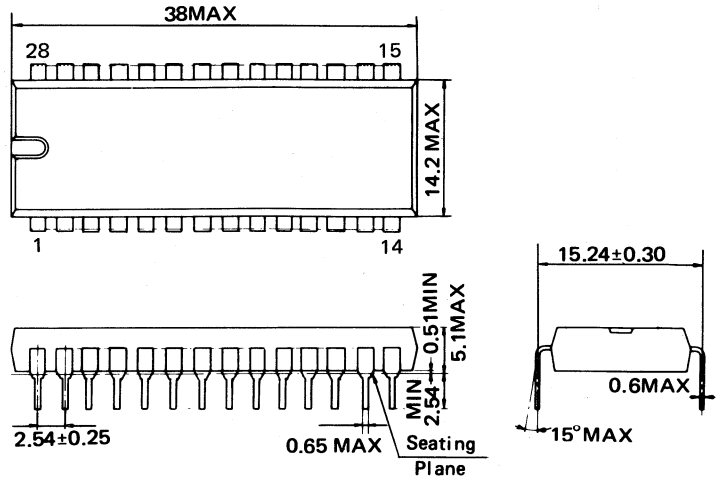
• 22 PIN PLASTIC



• 24 PIN PLASTIC DIP

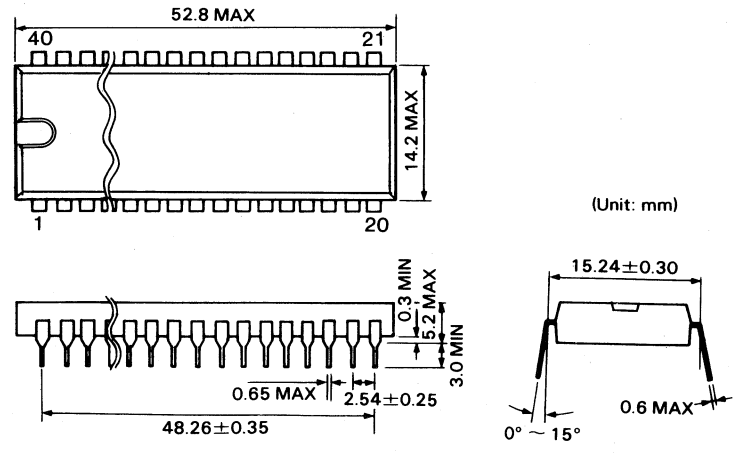


• 28 PIN PLASTIC DIP

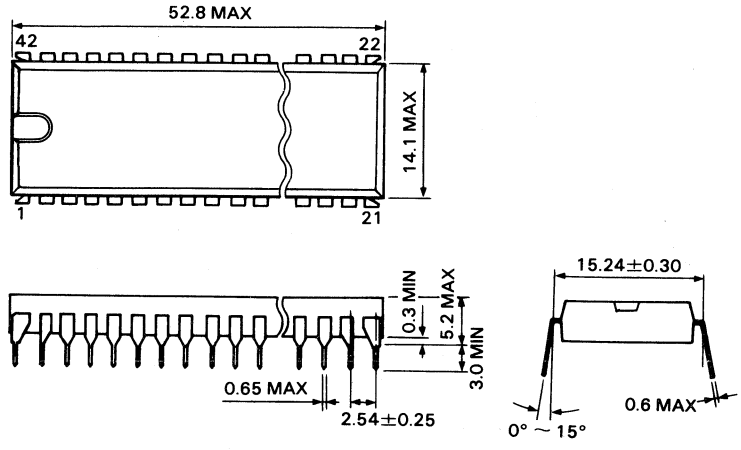


II

• 40 PIN PLASTIC DIP

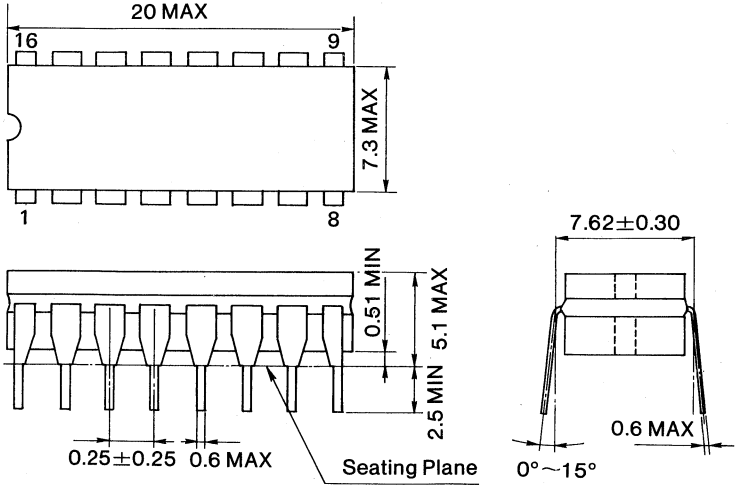


• 42 PIN PLASTIC DIP

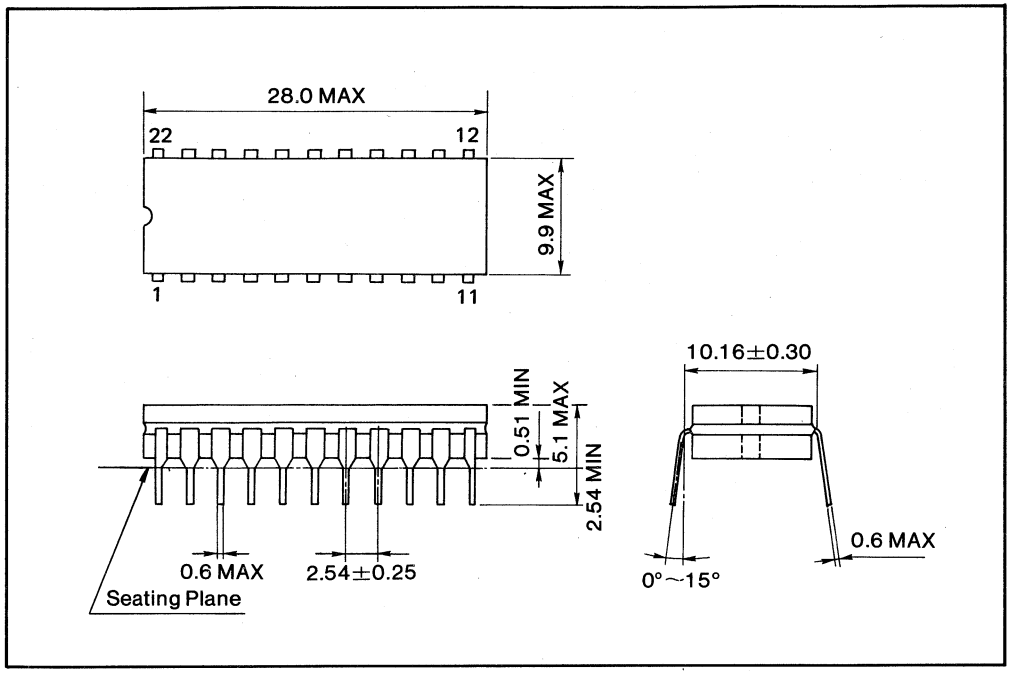


II

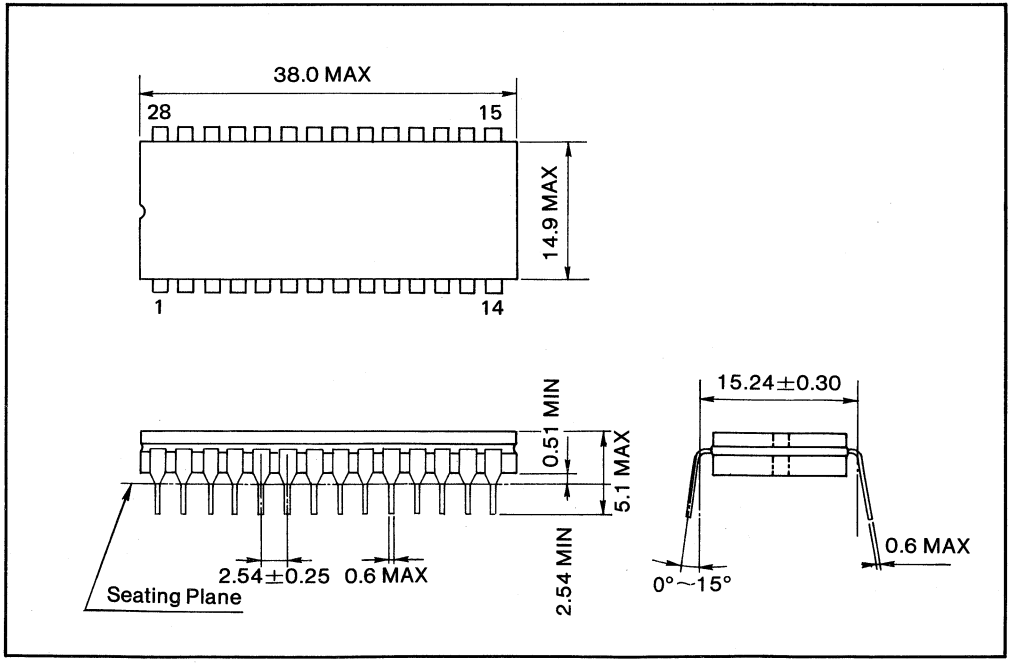
• 16 PIN CERAMIC DIP (CERDIP)



• 22 PIN CERAMIC DIP (CERDIP)

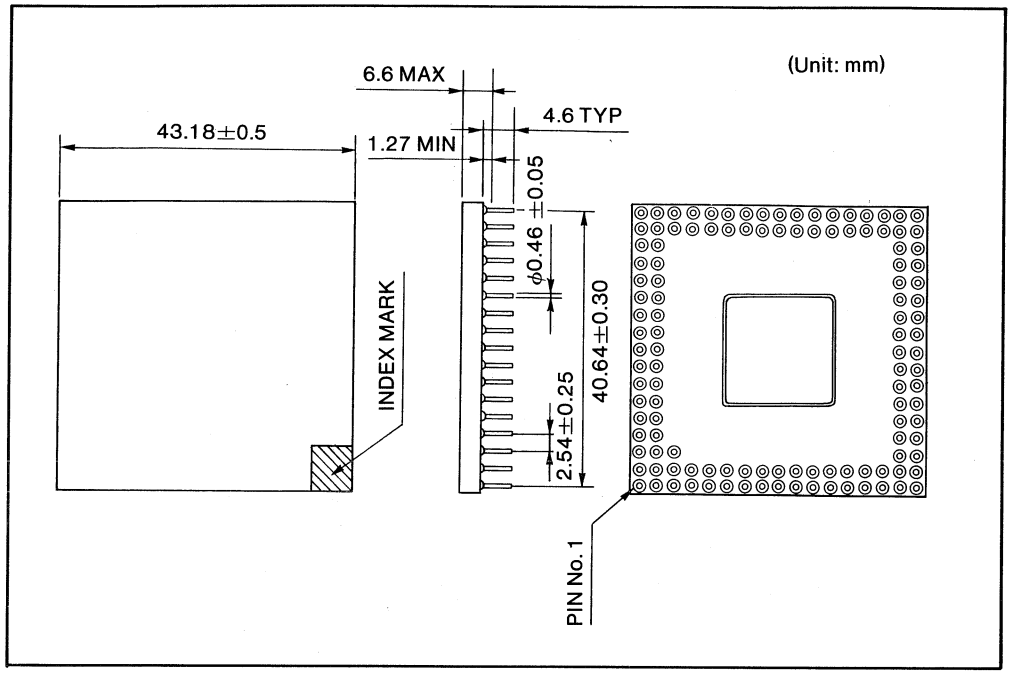


• 28 PIN CERAMIC DIP (CERDIP)

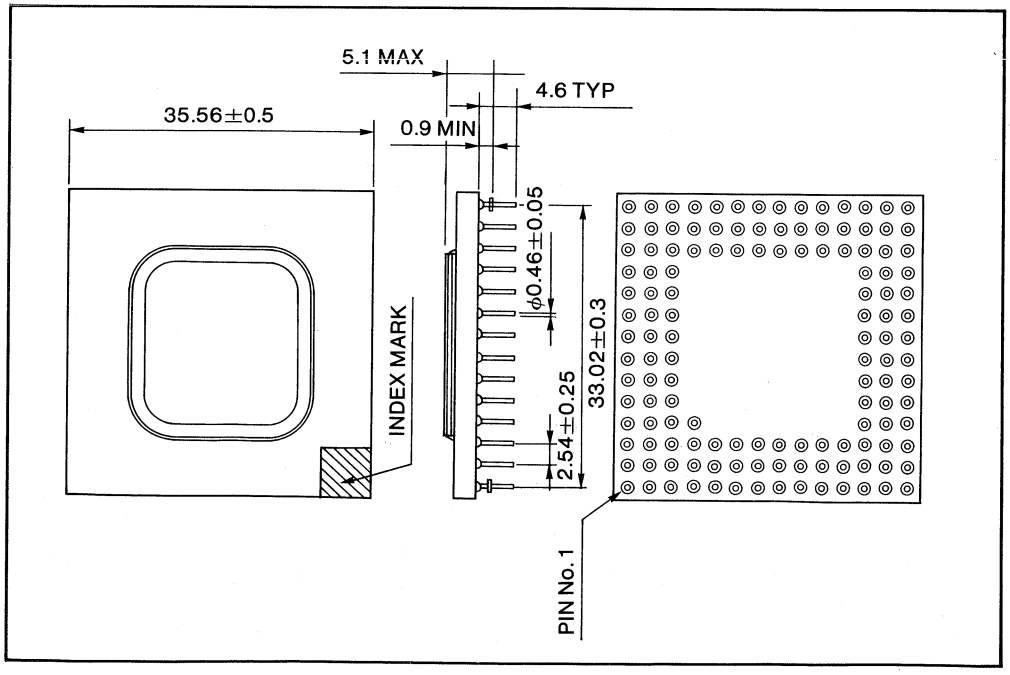


II

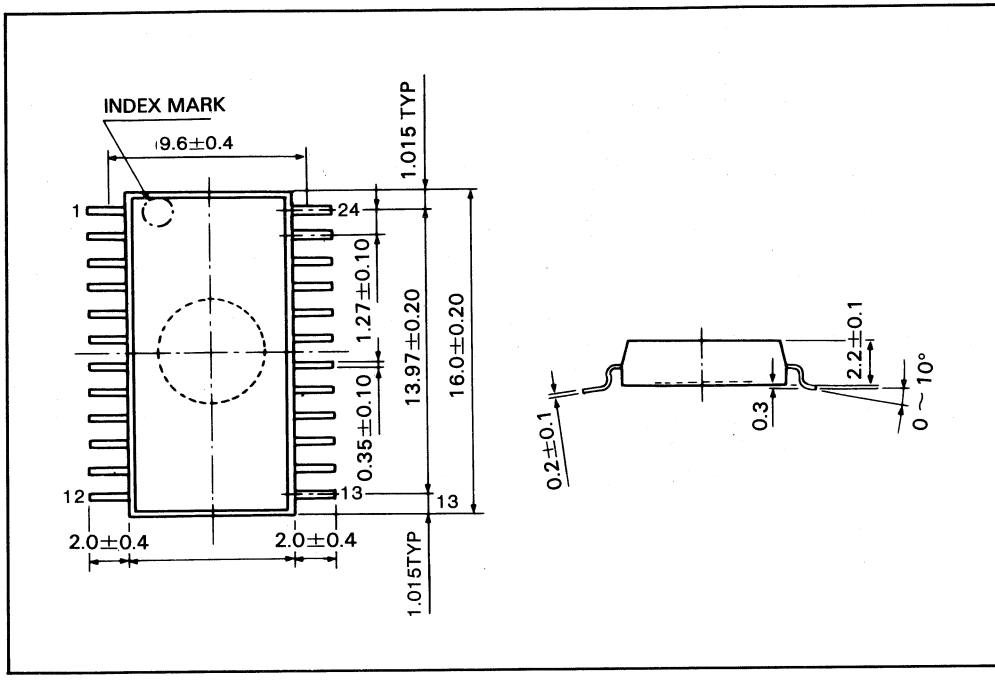
• 120 PIN CERAMIC PGA



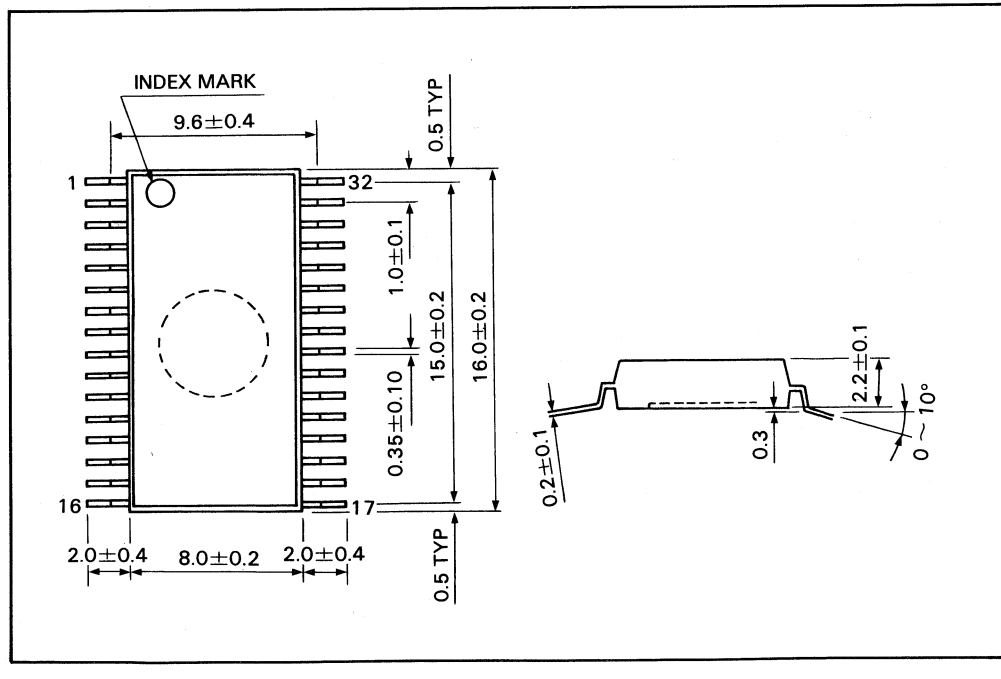
• 132 PIN CERAMIC PGA



• 24 PIN PLASTIC FLAT

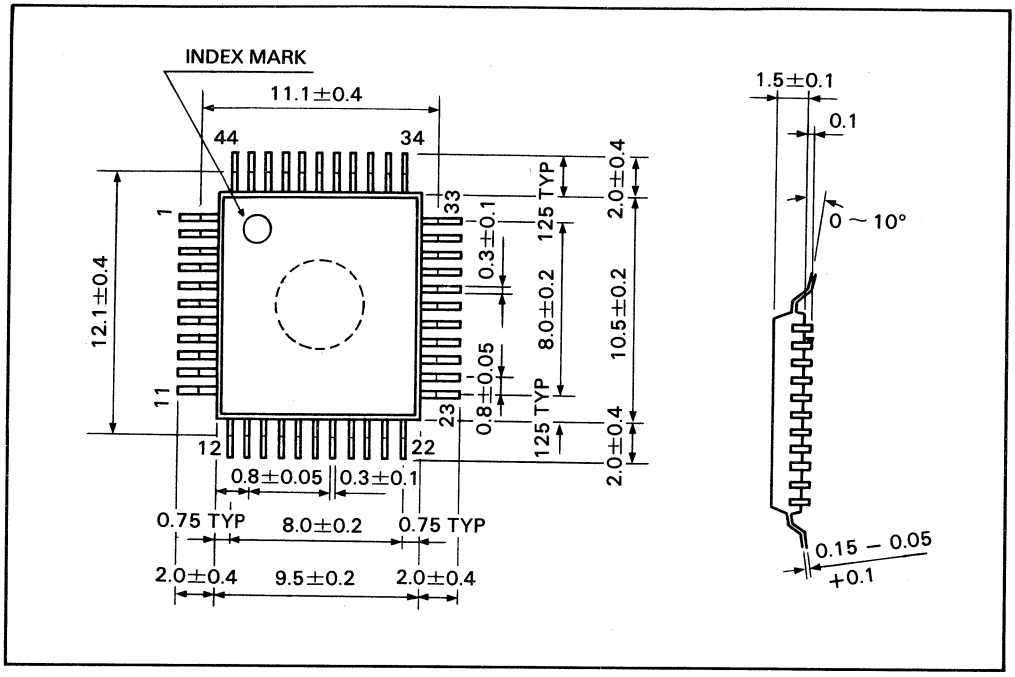


• 32 PIN PLASTIC FLAT

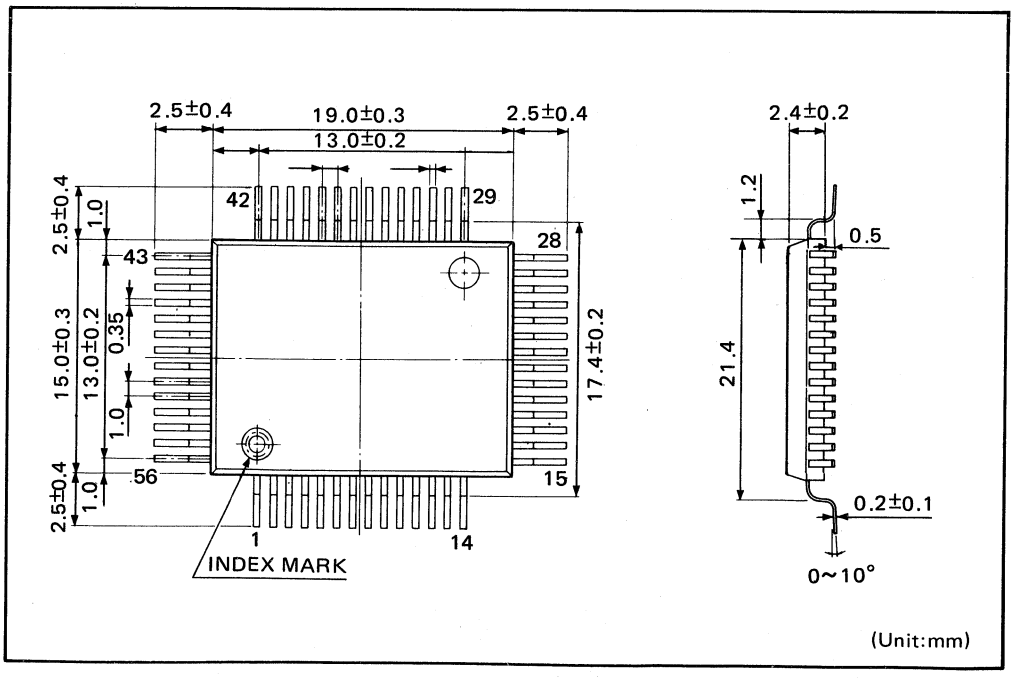


II

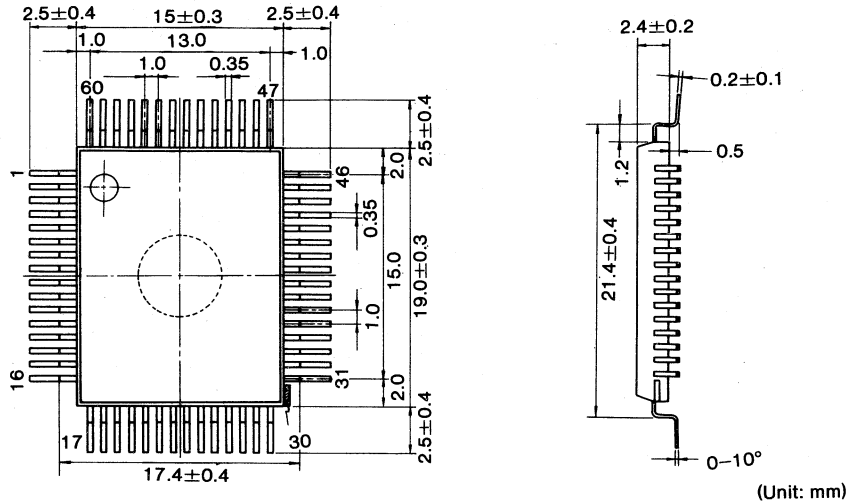
• 44 PIN PLASTIC FLAT



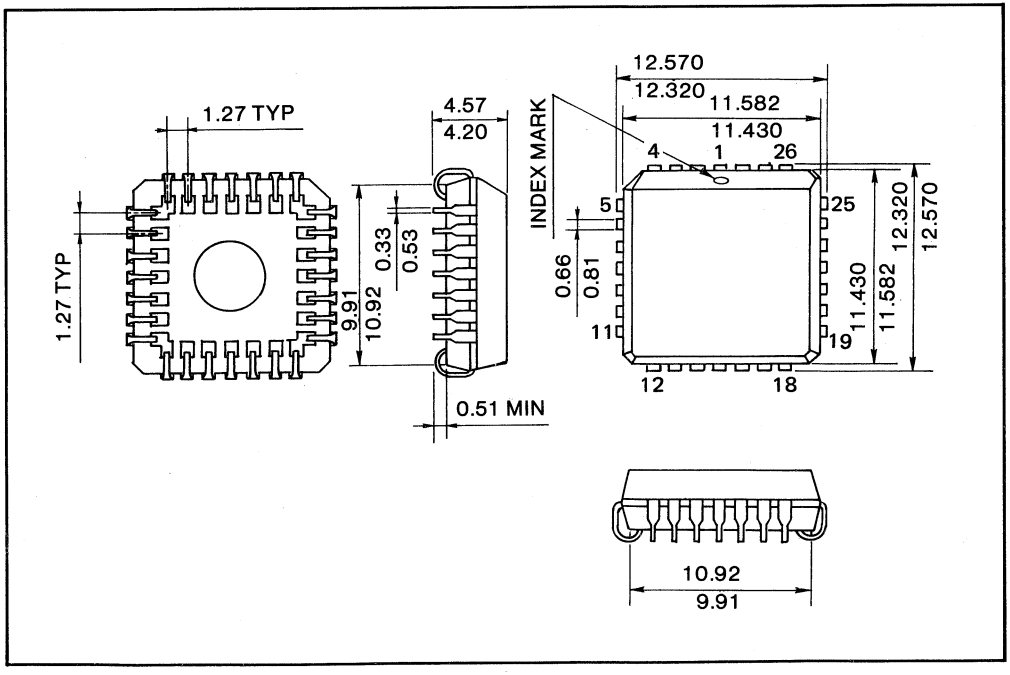
• 56 PIN PLASTIC FLAT (L)



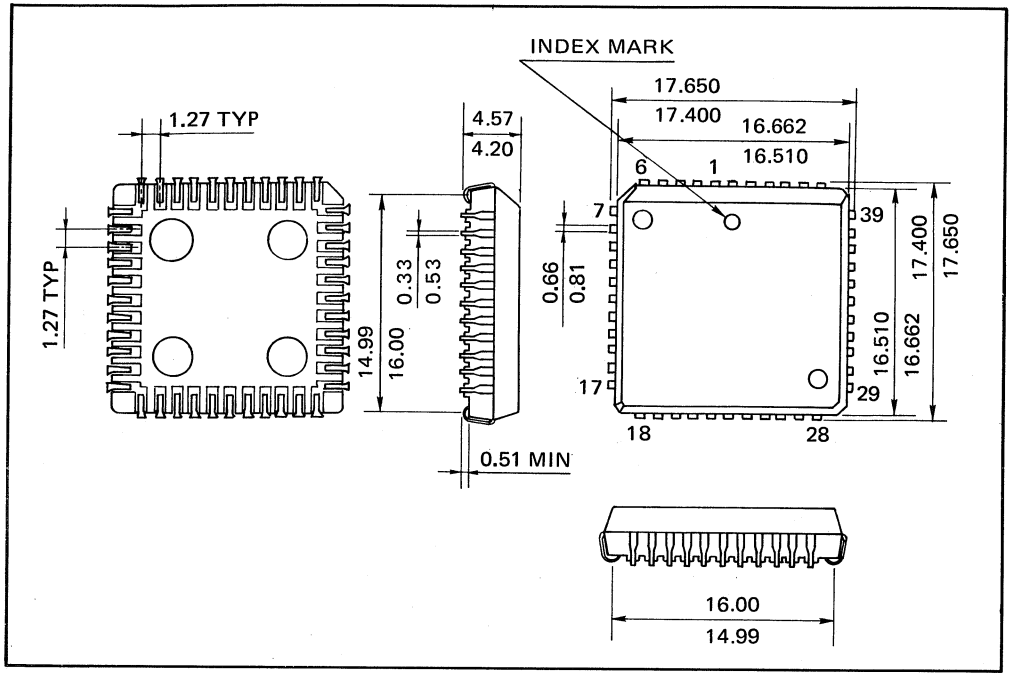
• 60 PIN PLASTIC FLAT



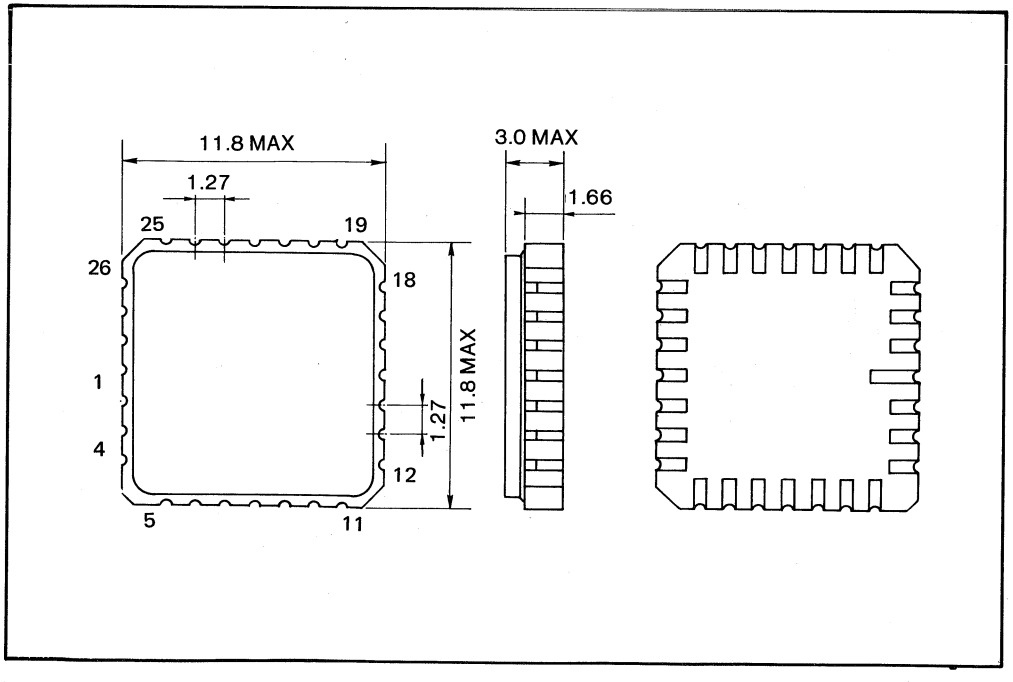
• 28 PIN PLCC



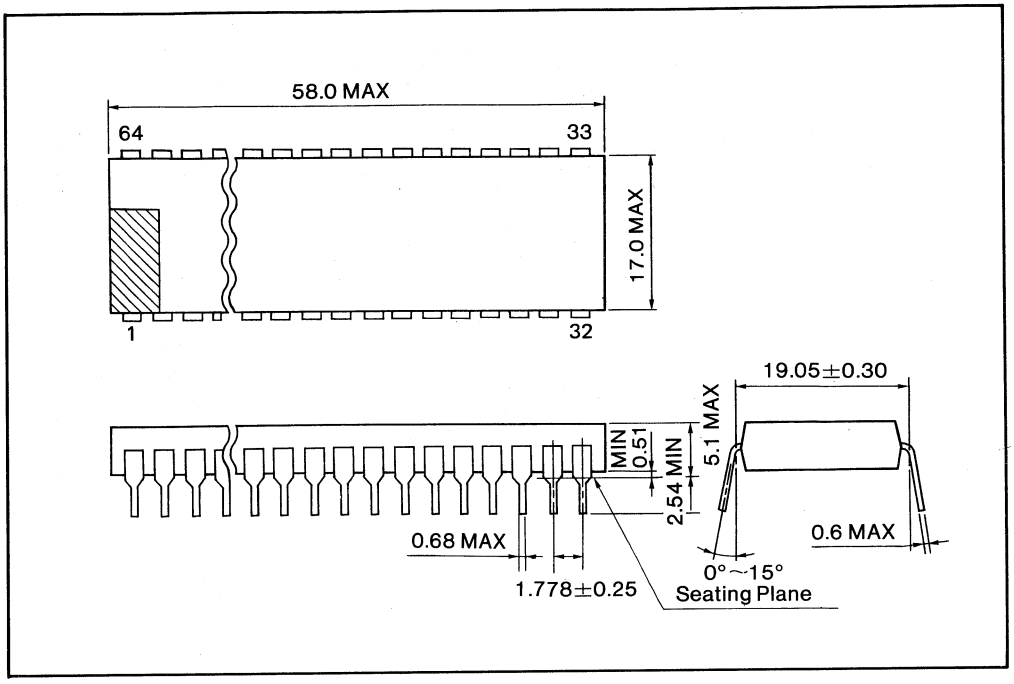
• 44 PIN PLCC



• 28 PIN CERAMIC CC



• 64 PIN MINI SIZE PLASTIC DIP



II

III
DATA SHEET

A. MODEM APPLICATION

III

OKI semiconductor

MSM6926 CCITT V.21/ MSM6946 BEL 103

300 BPS SINGLE CHIP MODEM

GENERAL DESCRIPTION

The MSM6926 and the MSM6946 are OKI's 300 bps single chip modem series that transmit and receive serial, binary data over a switched telephone network using frequency shift keyed (FSK) modulation.

The MSM6926 is compatible with CCITT V.21 series data sets, while the MSM6946 is compatible with Bell 103 series data sets.

These devices provide all the necessary modulation, demodulation, and filtering required to implement a serial, asynchronous communication link.

OKI's single chip modem series are designed for users who are not telecommunication experts and are easy to use cost effective alternative to standard discrete modem design.

CMOS LSI technology provides the advantages of small size, low power, and increased reliability.

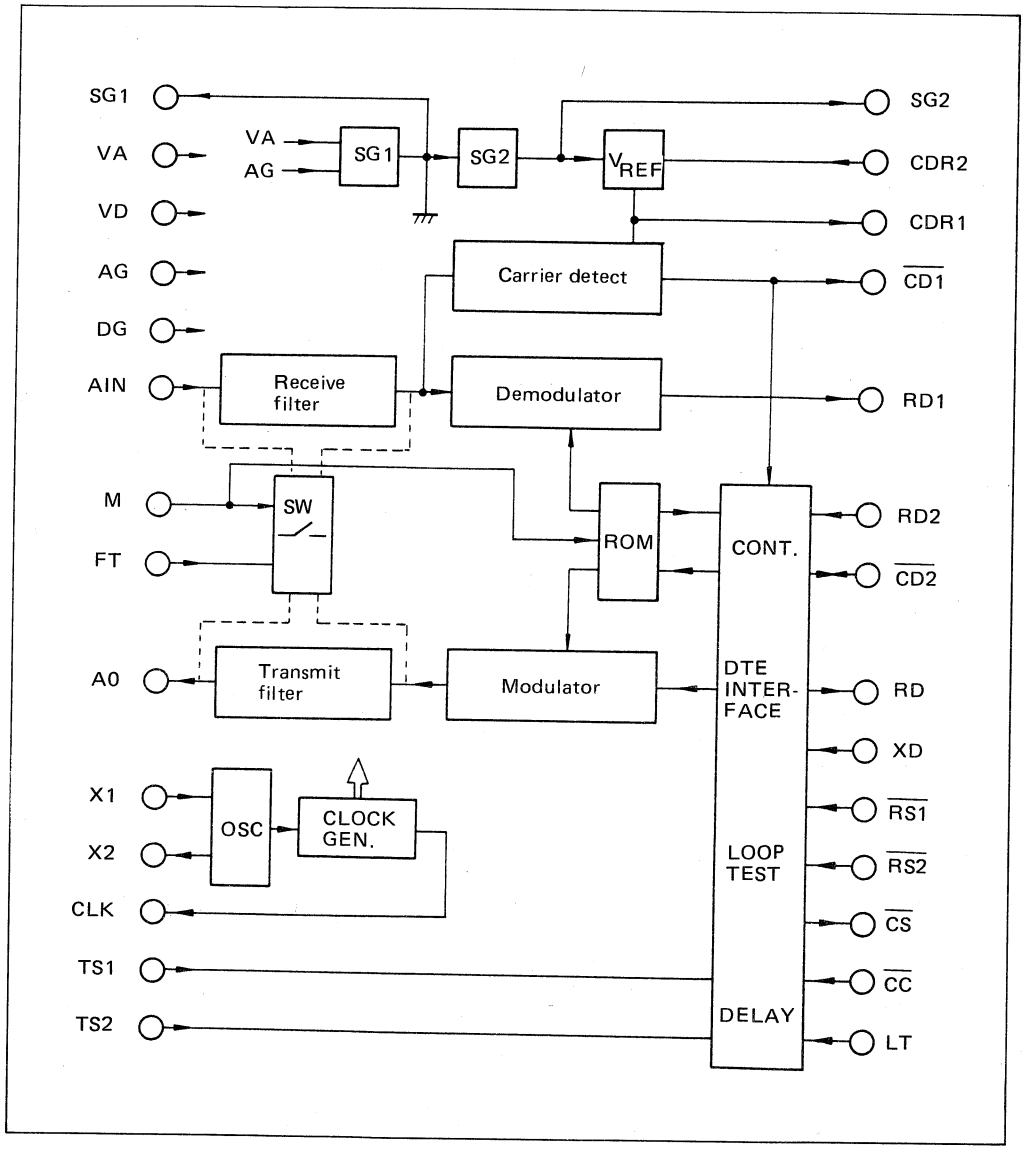
The design of the integrated circuit assures compatibility with a broad base of installed low speed modems and acoustic couplers. Applications include interactive terminals, desk top computers, point of sale equipment, and credit verification systems.

III

FEATURES

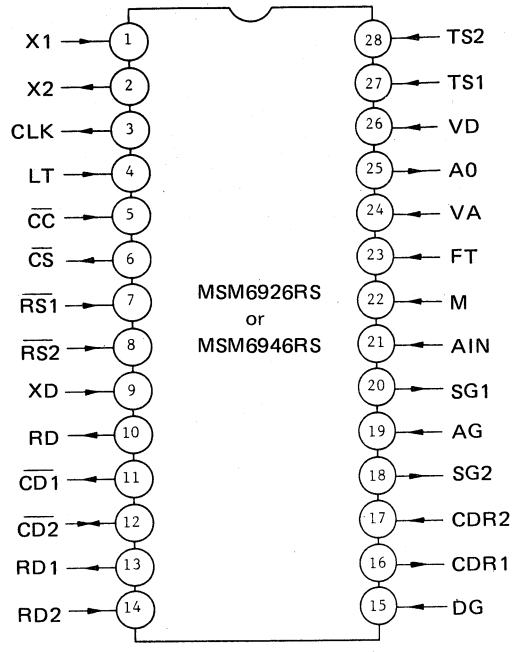
- Compatible with CCITT V.21 (MSM-6926)
- Compatible with BELL 103 (MSM6946)
- CMOS silicon gate process
- Switched capacitor and advanced CMOS analog technology
- Data rate from zero to 300 bps
- Full duplex (2-wire)
- Originate and Answer modes
- Selectable built-in timers and external delay timers possible
- All filtering, modulation, demodulation, and DTE interface on chip
- TTL compatible digital interface
- Low power dissipation 90 mW
- 28 pin plastic DIP package
- 44 pin plastic FLAT package

BLOCK DIAGRAM



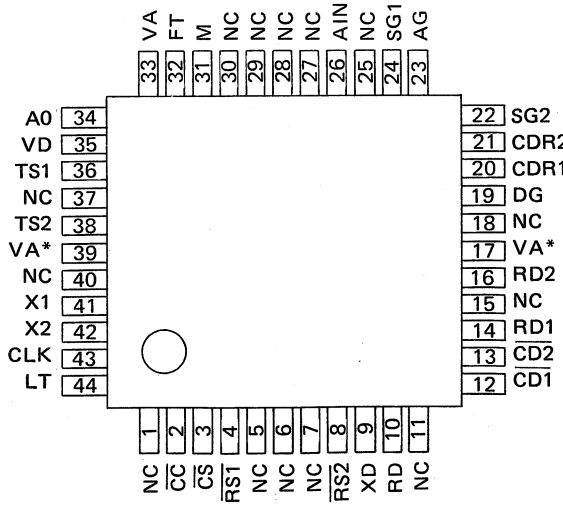
PIN CONFIGURATION (TOP VIEW)

28 LEAD PLASTIC DIP PACKAGE (RS)



III

44 LEAD PLASTIC FLAT PACKAGE (GS-K)



* Both No. 17 pin and No. 39 pin are set to be at VA level by setting No. 33 pin at VA level.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Ratings	Unit
Power supply voltage	VA	T_a = 25°C With respect to AG or DG	-0.3 ~ 15	V
	VD		-0.3 ~ 7	
Analog *1 input voltage	VIA		-0.3 ~ VA + 0.3	
Digital *2 input voltage	VID		-0.3 ~ VD + 0.3	
Operating temperature	T_{OP}	—	0 ~ 70	°C
Storage temperature	T_{STG}	—	-55 ~ 150	

*1 CDR2, A_{IN}

*2 X1, LT, $\overline{CC}$, $\overline{RS1}$, $\overline{RS2}$, XD, $\overline{CD2}$ *3, RD2, M, FT, T_{S1}, T_{S2}

*3: $\overline{CD2}$ is I/O terminal.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Power supply voltage	VA	With respect to AG	10.8	12.0	13.2	V
	VD	With respect to DG	4.75	5.00	5.25	
	AG, DG			0		
Operating temperature	T_{OP}		0		70	°C
CRYSTAL				3.579545		MHz
R_1		Transformer impedance = 600Ω		600		Ω
R_2				51		kΩ
R_3				51		
R_4				51		
R_5				51		
R_6				51		
R_7				51		
R_8				33		
R_9				51		
C_0, C_1				0.047		μF
C_2				2.2		
C_3			1.0			
C_4			0.01			
C_5				10		
C_6				10		

Application circuits using above conditions are proviced in Figure 8.

DC AND DIGITAL INTERFACE CHARACTERISTICS

(VA = 12 V ±10%, VD = 5 V ±5%, T_a = 0 ~ 70°C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Power supply current	IA	Ordinary operation		7.5	15.0	mA
	ID			1.0	2.0	
Input leakage current *1	I_{IL}	$V_I = O_V$	-10		10	μA
	I_{IH}	$V_I = V_D$	-10		10	
Input voltage *1	V_{IL}		0		0.8	V
	V_{IH}		2.2		VD	
Output voltage *2	V_{OL}	I_{OL} = 1.6 mA	0		0.4	
	V_{OH}	I_{OH} = 400 μA	0.8 · VD		VD	

*1 LT, $\overline{CC}$, $\overline{RS1}$, $\overline{RS2}$, XD, $\overset{*3}{\overline{CD2}}$, RD2, M, FT, T_{S1}, T_{S2}

*2 CLK, $\overline{CS}$, RD, $\overline{CD1}$, $\overset{*3}{\overline{CD2}}$, RD1

*3 $\overline{CD2}$ is I/O terminal.

III

ANALOG INTERFACE CHARACTERISTICS

1. MSM6926

(VA = 12 V ±10%, VD = 5 V ±5%, T_a = 0 ~ 70°C)

Parameter		Symbol	Condition	Min	Typ	Max	Unit
Transmit Carrier Out (A_O)							
ORIGINATE MODE Carrier frequency	Mark 1	f_{OM}	$f_{CRYSTAL}$ = 3.579545 MHz	974	980	986	Hz
	Space 0	f_{OS}		1174	1180	1186	
ANSWER MODE Carrier frequency	Mark 1	f_{AM}		1644	1650	1656	
	Space 0	f_{AS}		1844	1850	1856	
Output resistance		R_{OXA}				200	Ω
Load resistance		R_{LXA}		50			kΩ
Load capacitance		C_{LXA}				100	PF
Transmit level		V_{OXA}		4	6	8	*1 dBm
Output offset voltage		V_{OSX}		$\frac{VA}{2}$ -1	$\frac{VA}{2}$	$\frac{VA}{2}$ + 1	V
Out-of-band energy (referred to carrier level)		E_{OX}	C_1 = 0.047 μF	Refer to Figure 1			dB
Receive Carrier Input (A_{IN})							
Input resistance		R_{IRA}		100			kΩ
Receive signal level range		V_{IRA}		-48		-6	*1 dBm
Carrier detect level	ON	V_{CD} ON	R_8 = 33 kΩ*2, R_9 = 51 kΩ			-43	
	OFF	V_{CD} OFF		-48			
Carrier detect hysteresis		H_{YS}	V_{CD} ON − V_{CD} OFF	2			dB
Receive Filter							
Group delay distortion		D_{DL}	ORIG. MODE, 1600 ~1900 Hz		800		μS
			ANS. MODE, 930 ~ 1230 Hz		850		
Adjacent channel rejection		L_{AC}	V_{AIN} = −6 dBm	50			dB

Note: *1 0 dBm = 0.775 Vrms

*2 The resistor values are typical.

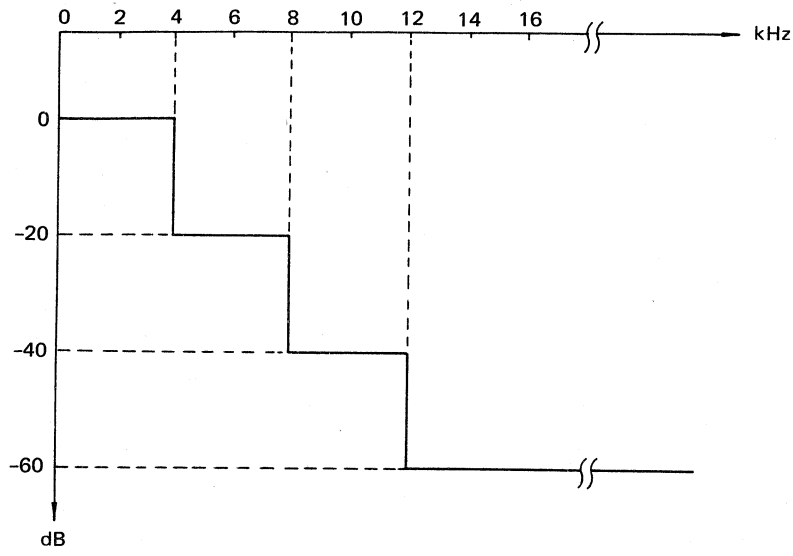


Figure 1 MSM6926 Out-of-Band Energy referred to Carrier Level (C_1 = 0.047 μF)

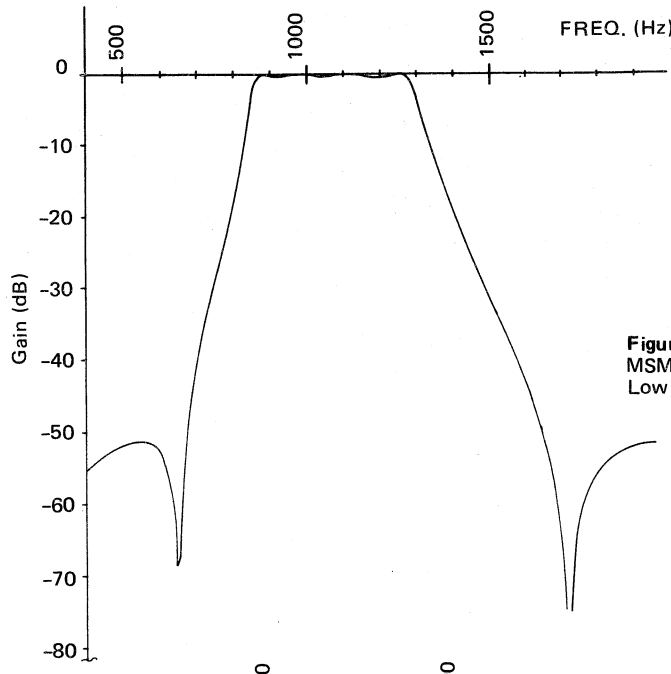


Figure 2
MSM6926
Low Band Filter

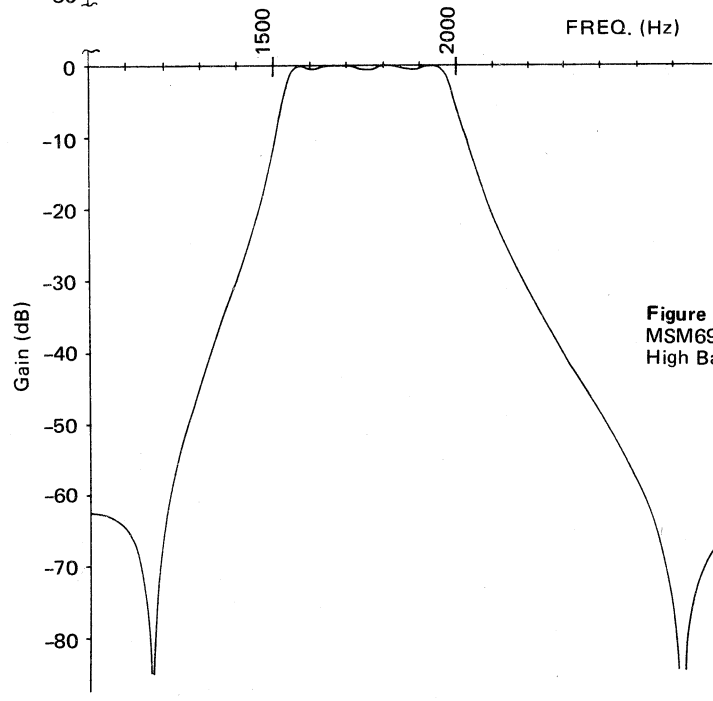


Figure 3
MSM6926
High Band Filter

III

2. MSM6946

(V_A = 12 V ±10%, V_D = 5 V ±5%, T_a = 0 ~ 70°C)

Parameter		Symbol	Condition	Min	Typ	Max	Unit
Transmit Carrier Out (A_O)							
ORIGINATE MODE Carrier frequency	Mark 1	f_{OM}	$f_{CRYSTAL}$ = 3.579545 MHz	1264	1270	1276	Hz
	Space 0	f_{OS}		1064	1070	1076	
ANSWER MODE Carrier frequency	Mark 1	f_{AM}		2219	2225	2231	
	Space 0	f_{AS}		2019	2025	2031	
Output resistance		R_{OXA}				200	Ω
Load resistance		R_{LXA}		50			kΩ
Load capacitance		C_{LXA}				100	PF
Transmit level		V_{OXA}		4	6	8	*1 dBm
Output offset voltage		V_{OSX}		$\frac{VA}{2}-1$	$\frac{VA}{2}$	$\frac{VA}{2}+1$	V
Out-of-band energy (referred to carrier level)		E_{OX}	C_1 = 0.047 μF	Refer to Figure 4			dB
Receive Carrier Input (A_{IN})							
Input resistance		R_{IRA}		100			kΩ
Receive signal level range		V_{IRA}		-48		-6	*1 dBm
Carrier detect level	ON	V_{CD} ON	R_8 = 33 kΩ*2, R_9 = 51 kΩ R			-43	
	OFF	V_{CD} OFF		-48			
Carrier detect hysteresis		H_{YS}	V_{CD} ON − V_{CD} OFF	2			dB
Receive Filter							
Group delay distortion		D_{DL}	ORIG. MODE 1975 ~ 2275 Hz		650		μS
			ANS. MODE 1020 ~ 1320 Hz		750		
Adjacent channel rejection		L_{AC}	V_{AIN} = −6 dBm	50			dB

Note: *1 0 dBm = 0.775 Vrms

*2 The resistor values are typical.

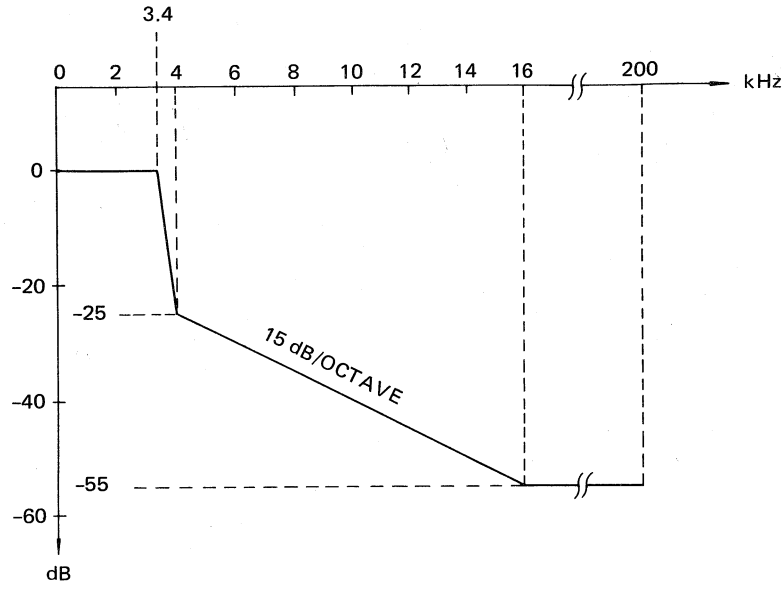


Figure 4 MSM6946 Out-of-Band Energy referred to Carrier Level (C_1 = 0.047 μF)

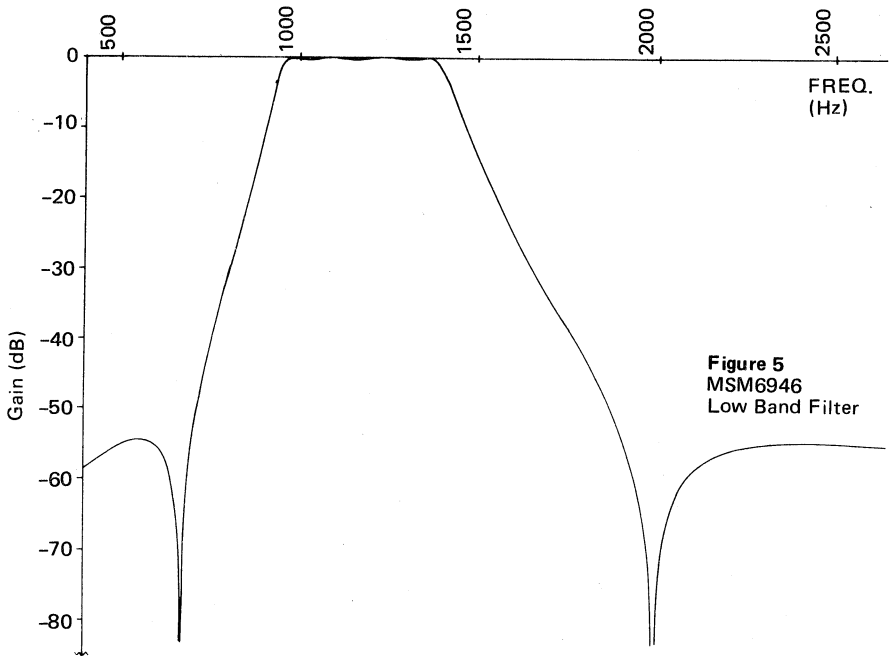


Figure 5
MSM6946
Low Band Filter

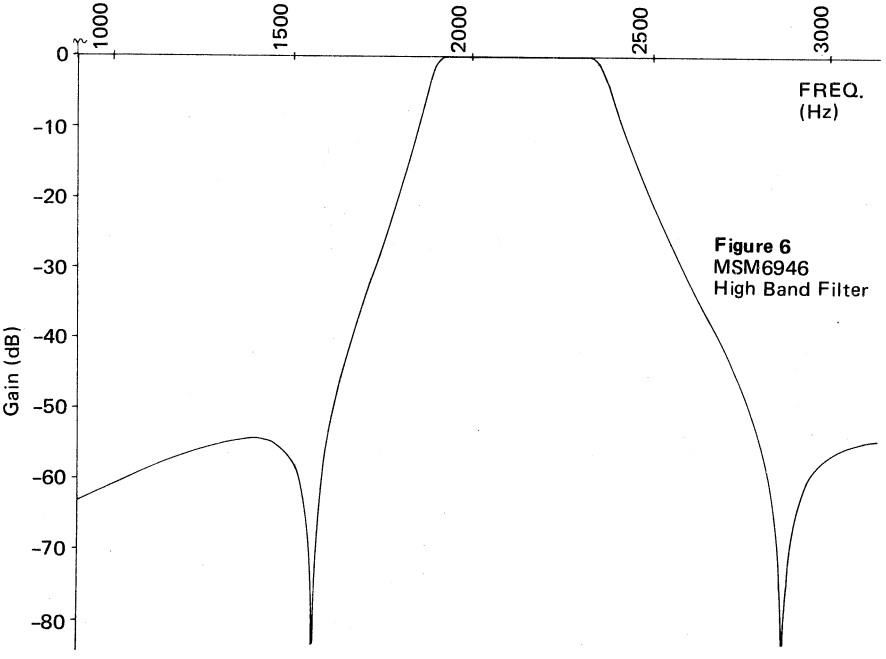


Figure 6
MSM6946
High Band Filter

DEMODULATED BIT CHARACTERISTICS

(VA = 12 V ±10%, VD = 5 V ±5%, T_a = 0 ~ 70°C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Peak intersymbol distortion	ID	Back-to-back over input signal range -6 to -40 dBm. 511-bit test pattern.		6		%
Bit error rate	BER	Back-to-back with 0.3 ~ 3.4 kHz flat noise. Receive signal level -25 dBm. 511-bit test pattern. S/N (dB) = 5		10^{-5}		

TIMING CHARACTERISTICS

1. MSM6926

(VA = 12 V ±10%, VD = 5 V ±5%, T_a = 0 ~ 70°C)

Parameter	Symbol	Condition	TS2	TS1	Min	Typ	Max	Unit
RS/CS delay time	T_{RC} ON	RS1 = "0" → CS = "0"	0	0	395	400	405	ms
			0	1	25	30	35	
			1	0	345	350	355	
			1	1	External delay timer			
	T_{RC} OFF	RS1 = "1" → CS = "1"	*	*	0		0.5	
CD/ON delay time	T_{CD} ON		0	0	300		320	
			0	1	5		20	
			1	0	150		170	
			1	1	External delay timer			
CD/OFF delay time	T_{CD} OFF		0	0	20		70	
			0	1	20		70	
			1	0	10		40	
			1	1	External delay timer			
Soft Turn-OFF time	T_{ST}		*	*		10		

Refer to Figure 7.

Note: * ..... Irrespective of 1/0 condition.

2. MSM6946

(VA = 12 V ±10%, VD = 5 V ±5%, T_a = 0 ~ 70°C)

Parameter	Symbol	Condition	TS2	TS1	Min	Typ	Max	Unit
RS/CS delay time	T_{RC} ON	RS1 = "0" → CS = "0"	0	0	195	200	205	ms
			0	1		+		
			1	0		+		
			1	1	External delay timer			
	T_{RS} OFF	RS1 = "1" → CS = "1"	*	*	0		0.5	
CD/ON delay time	T_{CD} ON		0	0	100		120	
			0	1		+		
			1	0		+		
			1	1	External delay timer			
CD/OFF delay time	T_{CD} OFF		0	0	10		50	
			0	1		+		
			1	0		+		
			1	1	External delay timer			
Soft Turn-OFF time	T_{ST}		*	*		10		

Refer to Figure 8.

Note: * ..... Irrespective of 1/0 condition.
+ ..... Reserved

TIMING DIAGRAM

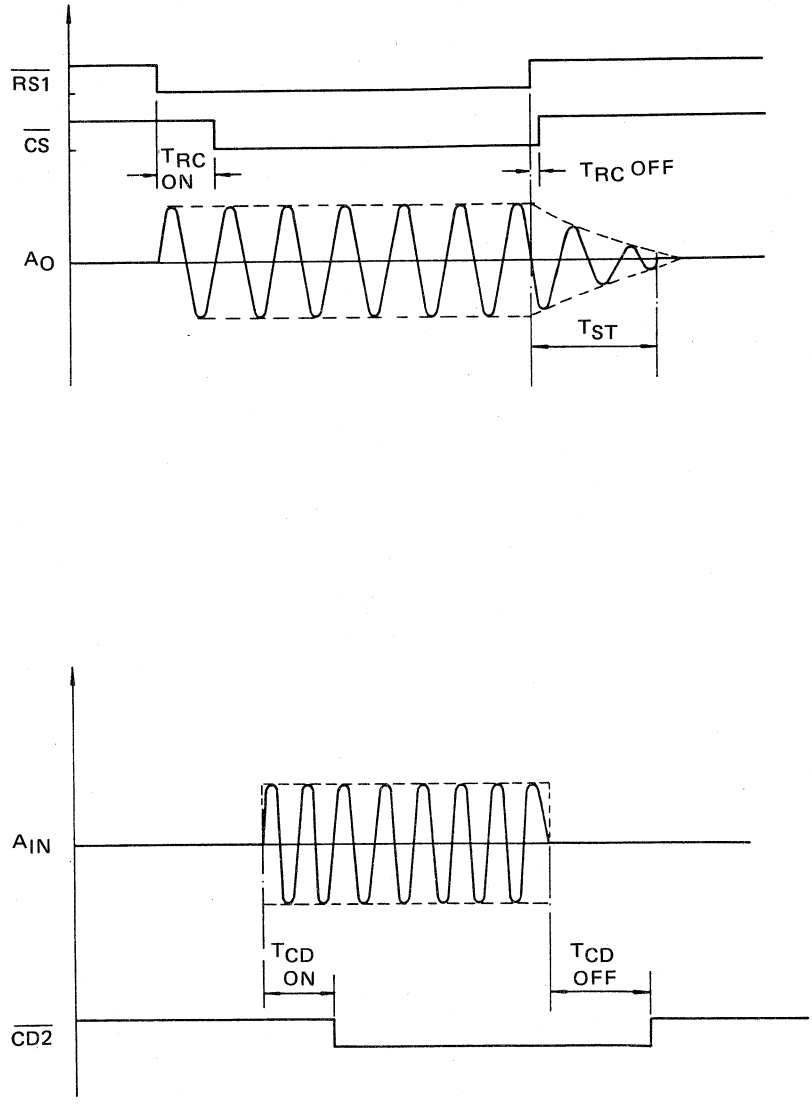


Figure 7 MSM6926/6946 Timing Diagram

PIN DESCRIPTIONS

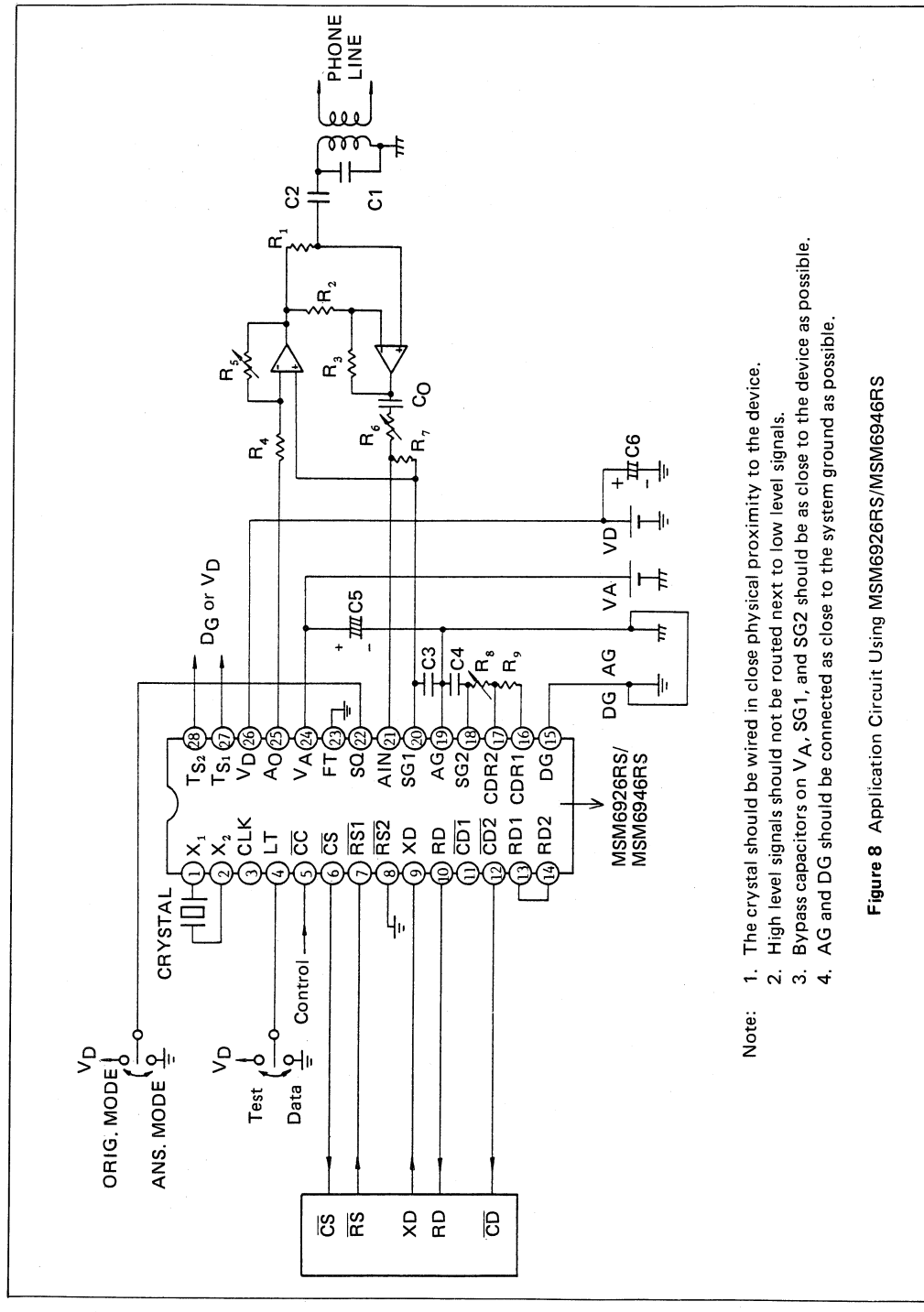
Name	Pin No. RS	Pin No. GS-K	I/O	Function
POWER				
DG	15	19		Ground reference of V_D (digital ground)
AG	19	23		Ground reference of V_A (analog ground)
V_A	24	33		Supply voltage (+12 V nominal)
V_D	26	35		Supply voltage (+5 V nominal)
CLOCKS				
X1	1	41		Master clock timing is provided by either a series resonant crystal (3.579545 MHz ±0.01%) connected across X1 and X2, or by an external TTL/CMOS clock driving X2 with AC coupling where X1 is left unconnected. See Figure 10.
X2	2	42		
CLK	3	43	O	873.9 Hz clock output. This clock is used to implement external delay circuits etc.
CONTROL				
LT	4	44	I	Digital loop back. During digital "High", any data sent on the X_D pin will appear on the RD pin, and any data sent on the $\overline{RS1}$ pin will immediately appear on the $\overline{CS}$ pin. Any data demodulated from the received carrier on the A_{IN} pin will be the modulated data to implement the transmitted carrier. In this case, sending the transmitted carrier to the phone line depends on the $\overline{CC}$, but never on $\overline{RS1}$.
$\overline{CC}$	5	2	I	During digital loopback, the data on this pin becomes a control signal for sending the transmitted carrier to the phone line in place of $\overline{RS1}$.
$\overline{RS2}$	8	8	I	When an external circuit gives the RS/CS delay time which is not within the device as required, this pin should be connected to the external circuit output. See Figure 11.
$\overline{CD1}$	11	12	O	The fast carrier detection output. This pin is internally connected to the input of the built-in carrier detect delay circuit. When an external delay circuit provides the delay time which is not within the device as required, the $\overline{CD1}$ should be connected to the external circuit input. See Figure 11.

Name	Pin No. RS	Pin No. GS-K	I/O	Function
$\overline{CD2}$	12	13	I/O	When an external circuit gives the carrier detect delay time which is not within the device as required, this pin becomes the input pin for the external circuit output signal. In other cases (when using the delay time within the device, the data on the TS1 or TS2 is not digital "High"), this pin becomes the Carrier-Detect signal output.
RD1	13	14	O	The RD1 data is demodulated data from the received carrier and the RD2 is the input of the following logic circuits referred to in Figure 12. Usually, the RD1 data is input directly to RD2. In some cases, as input data to RD2, the data that is controlled by NCU (Network-Control-Unit) etc. may be required in stead of the RD1 data.
RD2	14	16	I	
CDR1	16	20	O	These two pins are the output (CRD1) and inverting input (CDR2) of the buffer operational amplifier of which noninverting input is connected to the built-in voltage reference, stabilized to variations in the supply voltage and temperature. See Figure 13. An adequate carrier-detect level can be set by selecting the ratio of R_8 and R_9. Therefore, the loss in the received carrier level by phone-line transformer can be compensated by adjusting the ratio of R_8 and R_9. $R_8 + R_9$ should be greater than 50 kΩ.
CDR2	17	21	I	
M	22	31	I	Answer/Originate mode select. During digital "High", the originate mode is selected. A low input selects the answer mode.
FT	23	32	I	This pin may be used for device tests only. During digital "High", the A_O pin will be connected to receiving filter output instead of transmitting filter output.
TS1	27	36	I	RS/CS delay and carrier detect delay options referred to chapter about timing characteristics are selected by TS1 and TS2 inputs. Be careful that each delay can not be individually selected. If the other delay time unprovided within the device as option is required, input digital "High" to the TS1 and TS2 pin and implement the external delay circuits to obtain the desired delay characteristics. In this case, the CD2 pin becomes not only the input for the external circuit output signal, but also the Carrier Detect output. See Figure 11.
TS2	28	38	I	

III

Name	Pin No. RS	Pin No. GS-K	I/O	Function
				INPUT/OUTPUT
$\overline{CS}$	6	3	O	Clear-to-Send signal output. The digital "High" level indicates the "OFF" state and digital "Low" indicates the "ON" state. This output goes "Low" at the end of a delay (RS/CS delay) initiated when $\overline{RS1}$ (Request-to-Send) goes "Low".
$\overline{RS1}$	7	4	I	Request-to-Send signal input. The digital "High" level indicates the "OFF" state. The digital "Low" level indicates the "ON" state and instructs the modem to enter the transmit mode. This input must remain "Low" for the duration of data transmission. "High" turns the transmitter off.
XD	9	9	I	This is digital data to be modulated and transmitted via A_O. Digital "High" will be transmitted as "Mark". Digital "Low" will be transmitted as "Space". No signal sppears at A_O unless $\overline{RS1}$ is "Low".
RD	10	10	O	Digital data demodulated from A_{IN} is serially available at this output. Digital "High" indicates "Mark" and digital "Low" indicates "Space". For example, under the following condition, this output is forced to be "Mark" state because the data may be invalid. • When $\overline{CD2}$ (Carrier-detect) is in the "OFF" state.
SG2	18	22	O	The SG1 and SG2 are built-in analog signal grounds. SG2 is used only for Carrier-Detect function. The DC voltage of SG1 is approximately 6 V, so the analog line interface must be implemented by AC coupling. See Figure 9. To make impedance lower and ensure the device performance, it is necessary to put bypass capacitors on SG1 and SG2 in close physical proximity to the device.
SG1	20	24	O	
A_{IN}	21	26	I	This is the input for the analog signal from the phone line. The modem extracts the information in this modulated carrier and converts it into a serial data stream for presentation at RD output.
A_O	25	34	O	This analog output is the modulated carrier to be conditioned and sent over the phone line.

APPLICATION CIRCUIT



Note:
1. The crystal should be wired in close physical proximity to the device.
2. High level signals should not be routed next to low level signals.
3. Bypass capacitors on V_A, SG1, and SG2 should be as close to the device as possible.
4. AG and DG should be connected as close to the system ground as possible.

Figure 8 Application Circuit Using MSM6926RS/MSM6946RS

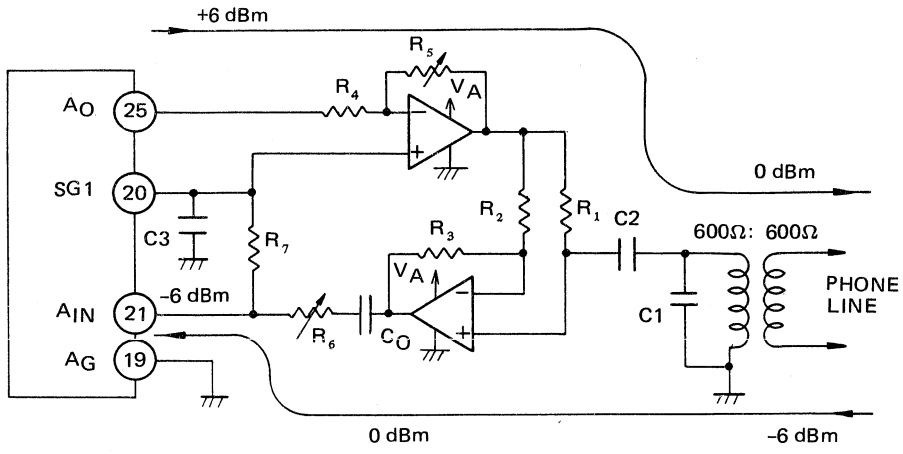
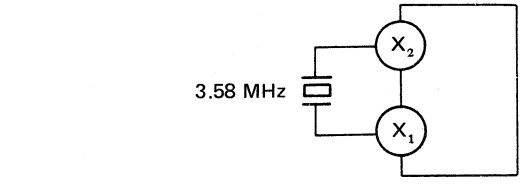


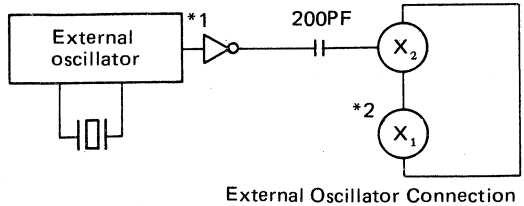
Figure 9-2 MSM6926RS/MSM6946RS Application

C_0, C_1	0.047 μF	R_2	51 kΩ	R_6	(51 kΩ)	Receive signal level
C_2	2.2 μF	R_3	51 kΩ	R_7	51 kΩ	
C_3	1 μF	R_4	51 kΩ	R_8	(33 kΩ)	Carrier detect level
R_1	600 Ω	R_5	(51 kΩ) Transmit signal level	R_9	51 kΩ	

Note: The signal level on the A_{IN} pin should not exceed -6 dBm.



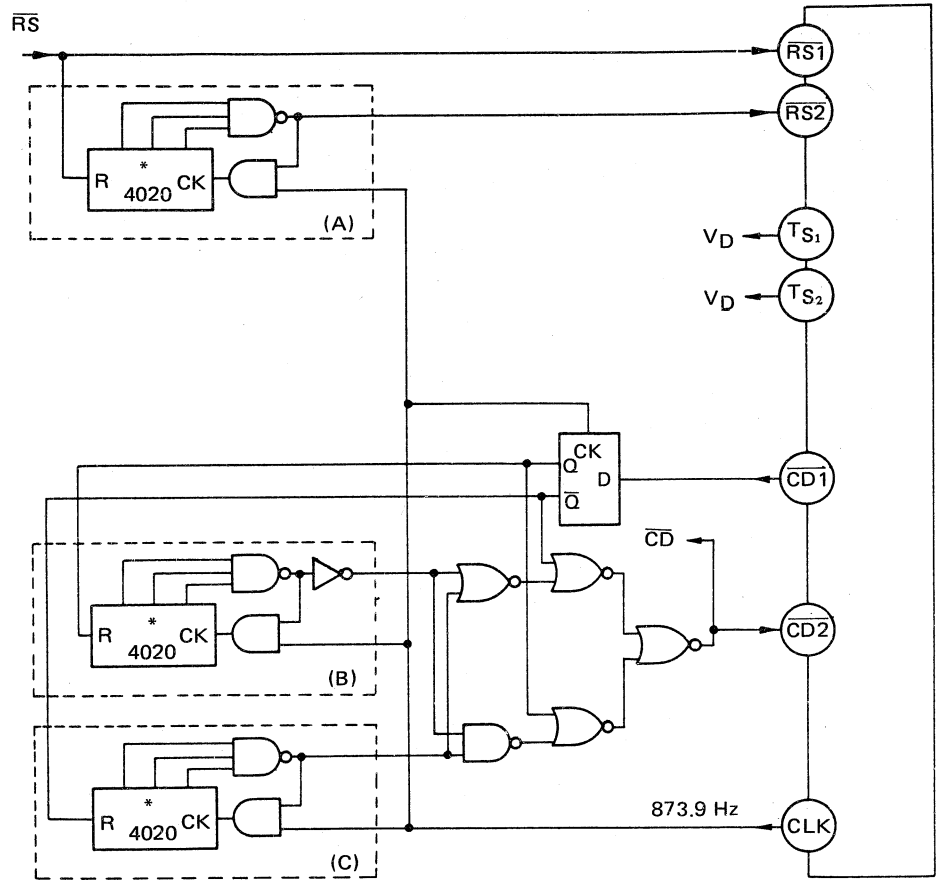
Crystal Oscillator Connection



External Oscillator Connection

*1 TTL or Hi-Speed CMOS GATE
*2 Left unconnected

Figure 10



(A) RS/CS delay, (B) CD/ON delay, (C) CD/OFF delay

Note: Supply voltage equals V_D for all gates.

*: The desired delay can be realized by selecting the appropriate bits from 4020's outputs. The number of the bits is not always 3. Each delay can be set differently from built-in delays.

Figure 11 External Delays Connection

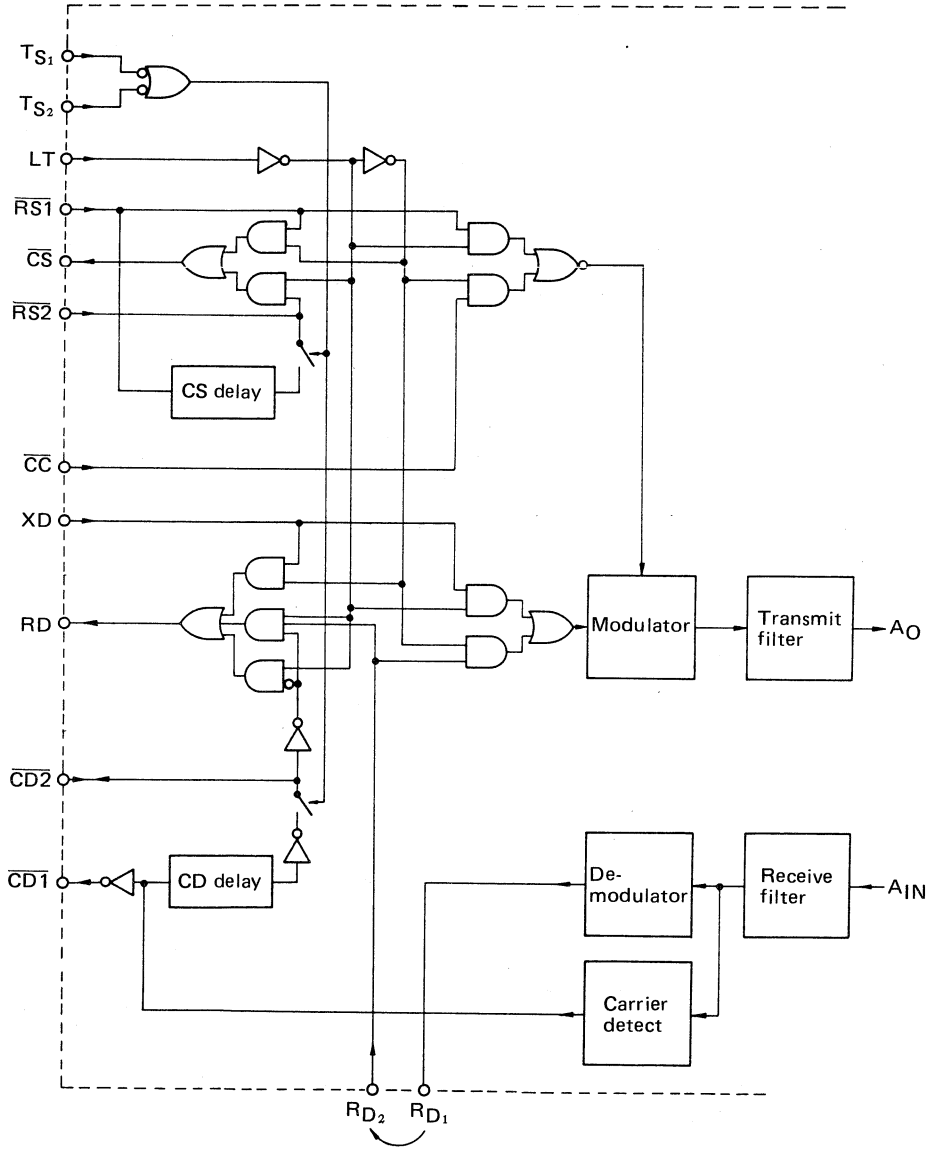


Figure 12 Equivalent Logic Interface of the Integrated Modem

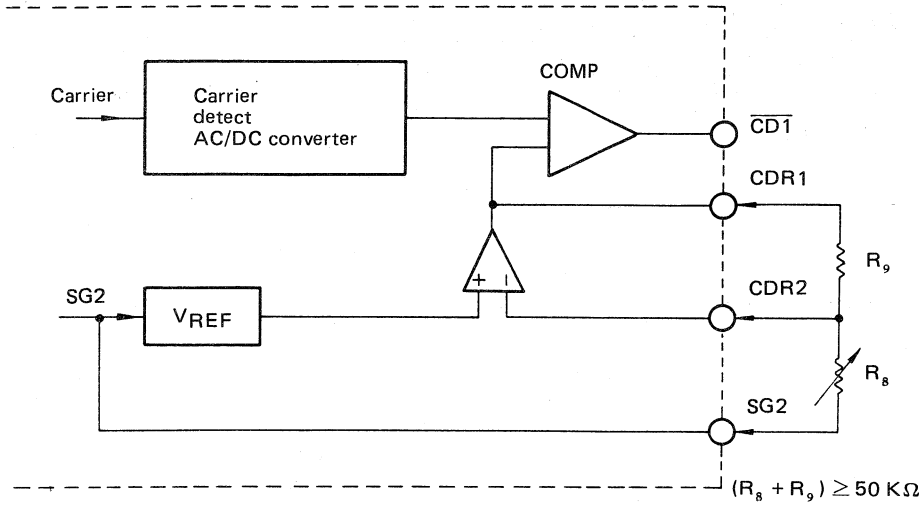


Figure 13 External Resistor Connection for the Setting of Carrier Detect Level

III

MSM6927 CCITT V.23/ MSM6947 BELL 202

1200 BPS SINGLE CHIP MODEM

GENERAL DESCRIPTION

The MSM6927 and the MSM6947 are OKI's 1200 bps single chip modem series that trasmit and receive serial, binary data over a telephone network using frequency shift keyed (FSK) modulation.

The MSM6927 is compatible with CCITT V.23 series data sets, while the MSM6947 is compatible with BELL 202 series data sets.

These devices provide all the necessary modulation, demodulation, and filtering required to implement a serial, asynchronous communication link.

OKI's single chip modem series are designed for users who are not telecommunication experts and are easy to use cost effective alternative to standard discrete modem design.

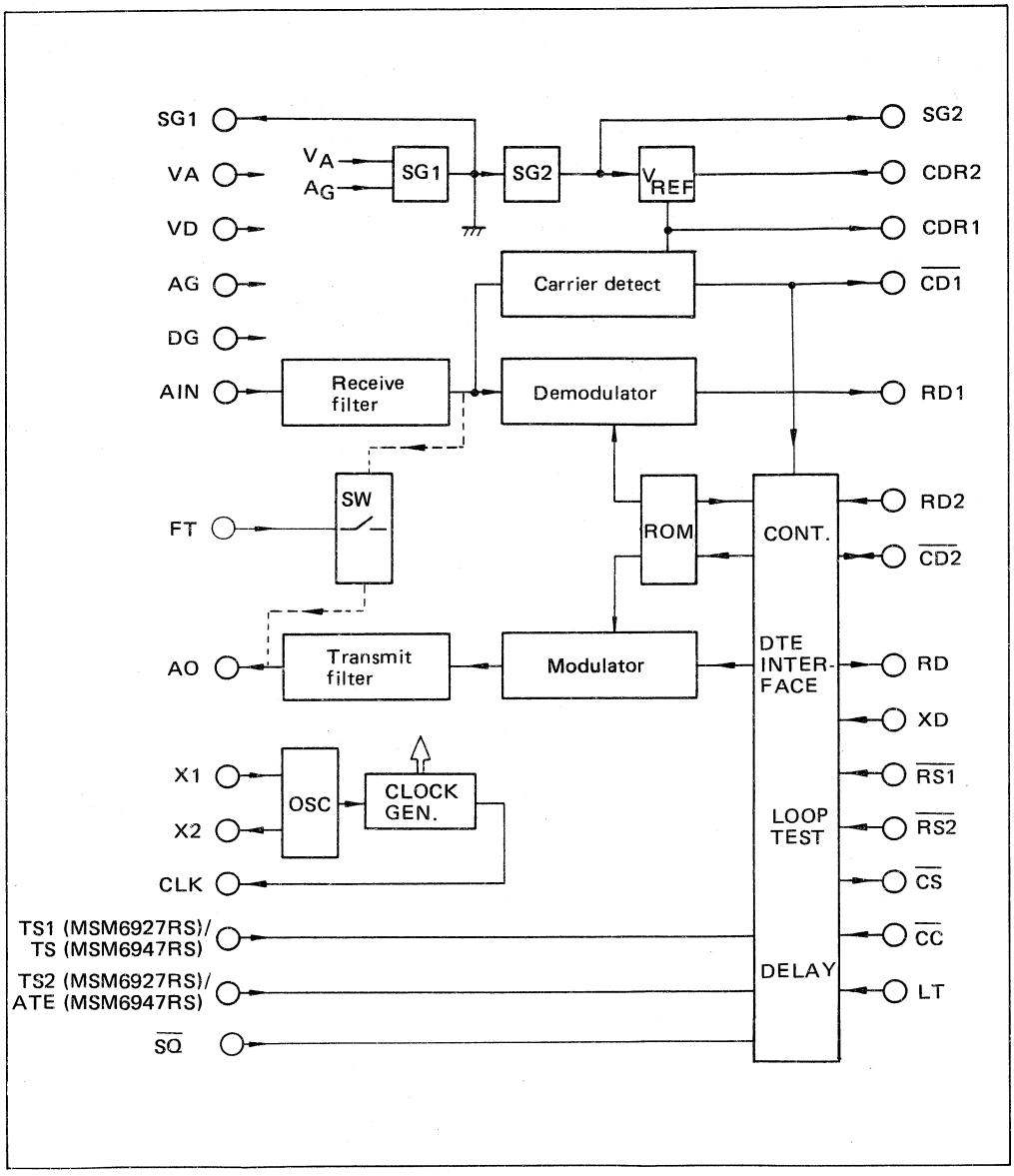
CMOS LSI technology provides the advantages of small size, low power, and increased reliability.

The design of the integrated circuit assures compatibility with a broad base of installed low speed modems and acoustic couplers. Applications include interactive terminals, desk top computers, point of sale equipment, and credi verification systems.

FEATURES

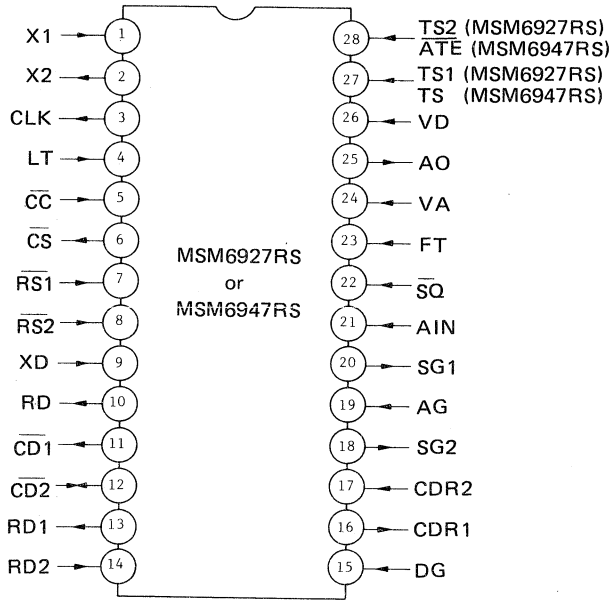
- Compatible with CCITT V.23 (MSM-6927)
- Compatible with BELL 202 (MSM6947)
- CMOS silicon gate process
- Switched capacitor and advanced CMOS analog technology
- Data rate from zero to 1200 b/s
- Half duplex (2-wire)
- Receive Squelch delay and Soft-Turn OFF
- Selectable built-in timers and external delay timers possible
- All filtering, modulation, demodulation, and DTE interface on chip
- Crystal controlled oscillator on chip
- TTL compatible digital interface
- Low power dissipation 90 mW
- 28 pin plastic DIP package
- 44 pin plastic FLAT package

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)

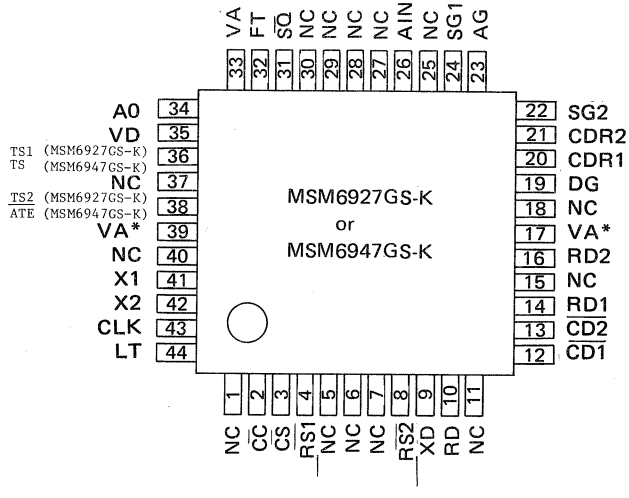
28 LEAD PLASTIC DIP PACKAGE (RS)



All pin descriptions except No. 27 and No. 28 pins are same for both MSM6927RS and MSM6947RS.

III

44 LEAD PLASTIC FLAT PACKAGE (GS-K)



All pin descriptions except No. 36 and No. 28 pins are same for both MSM6927GS-K and MSM6947GS-K.

* Both No. 17 pin and No. 39 pin are set to be at VA level by setting No. 33 pin at VA level.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Ratings	Unit
Power supply voltage	VA	T_a = 25°C With respect to AG or DG	-0.3 ~ 15	V
	VD		-0.3 ~ 7	
Analog *1 input voltage	VIA		-0.3 ~ VA + 0.3	
Digital *2 input voltage	VID		-0.3 ~ VD + 0.3	
Operating temperature	T_{OP}	–	0 ~ 70	°C
Storage temperature	T_{STG}	–	-55 ~ 150	

*1 CDR2, A_{IN}

*2 X1, LT, $\overline{CC}$, $\overline{RS1}$, $\overline{RS2}$, XD, $\overline{CD2}$ *3, RD2, $\overline{SQ}$, TS_1 (TS), $TS_2(\overline{ATE})$

*3 $\overline{CD2}$ is I/O terminal.

III

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Power supply voltage	VA	With respect to AG	10.8	12.0	13.2	V
	VD	With respect to DG	4.75	5.00	5.25	
	AG, DG			0		
Operating temperature	T_{OP}		0		70	°C
CRYSTAL				3.579545		MHz
R_1		Transformer impedance = 600Ω		600		Ω
R_2				51		kΩ
R_3				51		
R_4				51		
R_5				51		
R_6				51		
R_7				51		
R_8				33		
R_9				51		
C_0, C_1				0.047		μF
C_2				2.2		
C_3			1.0			
C_4			0.01			
C_5				10		
C_6				10		

Application circuits using above conditions are proviced in Figure 8.

DC AND DIGITAL INTERFACE CHARACTERISTICS

(VA = 12 V ±10%, VD = 5 V ±5%, T_a = 0 ~ 70°C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Power supply current	IA	Ordinary operation		9.0	18.0	mA
	ID			1.0	2.0	
Input leakage current *1	I_{IL}	$V_I = O_V$	-10		10	μA
	I_{IH}	$V_I = V_D$	-10		10	
Input voltage *1	V_{IL}		0		0.8	V
	V_{IH}		2.2		VD	
Output voltage *2	V_{OL}	I_{OL} = 1.6 mA	0		0.4	
	V_{OH}	I_{OH} = 400 μA	0.8 • VD		VD	

*1 LT, $\overline{CC}$, $\overline{RS1}$, $\overline{RS2}$, XD, $\overline{CD2}^{*}$, RD2, $\overline{SQ}$, TS_1(TS), $TS_2(\overline{ATE})$

*2 CLK, $\overline{CS}$, RD, $\overline{CD1}$, $\overline{CD2}^{*3}$, RD1

*3 CD2 is I/O terminal.

III

ANALOG INTERFACE CHARACTERISTICS

1. MSM6927

(VA = 12 V ±10%, VD = 5 V ±5%, T_a = 0 ~ 70°C)

Parameter		Symbol	Condition	Min	Typ	Max	Unit
Transmit Carrier Out (A0)							
Carrier frequency	Mark 1	f_M	$f_{CRYSTAL}$ = 3.579545 MHz	1290	1300	1310	Hz
	Space 0	F_S		2090	2100	2100	
Output resistance		R_{OXA}				200	Ω
Load resistance		R_{LXA}		50			kΩ
Load capacitance		C_{LXA}				100	PF
Transmit level		V_{OXA}		4	6	8	*1 dBm
Output offset voltage		V_{OSX}		$\frac{VA}{2}$ - 1	$\frac{VA}{2}$	$\frac{VA}{2}$ + 1	V
Out-of-band energy (referred to carrier level)		E_{OX}	C_1 = 0.047 μF	Refer to Figure 1			dB
Receive Carrier Input (A_{IN})							
Input resistance		R_{IRA}		100			kΩ
Receive signal level range		V_{IRA}		-48		-6	
Carrier detect level	ON	V_{CD} ON	R = 33 kΩ*2 R = 51 kΩ			-43	*1 dBm
	OFF	V_{CD} OFF		-48			
Carrier detect hysteresis		H_{YS}	V_{CD} ON − V_{CD} OFF	2			dB
Receive Filter							
Group delay distortion		D_{DL}	1100 ~ 2300 Hz		210		μS

Note: *1 0 dBm = 0.775 Vrms

*2 The resistor values are typical.

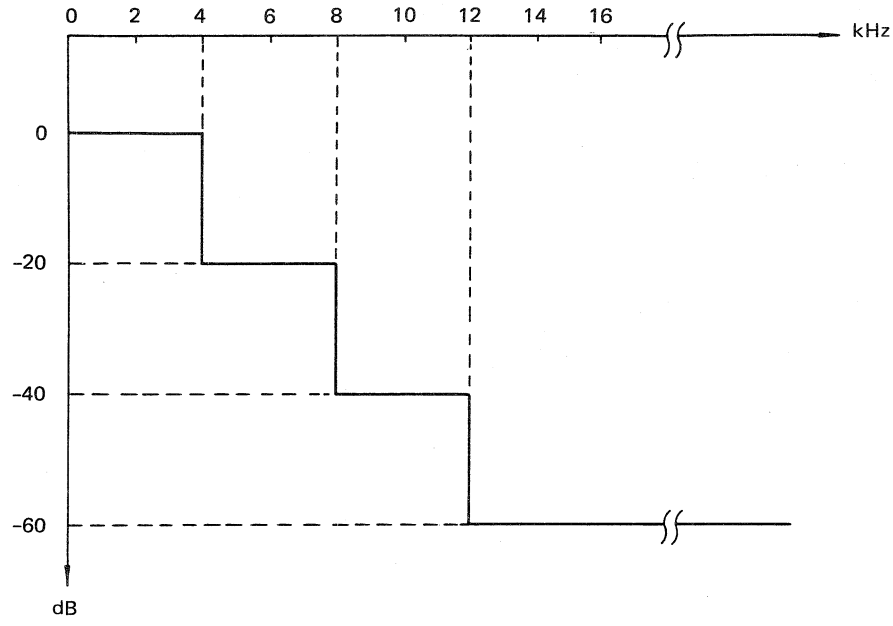


Figure 1 MSM6927 Out-of-Band Energy referred to Carrier Level (C_1 = 0.047 μF)

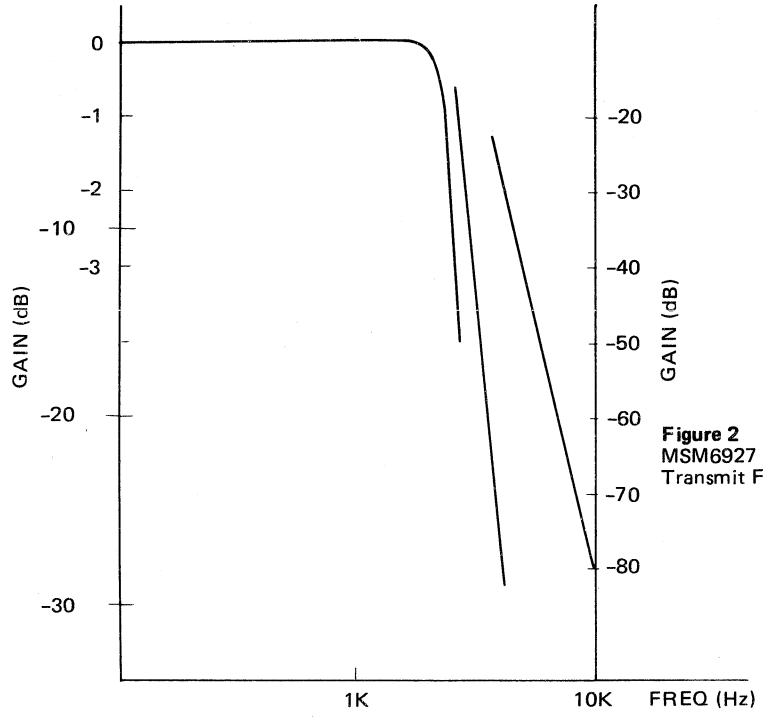


Figure 2
MSM6927
Transmit Filter

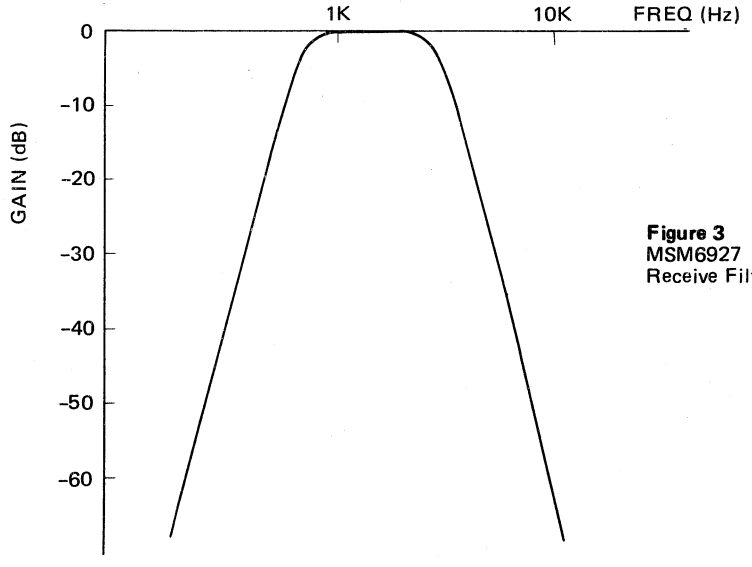


Figure 3
MSM6927
Receive Filter

2. MSM6947

($VA = 12\ V \pm 10\%$, $VD = 5\ V \pm 5\%$, $T_a = 0 \sim 70°C$)

Parameter		Symbol	Condition	Min	Typ	Max	Unit
Transmit Carrier Out (A0)							
Carrier frequency	Mark 1	f_M	$f_{CRYSTAL} = 3.579545$ MHz	1190	1200	1210	Hz
	Space 0	F_S		2190	2200	2200	
Answer tone frequency		f_A	$\overline{ATE}$ = "0"	2019	2025	2031	
Output resistance		R_{OXA}				200	Ω
Load resistance		R_{LXA}		50			kΩ
Load capacitance		C_{LXA}				100	PF
Transmit level		V_{OXA}		4	6	8	*1 dBm
Output offset voltage		V_{OSX}		$\frac{VA}{2}-1$	$\frac{VA}{2}$	$\frac{VA}{2}+1$	V
Out-of-band energy (referred to carrier level)		E_{OX}	$C_1 = 0.047\ \mu F$	Refer to Figure 4			dB
Receive Carrier Input (A_{IN})							
Input resistance		R_{IRA}		100			kΩ
Receive signal level range		V_{IRA}		-48		-6	*1 dBm
Carrier detect level	ON	V_{CD} ON	$R_8 = 33\ k\Omega$*2, $R_9 = 51\ k\Omega$			-43	
	OFF	V_{CD} OFF		-48			
Carrier detect hysteresis		H_{YS}	V_{CD} ON − V_{CD} OFF	0.5			dB
Receive Filter							
Group delay distortion		D_{DL}	1100 ~ 2300 Hz		210		μS

Note: *1 0 dBm = 0.775 Vrms
*2 The resistor values are typical.

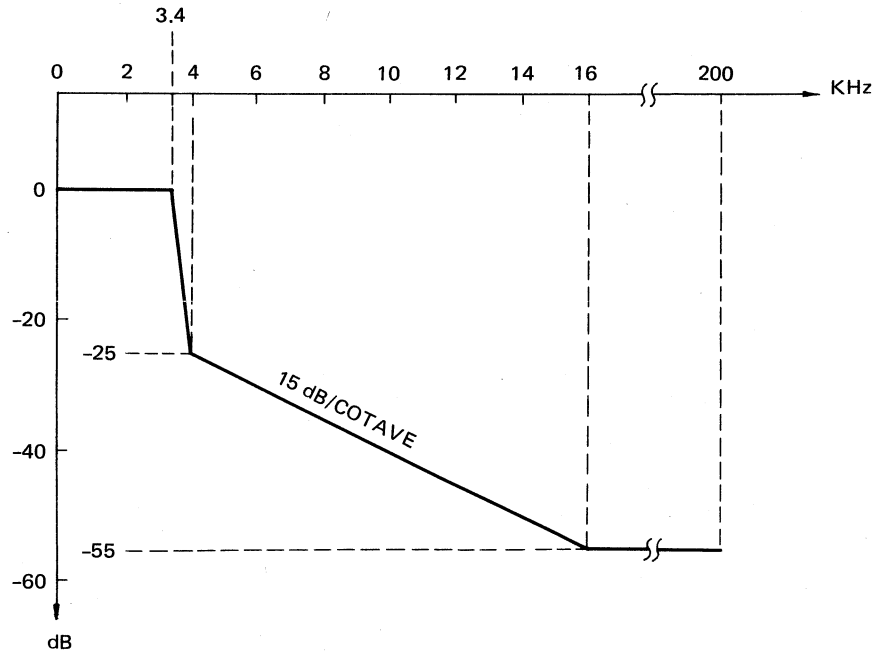


Figure 4 MSM6947 Out-of-Band Energy referred to Carrier Level (C_1 = 0.047 μF)

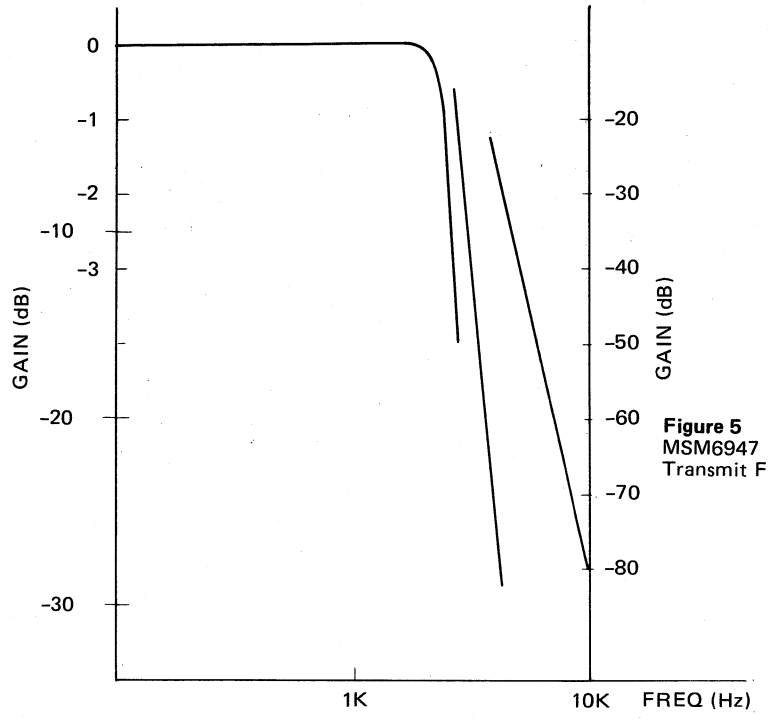


Figure 5
MSM6947
Transmit Filter

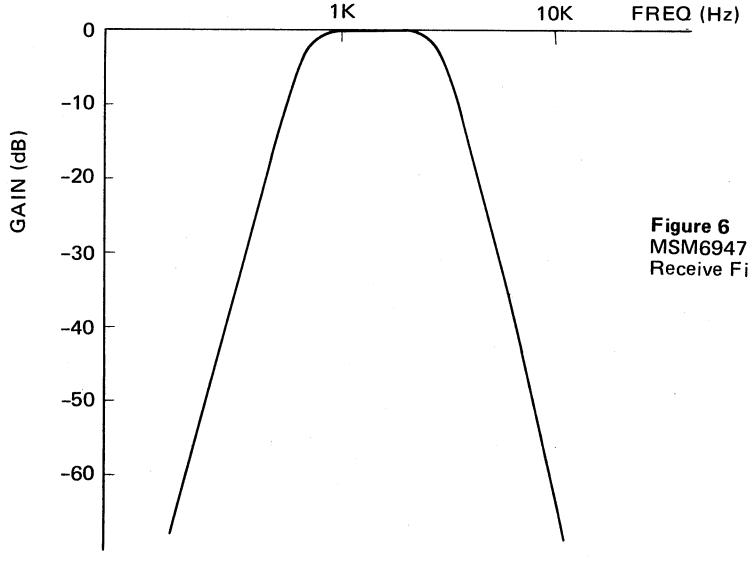


Figure 6
MSM6947
Receive Filter

III

DEMODULATED BIT CHARACTERISTICS

(VA = 12 V ±10%, VD = 5 V ±5%, T_a = 0 ~ 70°C)

Parameter	Symbol	Condition			Min	Typ	Max	Unit
Peak intersymbol distortion	ID	Back-to-back over input signal range –6 to –40 dBm. 511-bit test pattern.				9		%
Bit error rate	BER	Back-to-back with 0.3 ~ 3.4 kHz flat noise. Receive signal level –25 dBm. 511-bit test pattern	S/N (dB)	8		10^{-3}		
				11		10^{-5}		

TIMING CHARACTERISTICS

1. MSM6927

(VA = 12 V ±10%, VD = 5V ±5%, T_a = 0 ~ 70°C)

Parameter	Symbol	Condition	TS2	TS1	Min	Typ	Max	Unit
RS/CS delay time	T_{RC} ON	$\overline{RS1}$ = "0" → $\overline{CS}$ = "0"	0	0	195	200	205	ms
			0	1	25	30	35	
			1	0	65	70	75	
			1	1	External delay timer			
	T_{RC} OFF	$\overline{RS1}$ = "1" → $\overline{CS}$ = "1"	*	*	0		0.5	
CD/ON delay time	T_{CD} ON		0	0	10		25	
			0	1	10		25	
			1	0	10		25	
			1	1	External delay timer			
CD/OFF delay time	T_{CD} OFF		0	0	5		15	
			0	1	5		15	
			1	0	5		15	
			1	1	External delay timer			
Soft Turn-OFF time	T_{ST}		*	*		10		
Receive Data Squelch Delay Time	TSQ	$\overline{SQ}$ = "0"	0	0	145	150	155	
		$\overline{RS1}$ = "1" → RD = "1" Hold	0	1	145	150	155	
			1	0	35	40	45	
			1	1	External delay timer			

Refer to Figure 7.

Note: * ..... **Irrespective of 1/0 condition**

III

2. MSM6947

(VA = 12 V ±10%, VD = 5 V ±5%, T_a = 0 ~ 70°C)

Parameter	Symbol	Condition	TS	Min	Typ	Max	Unit
RS/CS Delay Time	T_{RCON}	$\overline{RS1}$ = "0" → $\overline{CS}$ = "0"	0	175	180	185	ms
			1	External Delay Timer			
	T_{RCOFF}	$\overline{RS1}$ = "1" → $\overline{CS}$ = "1"	*	0		0.5	
CD/ON Delay Time	T_{CDON}		0	15		35	
			1	External Delay Timer			
CD/OFF Delay Time	T_{CDOFF}		0	10		20	
			1	External Delay Timer			
Soft Turn OFF Time	T_{ST}		*		10		
Receive Data Squelch Delay Time	T_{SQ}	$\overline{SQ}$ = "0"	0		156		
		$\overline{RS1}$ = "1" → $\overline{RD}$ = "1" Hold	1	External Delay Timer			

Refer to Figure 7.
Note: * . . . Irrespective of 1/0 condition

TIMING DIAGRAM

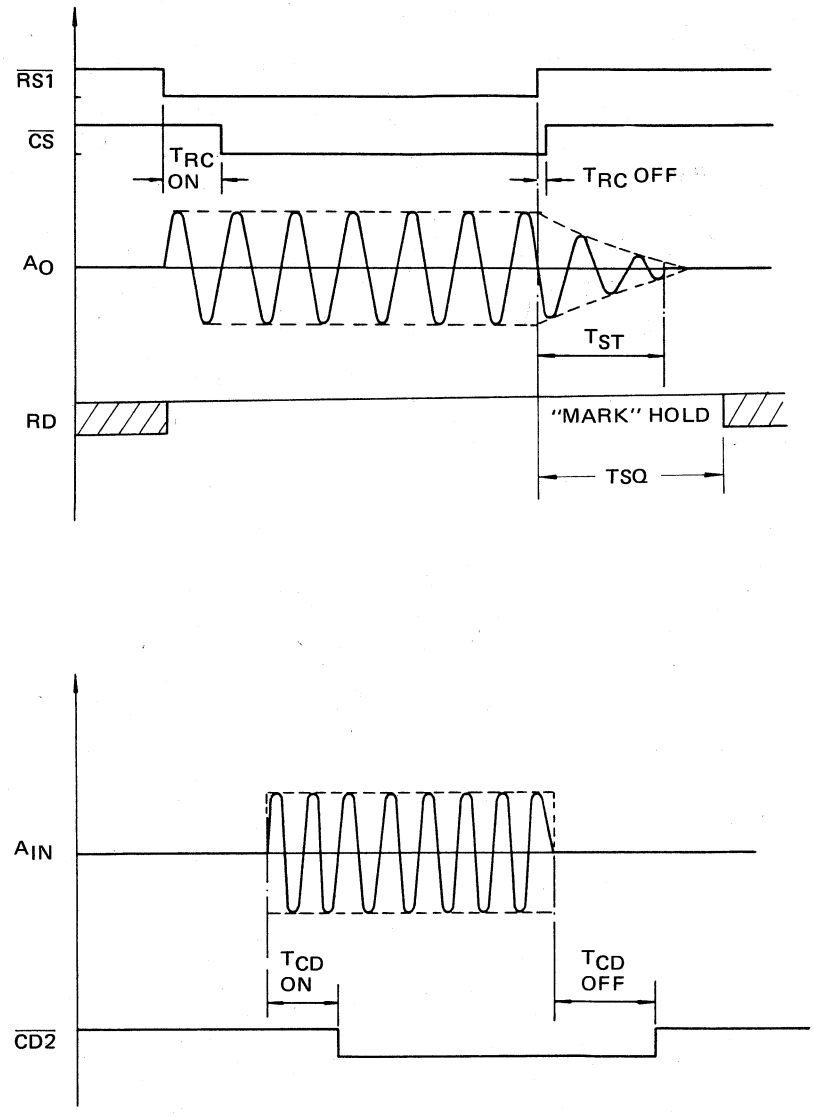


Figure 7 MSM6927/MSM6947 Timing Diagram

PIN DESCRIPTIONS

Name	Pin No. RS	Pin No. GS-K	I/O	Function
POWER				
DG	15	19		Ground reference of V_D (digital ground)
AG	19	23		Ground reference of V_A (analog ground)
V_A	24	33		Supply voltage (+12 V nominal)
V_D	26	35		Supply voltage (+5 V nominal)
CLOCKS				
X1	1	41		Master clock timing is provided by either a series resonant crystal (3.579545 MHz ±0.01%) connected across X1 and X2, or by an external TTL/CMOS clock driving X2 with AC coupling where X1 is left unconnected. See Figure 10.
X2	2	42		
CLK	3	43	O	873.9 Hz clock output. This clock is used to implement external delay circuits etc.
CONTROL				
LT	4	44	I	Digital loop back. During digital "High", any data sent on the X_D pin will appear on the RD pin, and any data sent on the $\overline{RS1}$ pin will immediately appear on the $\overline{CS}$ pin. Any data demodulated from the received carrier on the A_{IN} pin will be the modulated data to implement the transmitted carrier. In this case, sending the transmitted carrier to the phone line depends on the $\overline{CC}$, but never on $\overline{RS1}$.
$\overline{CC}$	5	2	I	During digital loopback, the data on this pin becomes a control signal for sending the transmitted carrier to the phone line in place of $\overline{RS1}$.
$\overline{RS2}$	8	8	I	When an external circuit gives the RS/CS delay time which is not within the device as required, this pin should be connected to the external circuit output. See Figure 11-1 or Figure 11-2 for MSM6927, MSM6947 respectively.

Name	Pin No. RS	Pin No. GS-K	I/O	Function
$\overline{CD1}$	11	12	O	The fast carrier detection output. This pin is internally connected to the input of the built-in carrier detect delay circuit. When an external delay circuit provides the delay time which is not within the device as required, the $\overline{CD1}$ should be connected to the external circuit input. See Figure 11-1 or Figure 11-2 for MSM6927, MSM6947 respectively.
$\overline{CD2}$	12	13	I/O	When an external circuit gives the carrier detect delay time which is not within the device as required, this pin becomes the input pin for the external circuit output signal. In other cases (when using the delay time within the device, the data on the TS_1 (TS) or TS_2 is not digital "High"), this pin becomes the Carrier-Detect signal output.
RD1	13	14	O	The RD1 data is demodulated data from the received carrier and the RD2 is the input of the following logic circuits referred to in Figure 12 and Figure 14. Usually, the RD1 data is input directly to RD2. In some cases, as input data to RD2, the data that is controlled by NCU (Network-Control-Unit) etc. may be required in stead of the RD1 data.
RD2	14	16	I	
CDR1	16	20	O	These two pins are the output (CRD1) and inverting input (CDR2) of the buffer operational amplifier of which noninverting input is connected to the built-in voltage reference, stabilized to variations in the supply voltage and temperature. See Figure 13. An adequate carrier-detect level can be set by selecting the ratio of R_8 and R_9. Therefore, the loss in the received carrier level by phone-line transformer can be compensated by adjusting the ratio of R_8 and R_9. $R_8 + R_9$ should be greater than 50 kΩ.
CDR2	17	21	I	
$\overline{SQ}$	22	31	I	When data rate is 1200 BPS and at half duplex operation on two-wire facilities, the delay function called as receiver-squelch is required. In case of four wire facilities, this function is not required usually. When digital "High" input to the $\overline{SQ}$ pin, this function can be omitted.
FT	23	32	I	This pin may be used for device tests only. During digital "High", the A_O pin will be connected to receiving filter output instead of transmitting filter output.

Both MSM6927RS (or GS-K) and MSM6947RS (or GS-K) have 28 (or 44) pins. The pin descriptions for these 28 (or 44) pins are same except those for No. 27 (or No. 36) pin and No. 28 (or No. 38). The pin descriptions for No. 27 (or No. 36) pin and No. 28 (or No. 38) pin are described as follows.

MSM6927

Name	Pin No.		I/O	Function
	RS	GS-K		
TS1	27	36	I	RS/CS delay and carrier detect delay options referred to in the chapter about timing characteristics are selected by TS1 and TS2 inputs. The receiver-squelch delay will be set at the same time. Be careful that each delay can not be individually selected. If the other delay time unprovided within the device as option is required, input digital "High" to the TS1 and TS2 pin and implement the external delay circuits to obtain the desired delay characteristics. In this case, the CD2 pin becomes not only the input for the external circuit output signal, but also the Carrier Detect output. See Figure 11-1.
TS2	28	38	I	

MSM6947

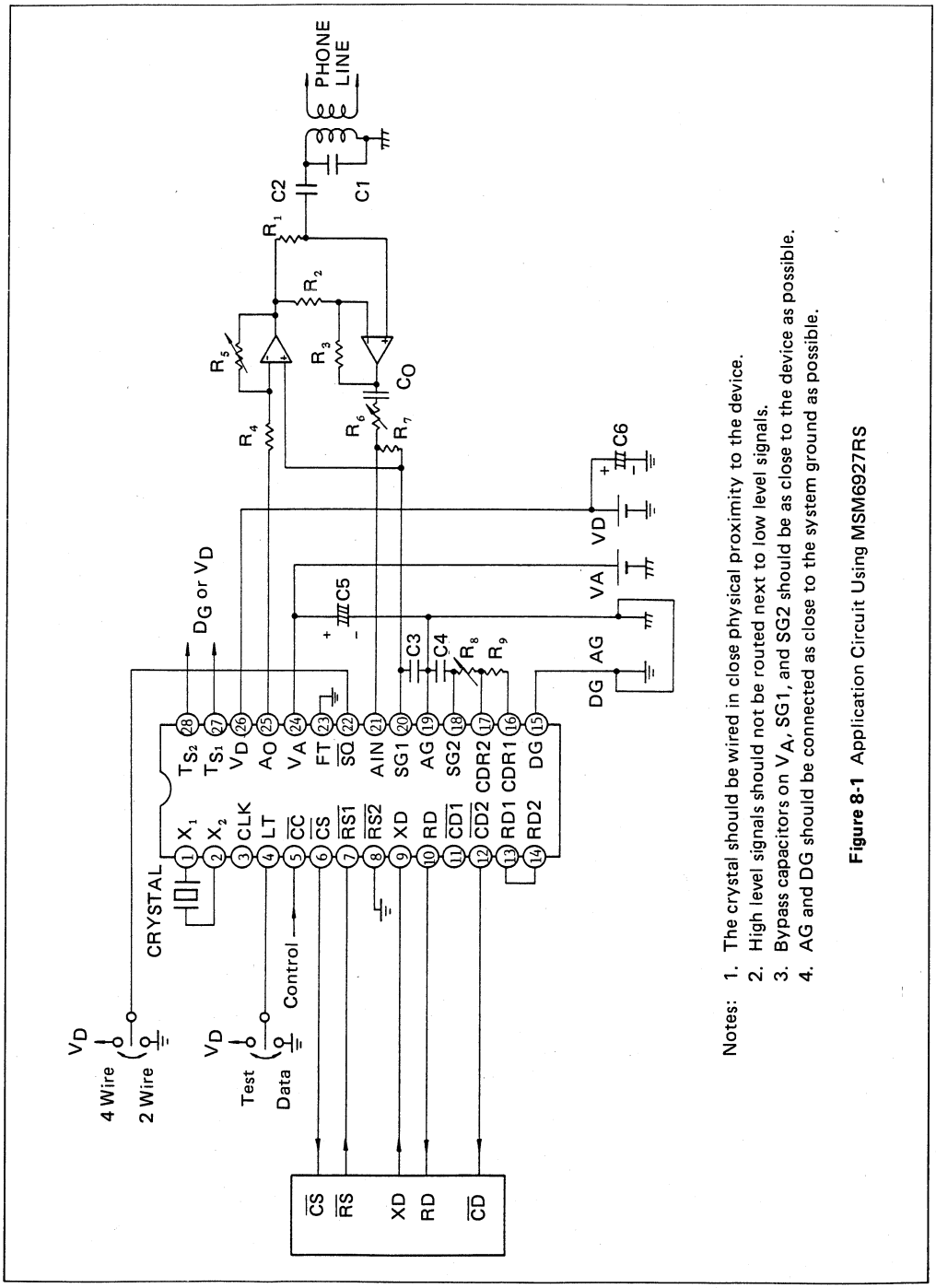
Name	Pin No.		I/O	Function
	RS	GS-K		
TS	27	36	I	When digital "Low" input to the TS pin, built-in RS/CS, carrier detect and receiver-squelch delay are provided. If the other delay time is required, by inputting digital "High" to this pin and implementing the external delay circuits, the desired delay can be realized. In this case, the $\overline{CD2}$ pin becomes not only the input for the external circuit output signal, but also the Carrier Detect output. See Figure 11-2.
$\overline{ATE}$	28	38	I	Answer Tone Enable input. When digital "Low" input to this pin and the $\overline{RS1}$ pin is in digital "Low" level, Answer Tone (~ 2025 Hz) is sent over the phone line via the A_O pin.

INPUT/OUTPUT

$\overline{CS}$	6	3	O	Clear-to-Send signal output. The digital "High" level indicates the "OFF" state and digital "Low" indicates the "ON" state. This output goes "Low" at the end of a delay (RS/CS delay) initiated when $\overline{RS1}$ (Request-to-Send) goes "Low".
$\overline{RS1}$	7	4	I	Request-to-Send signal input. The digital "High" level indicates the "OFF" state. The digital "Low" level indicates the "ON" state and instructs the modem to enter the transmit mode. This input must remain "Low" for the duration of data transmission. "High" turns the transmitter off.
XD	9	9	I	This is digital data to be modulated and transmitted via A_O. Digital "High" will be transmitted as "Mark". Digital "Low" will be transmitted as "Space". No signal appears at A_O unless $\overline{RS1}$ is "Low".
RD	10	10	O	Digital data demodulated from A_{IN} is serially available at this output. Digital "High" indicates "Mark" and digital "Low" indicates "Space". For example, under the following conditions this output is forced to be "Mark" state because the data may be invalid. • When $\overline{CD2}$ (Carrier-detect) is in the "OFF" state. • When $\overline{SO}$ is in digital "Low" (two-wire facilities) and $\overline{RS1}$ is in the "ON" state. • During the receive data squelch delay at half duplex operation on two wire facilities.
SG2	18	22	O	The SG1 and SG2 are built-in analog signal grounds. SG2 is used only for Carrier-Detect function. The DC voltage of SG1 is approximately 6V, so the analog line interface must be implemented by AC coupling. See Figure 9. To make these impedance lower and ensure the device performance, it is necessary to put bypass capacitors on SG1 and SG2 in close physical proximity to the device.
SG1	20	24	O	
A_{IN}	21	26	I	This is the input pin for the analog signal from the phone line. The modem extracts the information in this modulated carrier and converts it into a serial data stream for presentation at RD output.
A_O	25	34	O	This analog output is the modulated carrier to be conditioned and sent over the phone line.

APPLICATION CIRCUIT

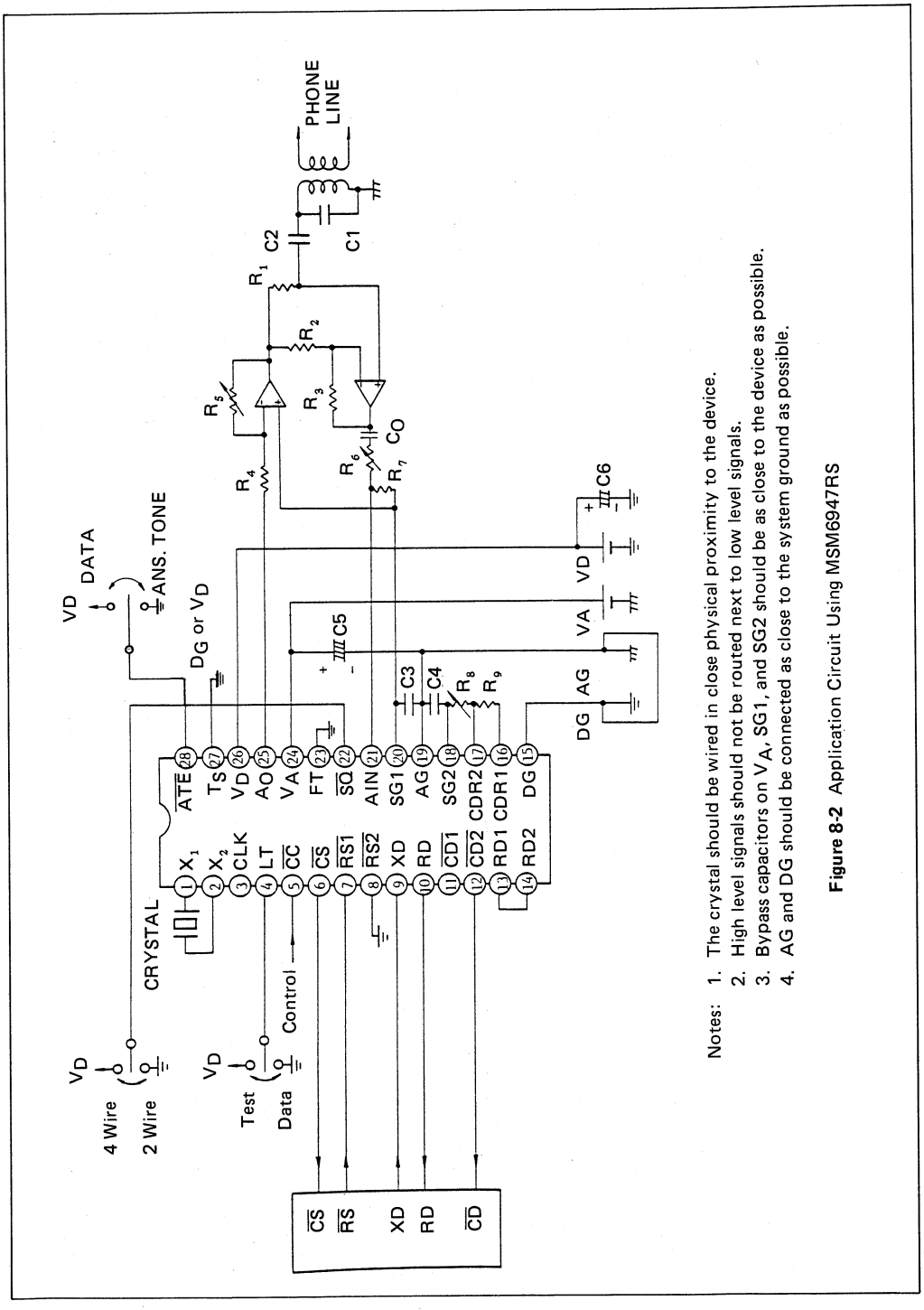
1. MSM6927RS



Notes:
1. The crystal should be wired in close physical proximity to the device.
2. High level signals should not be routed next to low level signals.
3. Bypass capacitors on V_A, SG1, and SG2 should be as close to the device as possible.
4. AG and DG should be connected as close to the system ground as possible.

Figure 8-1 Application Circuit Using MSM6927RS

2. MSM6947RS



Notes:
1. The crystal should be wired in close physical proximity to the device.
2. High level signals should not be routed next to low level signals.
3. Bypass capacitors on V_A, SG1, and SG2 should be as close to the device as possible.
4. AG and DG should be connected as close to the system ground as possible.

Figure 8-2 Application Circuit Using MSM6947RS

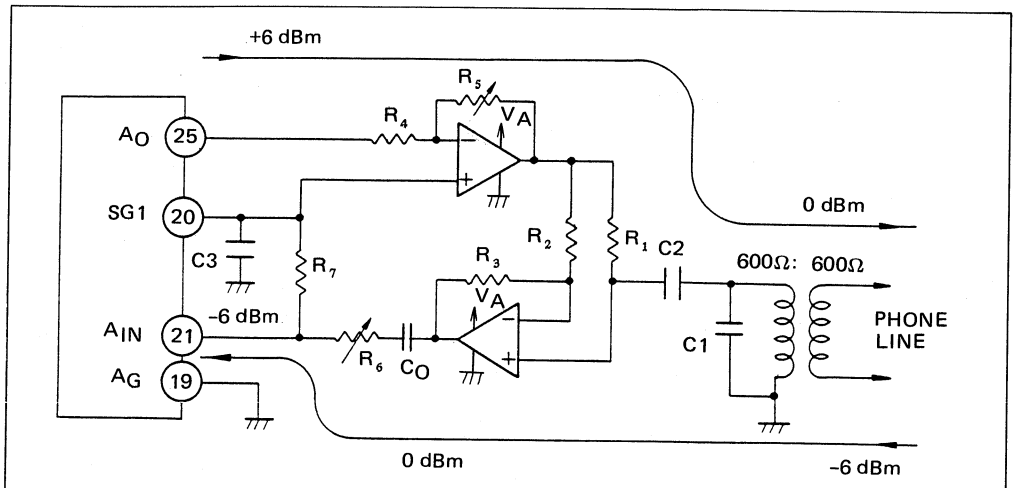
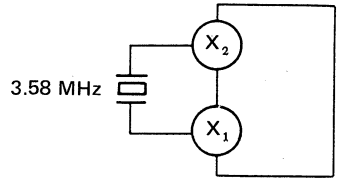


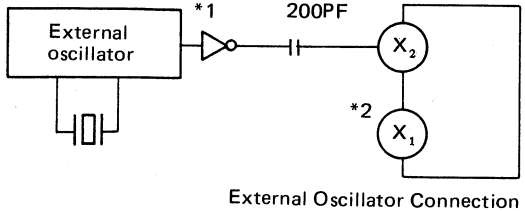
Figure 9 MSM6927RS/MSM6947RS Application

C_0, C_1	0.047 μF	R_2	51 kΩ	R_6	(51 kΩ)	Receive signal level
C_2	2.2 μF	R_3	51 kΩ	R_7	51 kΩ	
C_3	1 μF	R_4	51 kΩ	R_8	(33 kΩ)	Carrier detect level
R_1	600 Ω	R_5	(51 kΩ) Transmit signal level	R_9	51 kΩ	

Note: The signal level on the A_{IN} pin should not exceed -6 dBm.



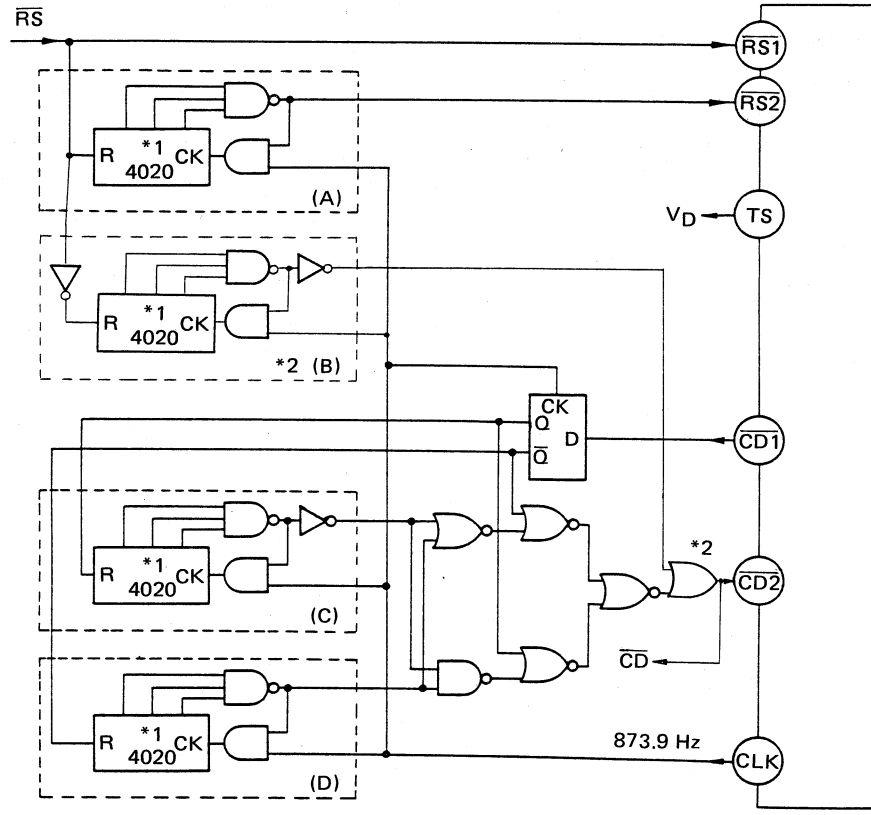
Crystal Oscillator Connection



External Oscillator Connection

*1 TTL or Hi-Speed CMOS GATE
*2 Left unconnected

Figure 10



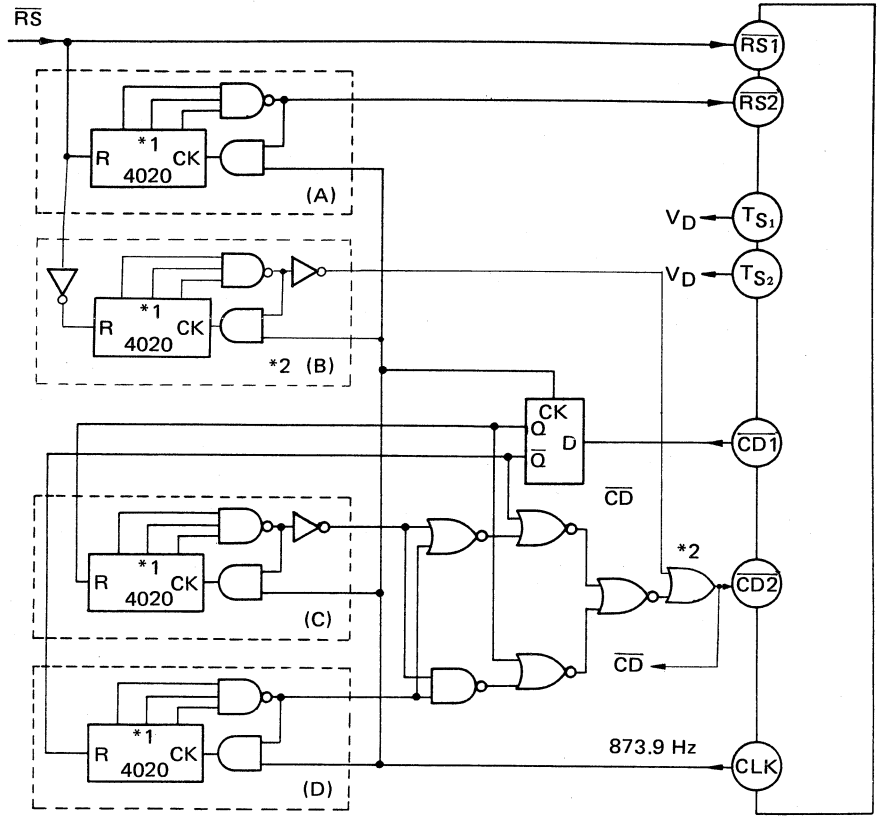
(A) RS/CS delay, (B) Receiver-squelch delay, (C) CD/ON delay, (D) CD/OFF delay

Note: Supply voltage equals V_D for all gates.

*1: The desired delay can be realized by selecting the appropriate bits from 4020's outputs. The number of the bits is not always 3. Each delay can be set differently from built-in delays.

*2: In the case that the Receiver-dquelch delay is unnecessary, circuit (B) and this OR gate should be omitted and the output of the NOR gate should be connected to $\overline{DC2}$ directly.

Figure 11-1 MSM6927 External Delays Connection



(A) RS/CS delay, (B) Receiver-squelch delay, (C) CD/ON delay, (D) CD/OFF delay

Note: Supply voltage equals V_D for all gates.

*1: The desired delay can be realized by selecting the appropriate bits from 4020's outputs. The number of the bits is not always 3. Each delay can be set differently from built-in delays.

*2: In the case that the Receiver-dquelch delay is unnecessary, circuit (B) and this OR gate should be omitted and the output of the NOR gate should be connected to $\overline{DC2}$ directly.

Figure 11-2 MSM6947 External Delays Connection

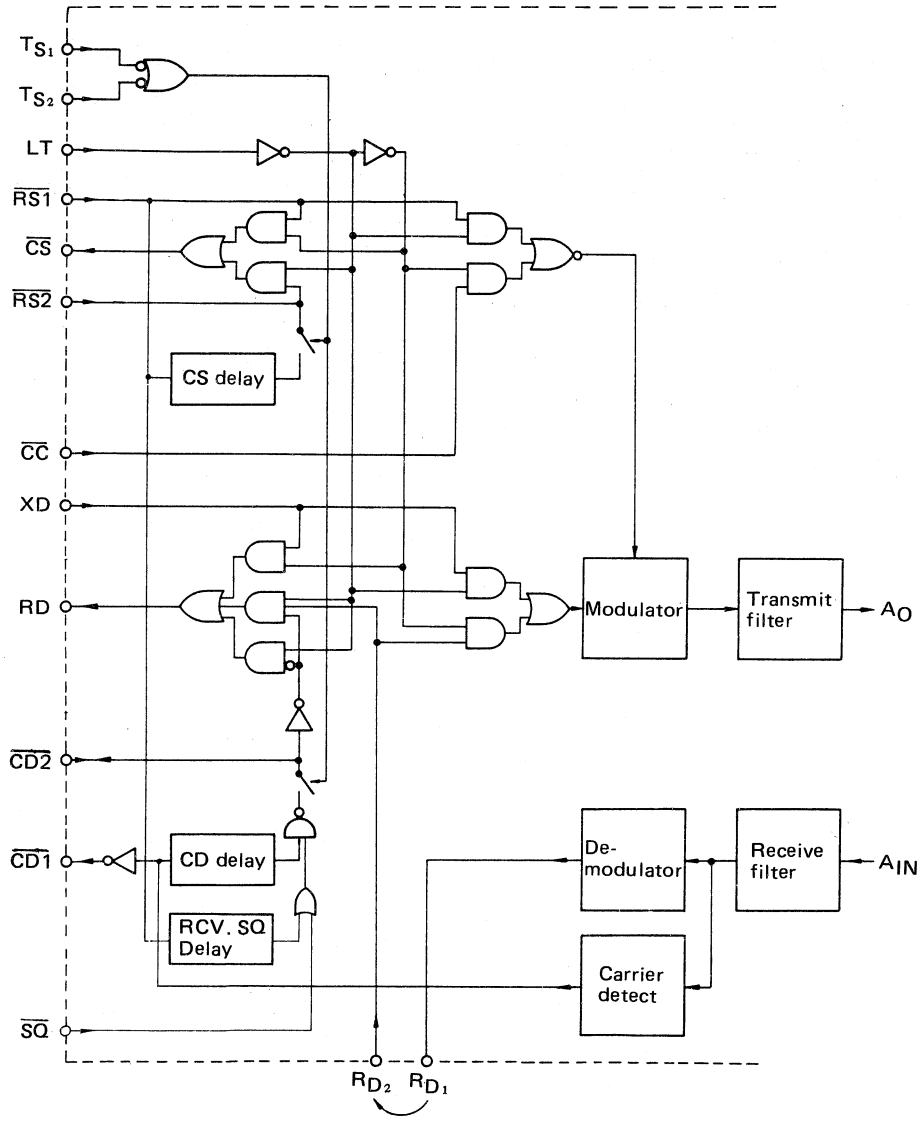


Figure 12-1 MSM6927 Equivalent Logic Interface of the Integrated Modem

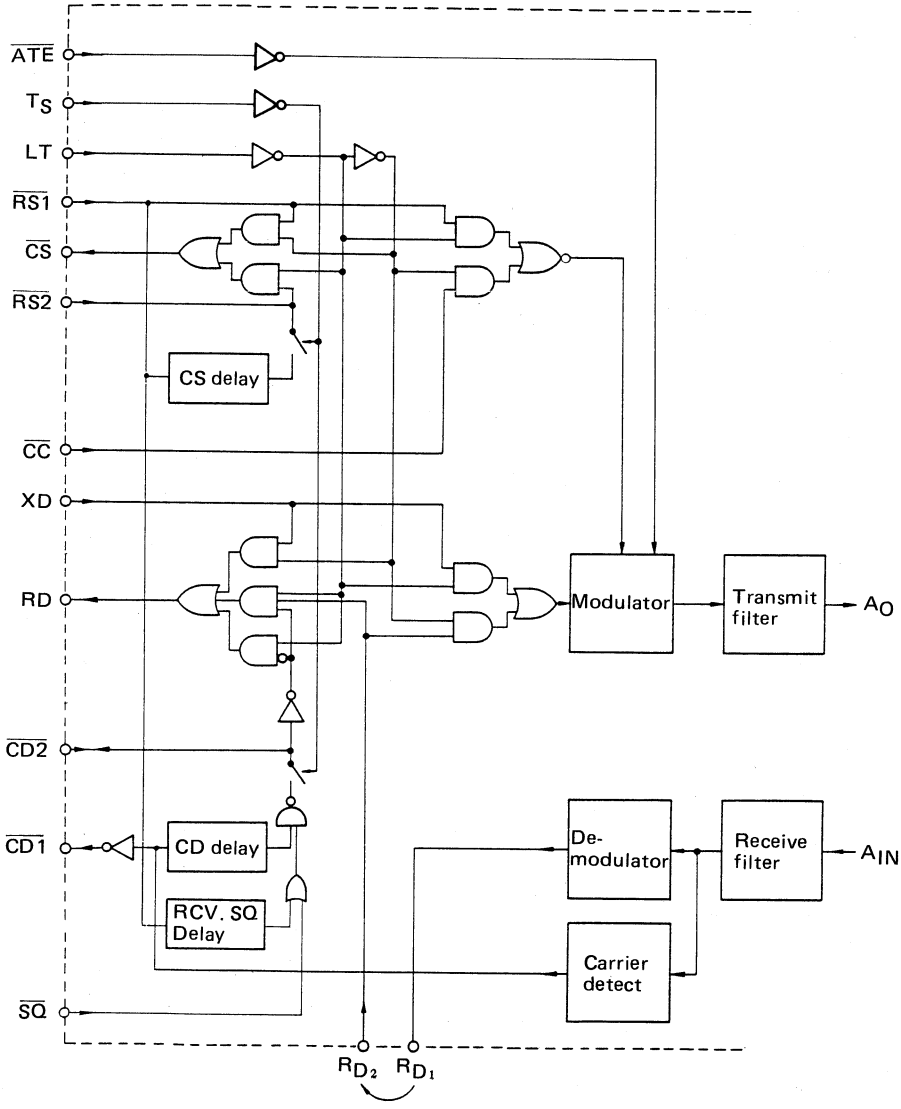


Figure 12-2 MSM6947 Equivalent Logic Interface of the Integrated Modem

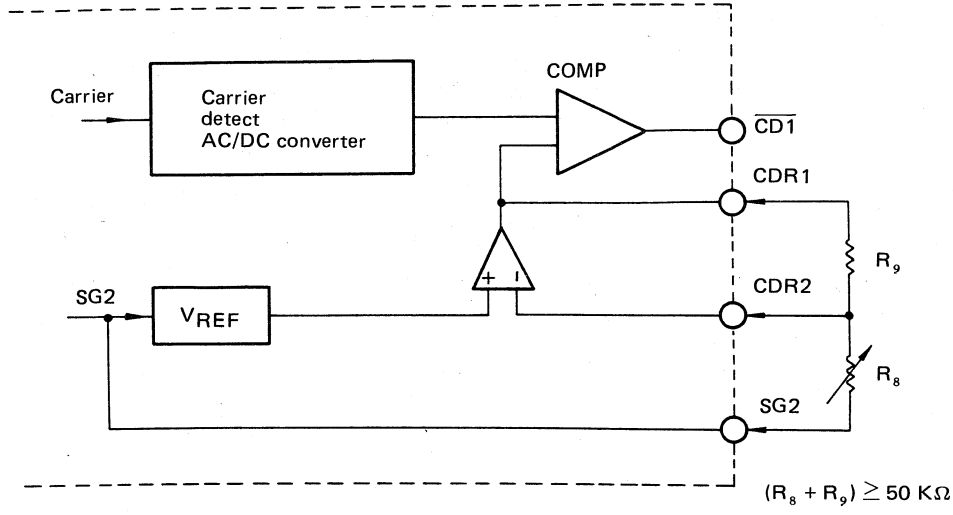


Figure 13 External Resistor Connection for the Setting of Carrier Detect Level

III

MSM6948

SINGLE CHIP MSK MODEM

GENERAL DESCRIPTION

The MSM6948 is a single chip MSK (Minimum Shift Keying) modem which is fabricated by OKI's low power consumption CMOS silicon gate technology.

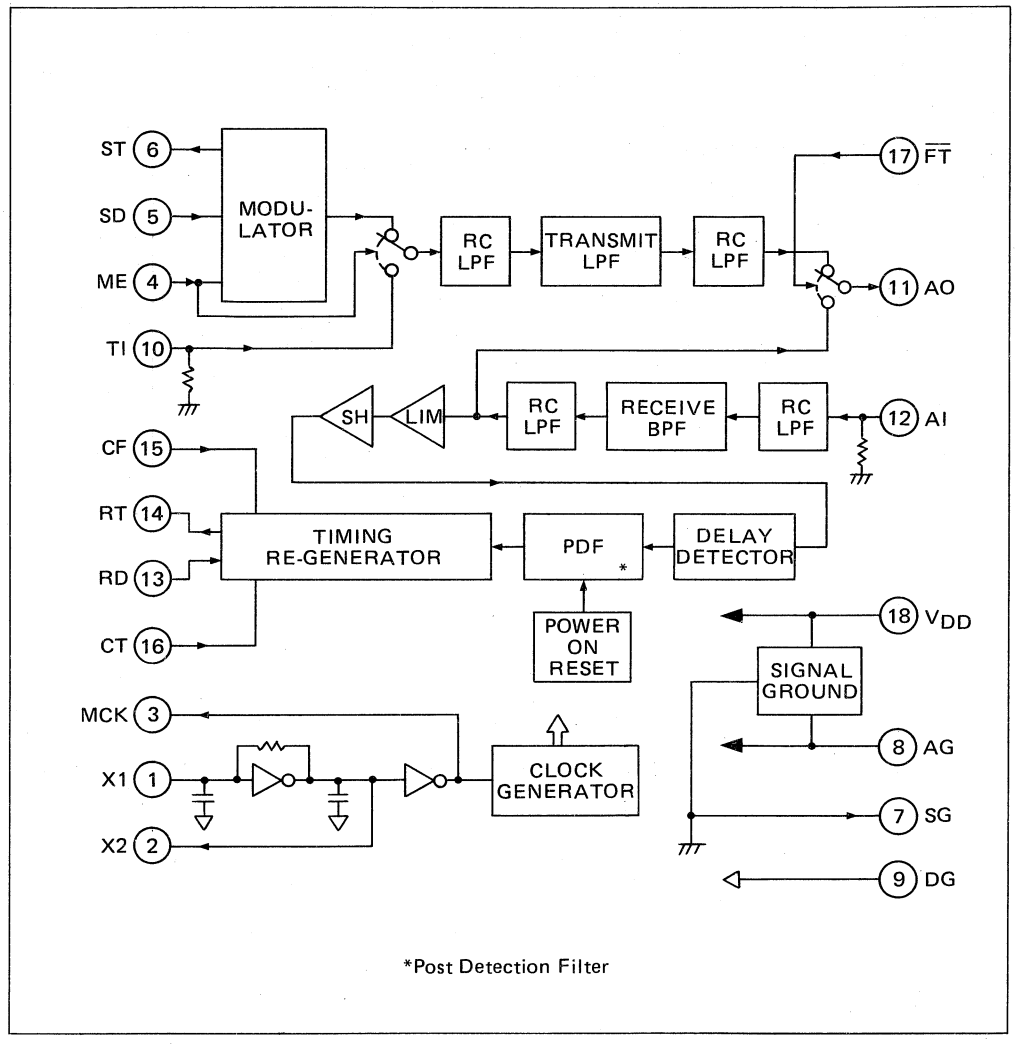
The modulator receives the data to be transmitted (SD) synchronized with the transmit timing clock (ST) generated by the on-chip clock generator. The signal, which is modulated by MSK method, is output.

The demodulator converts the received MSK signal to the received data (RD) by means of delay detection technique after limiting the band of the received MSK signal. This signal is input to the digital PLL and re-generated timing clock is output from the demodulator, synchronized with the RD.

FEATURES

- On-chip SCF (Switched Capacitor Filter)
- The transmit filter can be used as voice splutter filter.
- The receive timing re-generator has two different lock-in time performance options to be chosen from.
- On-chip oscillation circuit.
- Small numbers of external components for easy application.
- Wide application-wireless data equipment, MCA system.
- +5 V signal power supply.
- Low power consumption CMOS.
- 18 pin plastic DIP package.

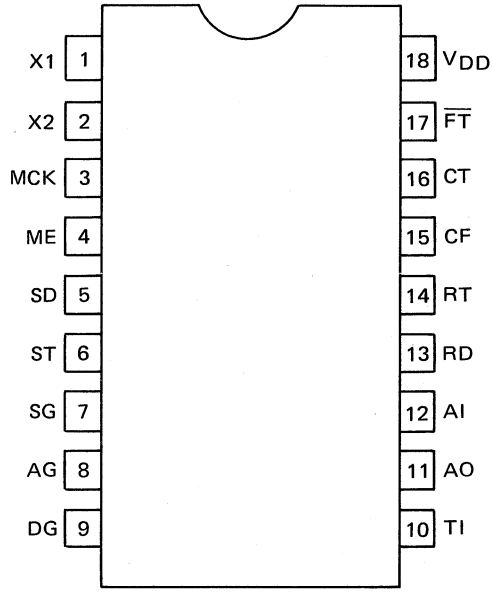
BLOCK DIAGRAM



PIN CONFIGURATION

(Top View)

18 Lead Plastic Package



III

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{DD}	Ta = 25°C Referred to AG or DG	-0.3 ~ 7	V
Analog Input Voltage *1	V_{IA}		-0.3 ~ V_{DD} + 3	
Digital Input Voltage *2	V_{ID}		-0.3 ~ V_{DD} + 0.3	
Operating Temperature	Top	—	-25 ~ 70	°C
Storage Temperature	Tstg	—	-55 ~ 150	

*1 TI, AI
*2 ME, SD, CF, CT, $\overline{FT}$

Recommended Operating Conditions

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Power Supply Voltage	V_{DD}	Referred to AG or DG	4.75	5	5.25	V
	AG, DG	–	–	0	–	
Operating Temperature	Top	–	-25	25	70	°C
Crystal Resonant	$f_{X'TAL}$	–	3.6860	3.6864	3.6868	MHz
Data rate	Ts	–	–	1200	–	bit/s
C_1	–	–	–	2.2	–	μF
C_2	–	–	–	0.1	–	
C_3	–	–	–	0.047	–	
C_4	–	Depend on Load Impedance for Ao Output				
C_5	–	–	–	0.047	–	

DC and Digital Interface Characteristics

V_{DD} = 5 V ±5%, Ta = -25 ~ 70°C

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Power Supply Current	I_{DD}	Normal Operating Condition	–	3	6	mA
Oscilating Frequency	f_{MCK}	$f_{X'TAL}$ = 3.6864 MHz ±0.01%	3.6857	3.6864	3.6871	MHz
Input Leakage Current *1	I_{IL}	$V_{IN} = O_V$	-10	–	10	μA
	I_{IH}	$V_{IN} = V_{DD}$	-10	–	10	
Input Voltage *1	V_{IL}	–	0	–	0.8	V
	V_{IH}	–	2.2	–	V_{DD}	
Output Voltage *2	V_{OL1}	I_{OL} = 1.6 mA	0	–	0.4	
	V_{OH1}	I_{OH} = 400 μA	0.8 V_{DD}	–	V_{DD}	
Output Voltage *3	V_{OL2}	$R_L > 50\ k\Omega$	0	–	0.4	
	V_{OH2}	$C_L < 20\ pF$	0.6 V_{DD}	–	V_{DD}	

*1 ME, SD, CF, CT, $\overline{FT}$
*2 ST, RD, RT
*3 MCK

III

Analog Interface Characteristics (V_{DD} = 5V ±5%, Ta = −25 ~ 70°C)

Transmit signal output (A_O)

Parameter	Symbol	Condition		Min	Typ	Max	Unit
Carrier frequency	f_M	SD = "1"	$\overline{FT}$ = "1" ME = "1"	1199	1200	1201	Hz
	f_S	SD = "0"		1799	1800	1801	
Carrier level	V_{OX}	$R_L \geq$ 100kΩ	$\overline{FT}$ = "1" ME = "1"	−2 / 1.74	0 / 2.19	+2 / 2.76	dBm / Vp-p
Output voltage swing	V_{OPP}	$C_L \leq$ 40PF	$\overline{FT}$ = "1" ME = "0"	2.2	3	—	Vp-p
Output resistance	R_{OX}	$f_{AO} \leq$ 4 kHz		—	—	1	kΩ
Load resistance	R_{LX}	—		100	—	—	
Load capacitance	C_{LX}	—		—	—	40	PF
Output DC voltage	V_{OSX}	—		$\frac{1}{2}V_{DD}-0.1$	$\frac{1}{2}V_{DD}$	$\frac{1}{2}V_{DD}+0.1$	V

Note: 0 dBm = 0.775 Vrms

Voice signal input (TI)

Voltage gain	G_T	V_{AO}/V_{TI}	$\overline{FT}$ = "1" ME = "0"	−2	0	+2	dB
Input signal level	V_{TI}	—		—	—	0	dBm
Input resistance	R_{TI}	$f_{TI} \leq$ 4kHz		50	—	—	kΩ

Built-in Signal Ground (SG)

DC Voltage	V_{SG}	Without DC Load	$\frac{V_{DD}}{2} - 0.1$	$\frac{V_{DD}}{2}$	$\frac{V_{DD}}{2} + 0.1$	V

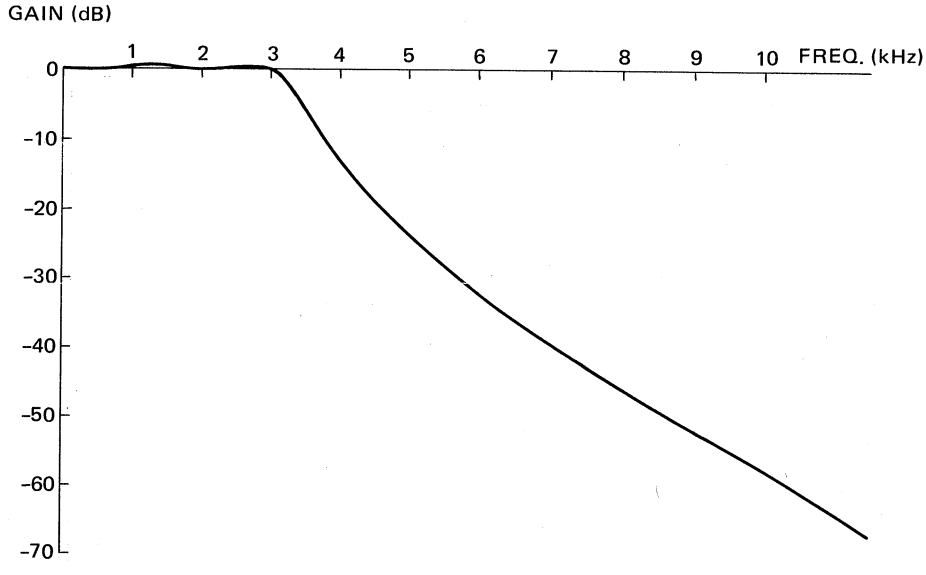
Receive Signal Input (AI) and Demodulator

Input Resistance	R_{IR}	$f_{AI} \leq 4$ kHz		50	—	—	kΩ
Receive Signal Level	V_{IR}	—		-30	—	0	dBm
Bit Error Rate	BER	S/N (at AI)	8 dB	—	4×10^{-3}	—	N/N
			12 dB	—	3×10^{-5}	—	

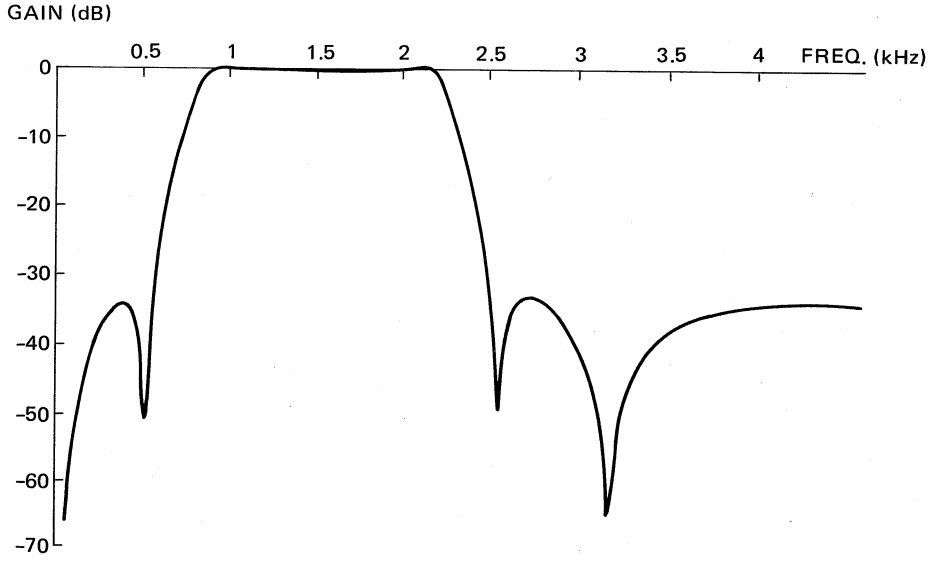
Re-generated Receive Data Timing Clock Output (RT)

Data Bit Number For PLL's Lock-in	N_{PLL1}	CF = "1"	CT = "0"	$\lvert\Delta\theta\rvert < 5°$	—	—	31	Bit
	N_{PLL2}		CT = "1"		—	—	65	

BUILT-IN FILTER FREQUENCY CHARACTERISTICS

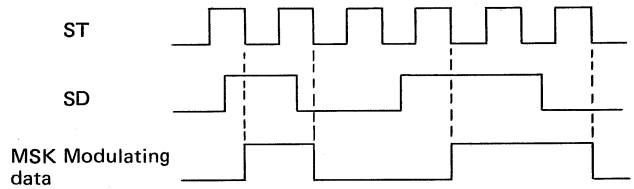


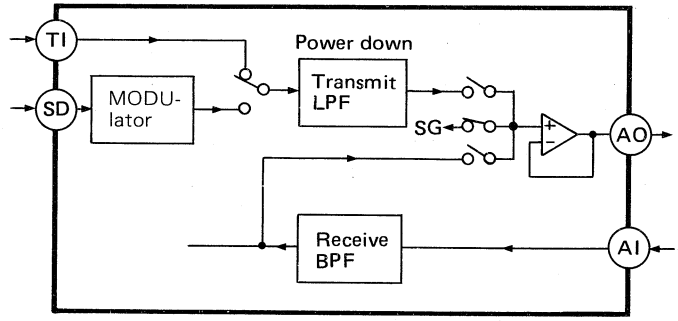
Transmit Low-pass Filter

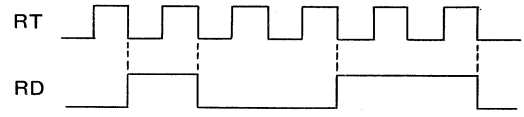


Receive Band-pass Filter

PIN DESCRIPTION

Pin Name	Pin No.	Function
X1	1	Crystal connection pins. A 3.6864 MHz crystal shall be connected. When an external clock is applied for MSM6948's oscillation source, it has to be input to X2. In this case, X2 has to be AC-compled by the capacitor of 200 pF. X1 shall be left open.
X2	2	
MCK	3	3.6864 MHz ±0.02% clock output. This can be used for other devices under limited load conditions.
ME	4	When digital "1" is put on this pin, MSK modulator output is connected to the input of transmit LPF. When digital "0" is put on, the input of transmit LPF is connected to TI that is voice signal input. The data put on ME terminal is synchronized with the negative edge of ST and input to internal logic as a control data. The positive edge of this synchronized data resets MSK modulator.
SD	5	Transmit data input terminal. The data on this pin is synchronized with the negative edge of ST and input to MSK modulator as a actual transmit data. ST is synchronizing signal used for ME and SD. This is made from master clock and is usually 1200 Hz.
ST	6	
SG	7	Built-in analog signal ground. The DC voltage is approximately half of VDD, so the analog signal interfaces of AI, AO and TI with peripheral circuits must be implemented by AC-coupling. To make this voltage source impedance lower and ensure the device performance, it is necessary to put a bypass capacitor on SG in close physical proximity to the device.
AG	8	Analog ground. This pin should be common with DG at the system ground point as close as possible.
DG	9	Digital ground. This pin should be common with AG at the system ground point as close as possible.
TI	10	Voice signal input terminal. The signal input to this pin can be sent out to AO through the transmit LPF, the characteristics of which, gives the splutter filter for voice band signal. When this function is used, digital "0" must be input to ME. TI is biased internally to SG with about 100 kΩ.

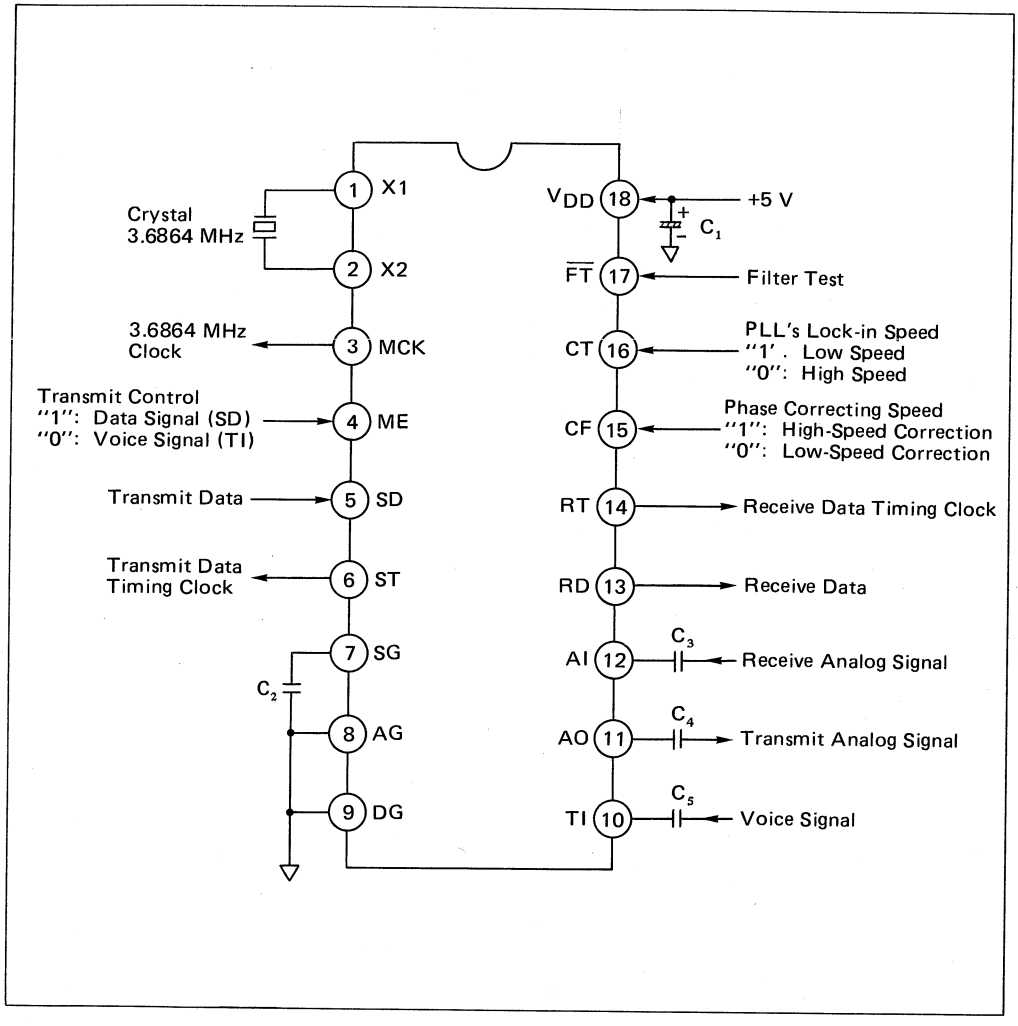
<table>
<tr><th>Pin Name</th><th>Pin No.</th><th>Function</th></tr>
<tr><td>AO</td><td>11</td><td>
Transmit analog signal output terminal. According to the control data on ME and $\overline{FT}$, AO is set to various state as an output terminal as follows.
<table>
<tr><th>$\overline{FT}$</th><th>ME</th><th>Transmit LPF</th><th colspan="2">State of AO</th></tr>
<tr><td>"1"</td><td>"1"</td><td rowspan="2">Power On</td><td rowspan="2">The output of Transmit LPF</td><td>MSK Signal</td></tr>
<tr><td>"1"</td><td>"0"</td><td>Voice Signal</td></tr>
<tr><td>"0"</td><td>"1"</td><td rowspan="2">Power Down</td><td colspan="2">The Output of Receive BPF (Used for Device Test Only)</td></tr>
<tr><td>"0"</td><td>"0"</td><td colspan="2">No-signal Output (DC-biased to SG)</td></tr>
</table>


The state when $\overline{FT}$ and ME = "0" is shown above. When the input digital data on $\overline{FT}$ changes to "1" from "0", AO remains to be connected to SG during about 12 ms and after that, and AO will be switched to transmit LPF. This delay time prevents AO from outputting meaningless signal during transient time from power down to on of LPF.
</td></tr>
<tr><td>AI</td><td>12</td><td>Receive analog signal input terminal. AI is biased internally to SG with about 100 kΩ same as TI. Receive BPF and demodulator extract the information in this signal and convert it into a serial data stream at RD output.</td></tr>
<tr><td>RD</td><td>13</td><td>Demodulated serial data output. This data is synchronized with the re-generated timing clock RT.</td></tr>
<tr><td>RT</td><td>14</td><td>
Receive data timing clock output. This signal is re-generated by internal digital PLL. Synchronizing to negative edge of RT, RD is output.


</td></tr>
</table>

<table>
<tr><th>Pin Name</th><th>Pin No.</th><th>Function</th></tr>
<tr><td>CF</td><td>15</td><td>Receive data timing clock is re-generated by digital PLL of which phase correcting speed can be selected with CF. When digital "1" is put on CF and phase difference between receive data timing and RT is more than 22.5 degree, phase correcting speed is high. In this case, as the phase difference enters within 22.5 degree, that speed changes to low immediately.
When digital "0" is input to CF, phase correcting speed of PLL remians to be low regardless of the phase difference..
Usually, CF is connected to digital "1".</td></tr>
<tr><td>CT</td><td>16</td><td>PLL's lock-in characteristics can be selected with CT. When digital "1" is put on CF, PLL requires max. 65 bit alternative data pattern. On the other hand, when digital "0" is input to CF, PLL can be locked in below 31 bit data.
<table><tr><th>Equipment</th><th>CT</th></tr><tr><td>Personal/MCA wireless terminals</td><td>"1"</td></tr><tr><td>MCA wireless bases</td><td>"0"</td></tr></table></td></tr>
<tr><td>$\overline{FT}$</td><td>17</td><td>Control signal for the internal connection of AO. Refer to column AO. When digital "0" is input to this pin, transmit LPF enters in power down mode, but the output buffer operational amplifier remains to be active.</td></tr>
<tr><td>VDD</td><td>18</td><td>+5 V power supply input terminal. This device is sensitive to supply noises as the switched capacitor techniques are utilized in plenty. By pass capacitor is indispensable to ensure the performance.</td></tr>
</table>

HINTS FOR APPLICATION



OKI semiconductor

CHIP SET FOR BELL 212A MODEM
(0 ~ 300 bps or 1200 bps IN FULL OR HALF-DUPLEX MODE)

GENERAL DESCRIPTION

This is the chip set to realize the data communication between computers or terminals via telephone line in full or half-duplex mode at a rate of 0 ~ 300 bps or 1200 bps.

This chip set consists of 6 LSIs. The MSM6950, MSM6928-06 and MSM61057 are OKI's original LSIs which are fabricated by OKI's low power CMOS silicon gate technology. The MSM80C31, MSM81C55 and MSM2764 are standard LSIs which can be sourced besides OKI.

Since this chip set provides most of all necessary functions for Bell 212A standard, only small number of MSIs, OP-amps and other components are required to make a complete modem set.

With this chip set, a modem which is compatible with the "Smartmodem 1200*" can be realized easily by programming MSM2764 accordingly by customer.

In the data sheets following herewith, OKI can provide application circuits of a modem based on Bell 212A standard by using this chip set.
(This modem is hereafter called OKI PC MODEM 212A.)

FEATURES

- Applied Netowrk: Public Switched 2-wire Line
- Network Interface: 600 ohm Balance
- DTE Interface: RS-232C (refer to 4-2.)
- Operating Mode: Full-duplex or Half-duplex
- Low Speed Data Format (0 ~ 300 bps): Serial/Binary/Asynchronous; 7 or 8 data bits; 1 or 2 stop bits; odd, even, or no parity.
- High Speed Data Format (1200 bps): Serial/Binary/Asynchronous;
  - 7 data bits; 1 or 2 stop bits; odd, even, or fixed parity.
  - 8 data bits; 1 or 2 stop bits; no parity.
- Modem Compatibility: Compatible with Bell System 103 or 212A modems, for asynchronous communication, in originate or answer mode.
- Receive Sensitivity: –45 dBm typical
- Transmit Level: –10 dBm typical
- Dialing Capability: Touch-Tone and Pulse (10 pps) Dialing
- Command Buffer: 40 Characters
- Power Supply Voltage: +5/–5 V, +12/–12 V (RS-232C)

<Additional High Speed Specifications>

- Input Data Rate: 1182 ~ 1212 bps
- Line Data Rate: 1200 bps ±0.01%
- Modem to Terminal Data Rate: 1219 bps
- Carrier Frequencies:

Originate Mode		Answer Mode	
Transmit:	1200 Hz ±0.01%	Transmit:	2400 Hz ±0.01%
Receive:	2400 Hz ±0.01%	Receive:	1200 Hz ±0.01%

- Received Signal Frequency Tolerance: ±7 Hz
- Data Modulation: 4-level Differential PSK at 600 baud ±0.01%
- Encoding:

Dibit	Phase Shift
00	+90
01	0
10	180
11	-90

- Scrambler Polynominal: $X = 1 + X^{-14} + X^{-17}$
- Line Equalization: Auto-equalizing function is provided in receiver

*Smartmodem 1200 is the registered trademark of Hayes Microcomputer Products Inc.,

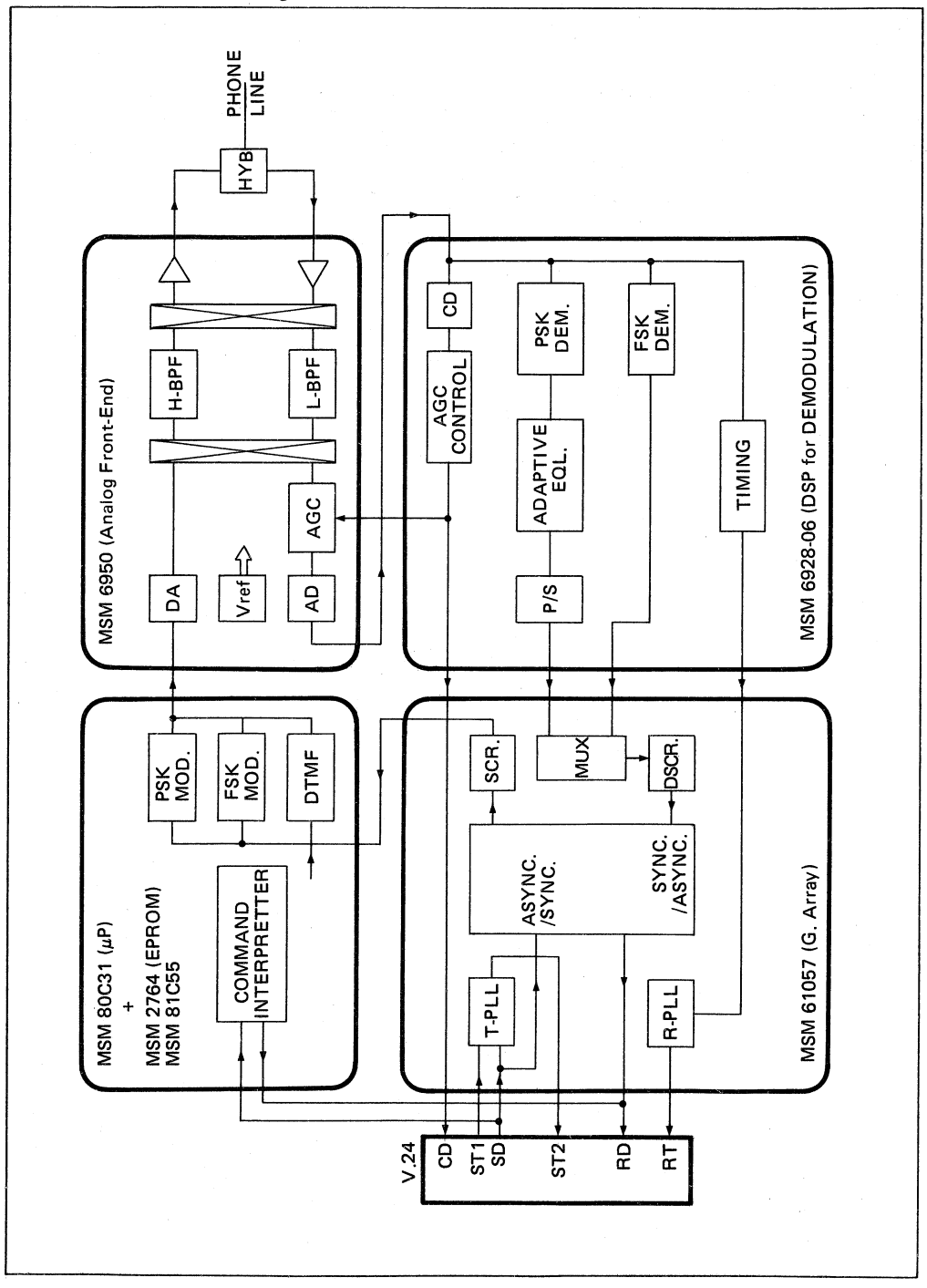
LIST OF CHIP SET

Type No.	Function	Power Dissipation Unit: mA				Package	
		Min	Typ	Max	Conditon	DIP	FLAT
MSM6950	Analog Front-End	—	12	20	+5 V	42 pin	56 pin
		—	11	20	-5 V		
MSM6928-06	DSP for Demodulation	—	35	40	+5 V	42 pin	60 pin
MSM61057	SYNC/ASYNC, Scramble/ Descramble	—	—	40		40 pin	60 pin
MSM80C31*1	Modulator, Hand-Shake, DTMF dialing	12	16	20		40 pin	44 pin
MSM81C55*2	I/O Port expander	—	—	5		40 pin	44 pin
MSM2764*3 or MSM27C64	ROM for MSM80C31	— —	— 32	100 —		28 pin	—

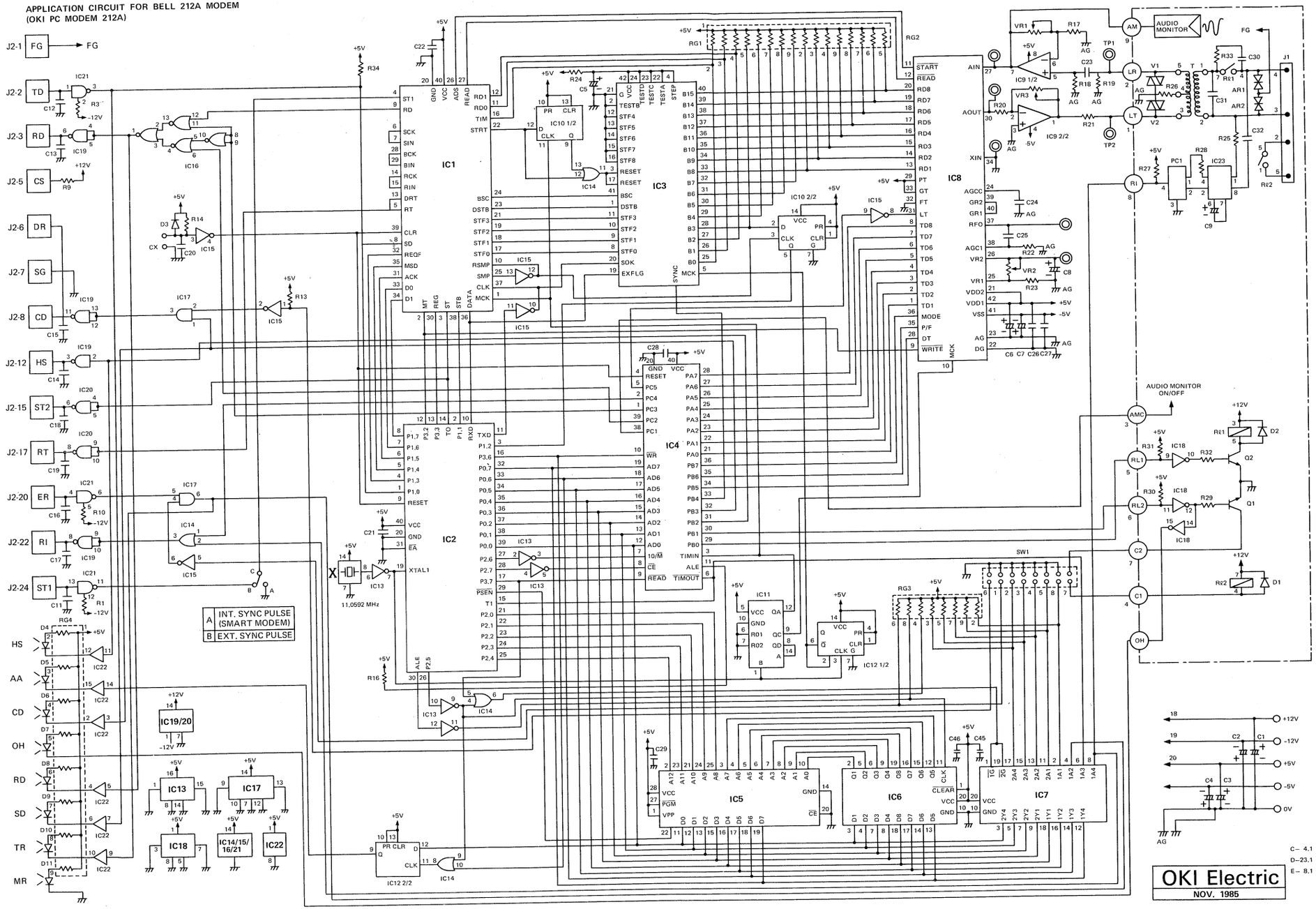
*1 Refer to the MICROCONTROLLER DATABOOK.
*2 Refer to the MICROPROCESSOR DATABOOK.
*3 Refer to the MEMORY DATABOOK.

212A MODEM BLOCK DIAGRAM

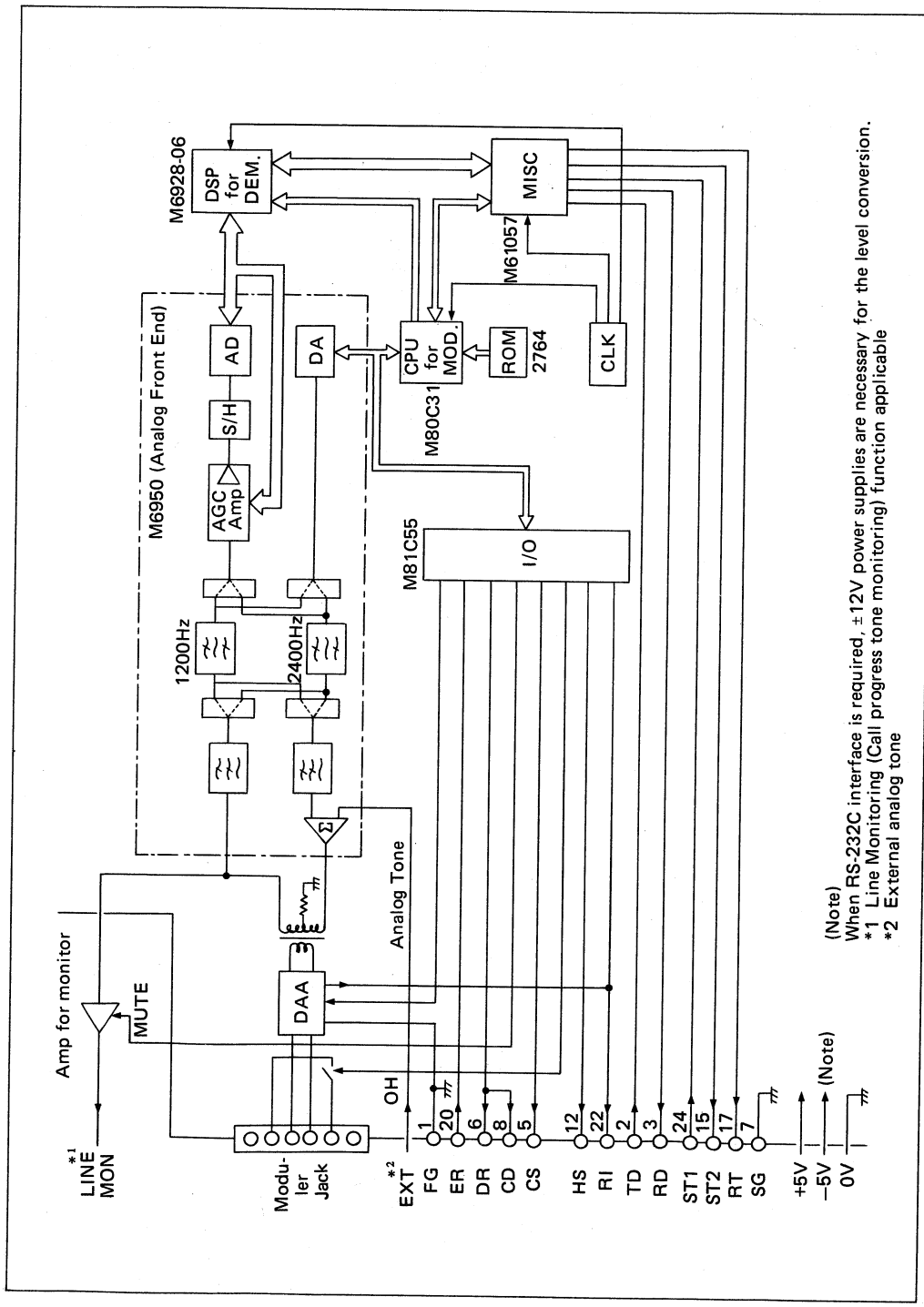
Function Circuit Block Diagram



APPLICATION CIRCUIT FOR BELL 212A MODEM
(OKI PC MODEM 212A)



Interconnections



III

Descriptions of Signal Interface (BD-25 Connector)

Pin No.	Circuit	Description	Direction
1	FG (AA)	Protective Ground	NA
2	TD (BA)	Transmit Data	To Modem
3	RD (BB)	Receive Data	From Modem
5	CS (CB)	Clear to Send	From Modem
6	DR (CC)	Data Set Ready	From Modem
7	SG (AB)	Signal Ground	NA
8	CD (CF)	Carrier Detect	From Modem
12	HS (CI)	High Speed Indicator	From Modem
20	ER (CD)	Data Terminal Ready	To Modem
22	RI (CE)	Ring Indicator	From Modem

Additional Interface

15	ST2 (DB)	Transmit Data Element Timing	From Modem
17	RT (DD)	Receive Data Element Timing	From Modem
24	ST1 (DA)	Transmit Data Element Timing	To Modem

Components Table (1/3) Chip Set; IC1, IC2, IC3, IC4, IC5, IC8

Name	Part Number	Note	Name	Part Number	Note
IC1	MSM61057RS		PC1	TLP521-1-A	Toshiba
IC2	MSM80C31RS		ARR1, 2	ERZ-C07DK151	Matsushita Denshi Buhin
IC3	MSM6928-06RS	DSP for Demodulator	RL1	NR-SD-12V	Matsushita Denko
IC4	MSM81C55RS		RL2	SY-12	Takamizawa
IC5	MSM2764	212A5Z	V1, 2	VR-61B-A	Shin Den Gen
IC6	MSM74HC273		Q1, 2	2SC372	
IC7	MSM74HC244		X	CX0-042B	(11.0592 MHz) Kinseki
IC8	MSM6950RS	Analog Front-End	D1, 2	V06C	
IC9	HA17458PS	Hitachi	D3	1S953	
IC10	MSM74HC74		D4~ 11	SEL1110R-Z	
IC11	HD74LS92	Hitachi			
IC12	MSM74HC74				
IC13	MSM74HC368		SW1	DYS-8	8-contacts DIP Switch
IC14	MSM74HC32		J1		6-Position Modular Jack
IC15	MSM74HC04		J2	DB-25SA-J4	DB-25 Connector JAE
IC16	MSM74HC02		T	31222-1	Daiwa Denki
IC17	MSM74HC08				
IC18	MSM4049				
IC19	HD75188P	Hitachi			
IC20	HD75188P	Hitachi			
IC21	HD75189P	Hitachi			
IC22	MSM4050				
IC23	TCM1520AP	Texas Inst.			

Components Table (2/3)

Name	Value	Tolerance	Wattage	Name	Value	Tolerance	Wattage
R1	39 kΩ	10%	1/4 W	R25	3.3 kΩ	10%	1/2 W
R2				R26	300 Ω	1%	1/4 W
R3	39 kΩ	10%	1/4 W	R27	10 kΩ	10%	1/4 W
R4				R28	2.4 kΩ	10%	1/4 W
R5				R29	2.2 kΩ	10%	1/4 W
R6				R30	10 kΩ	10%	1/4 W
R7				R31	10 kΩ	10%	1/4 W
R8				R32	2.2 kΩ	10%	1/4 W
R9	1.2 kΩ	10%	1/4 W	R33	150 Ω	10%	1/4 W
R10	39 kΩ	10%	1/4 W	R34	10 k	10%	1/4 W
R11							
R12							
R13	10 kΩ	10%	1/4 W				
R14	100 kΩ	10%	1/4 W				
R15							
R16	10 kΩ	10%	1/4 W				
R17	5.1 kΩ	1%	1/4 W	RG1	10 kΩ x 8	10%	1/4 W
R18	100 kΩ	1%	1/4 W	RG2	10 kΩ x 8	10%	1/4 W
R19	620 Ω	1%	1/4 W	RG3	10 kΩ x 8	10%	1/4 W
R20	51 kΩ	1%	1/4 W	RG4	330 Ω x 8	10%	1/4 W
R21	620 Ω	1%	1/4 W	VR1	Max 50 kΩ	Variable Resistor	
R22	100 kΩ	1%	1/4 W	VR2	Max 50 kΩ	Variable Resistor	
R23	33 kΩ	1%	1/4 W	VR3	Max 100 kΩ	Variable Resistor	
R24	2.4 Ω	+50% -20%	1/4 W				

Components Table (3/3)

Name	Value	Tolerance	DC-rated Voltage	Name	Value	Tolerance	DC-rated Voltage
C1	10 μF	50%	>15 V	C25	0.1 μF	50%	>15 V
C2	10 μF	50%	>15 V	C26	0.22 μF	50%	>15 V
C3	10 μF	50%	>15 V	C27	0.22 μF	50%	>15 V
C4	10 μF	50%	>15 V	C28	0.1 μF	50%	>15 V
C5	10 μF	50%	>15 V	C29	0.1 μF	50%	>15 V
C6	10 μF	50%	>15 V	C30	0.1 μF	50%	>15 V
C7	10 μF	50%	>15 V	C31	1000 pF	20%	>15 V
C8	10 μF	50%	>15 V	C32	0.47 μF	20%	>60 V
C9	10 μF	50%	>60 V	C33			
C10				C34			
C11	1000 pF	20%	>15 V	C35			
C12	1000 pF	20%	>15 V	C36			
C13	1000 pF	20%	>15 V	C37			
C14	1000 pF	20%	>15 V	C38			
C15	1000 pF	20%	>15 V	C39			
C16	1000 pF	20%	>15 V	C40			
C17	1000 pF	20%	>15 V	C41			
C18	1000 pF	20%	>15 V	C42			
C19	1000 pF	20%	>15 V	C43			
C20	0.47 μF	50%	>15 V	C44			
C21	0.1 μF	50%	>15 V	C45	0.1 μF	50%	>15 V
C22	0.1 μF	50%	>15 V	C46	0.1 μF	50%	>15 V
C23	0.022 μF	20%	>15 V				
C24	1 μF	50%	>15 V				

Initial Adjustment

Trimming for Reference Voltage

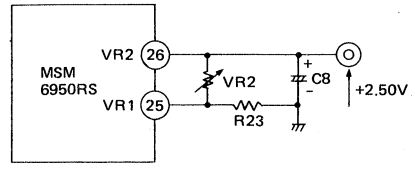


Figure-1

VR2 should be trimmed so that the DC voltage on pin 26 becomes +2.50 V.

Adjustment for Transmit/Receive Signal Level

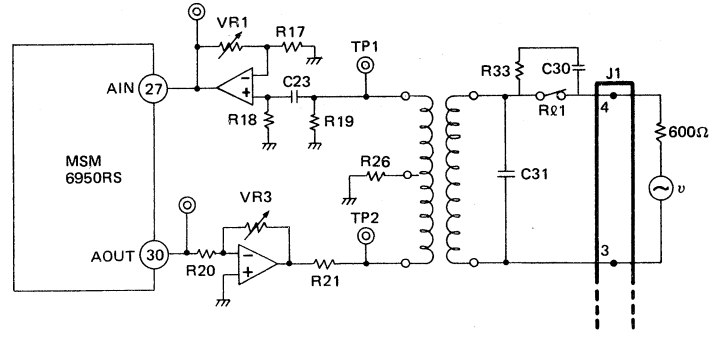


Figure-2

First, connect a 600 Ω signal source to pin 3 and pin 4 of J1 (normally 1200 Hz).

Next, make the signal source level minimum and make the modem send the PSK transmit signal to the phone line through the hybrid transformer using the "ATS10 = 255D" command mentioned in section 6-5.

Then, tune VR3 so that the signal between pin 3 and pin 4 of J1 should become −10 dBm.

Stop the modem to send the transmit signal using the "ATC0S10 = 255D" command and set the signal level between pin 3 and pin 4 of J1 at −10 dBm by increasing the signal source output level.

Then, tune VR1 so that the signal on AIN (pin 27) should be +4 dBm.

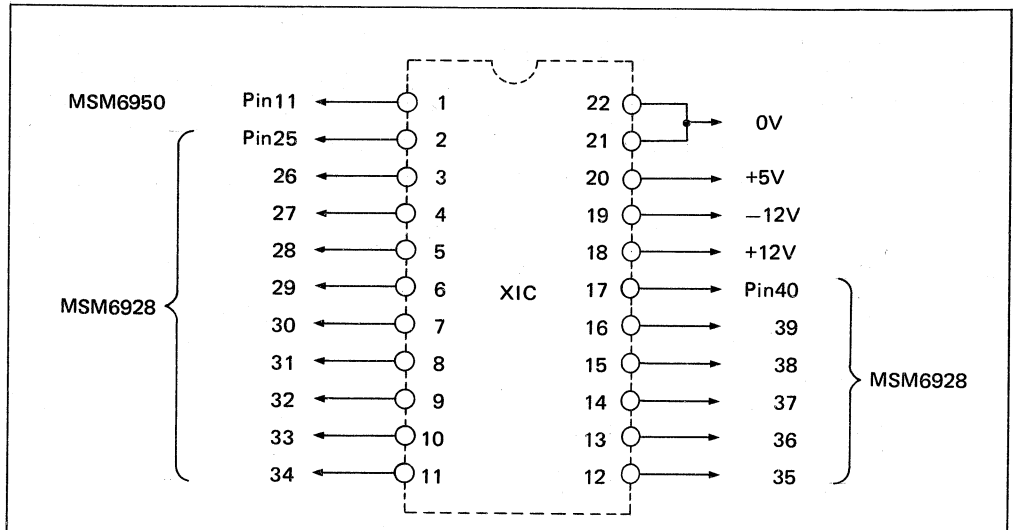
Note 1: 0 dBm = 0.775 Vrms
The input impedance of a level meter used for measurments must be "High".

Note 2: The mode of the level meter should be "Balance" when measuring the signal level between pin 3 and pin 4 of J1.
"Unbalance" mode should be used when measuring the signal level on AIN (pin 27), AOUT (pin 30), TP1 and TP2.

Decision Point of Monitoring

Decision point monitoring is the practical evaluation method.

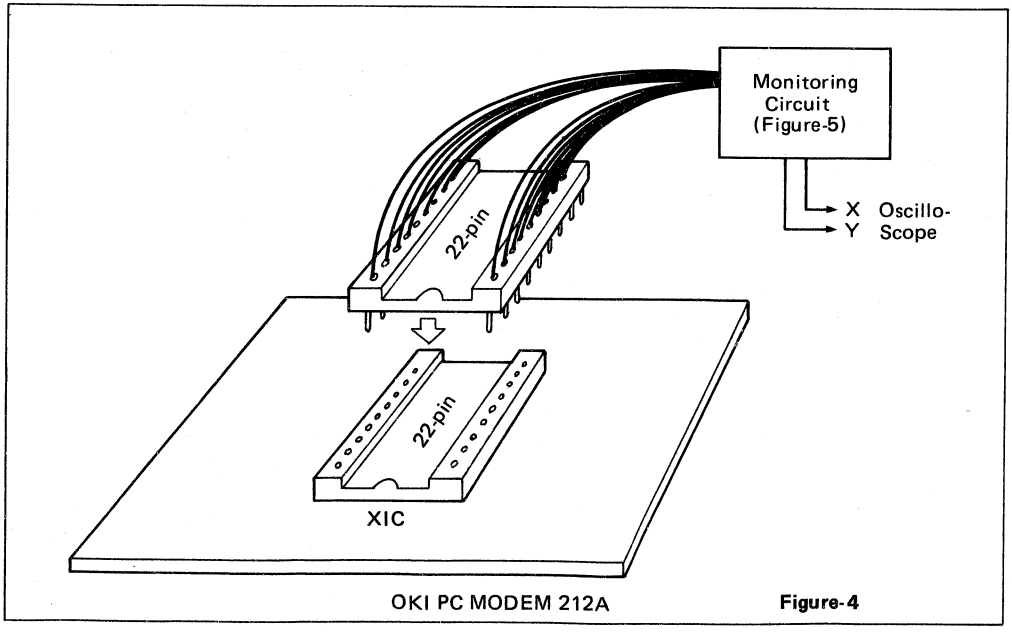
It can be easily performed by using XIC provided on the evaluation board and the external monitoring circuit.



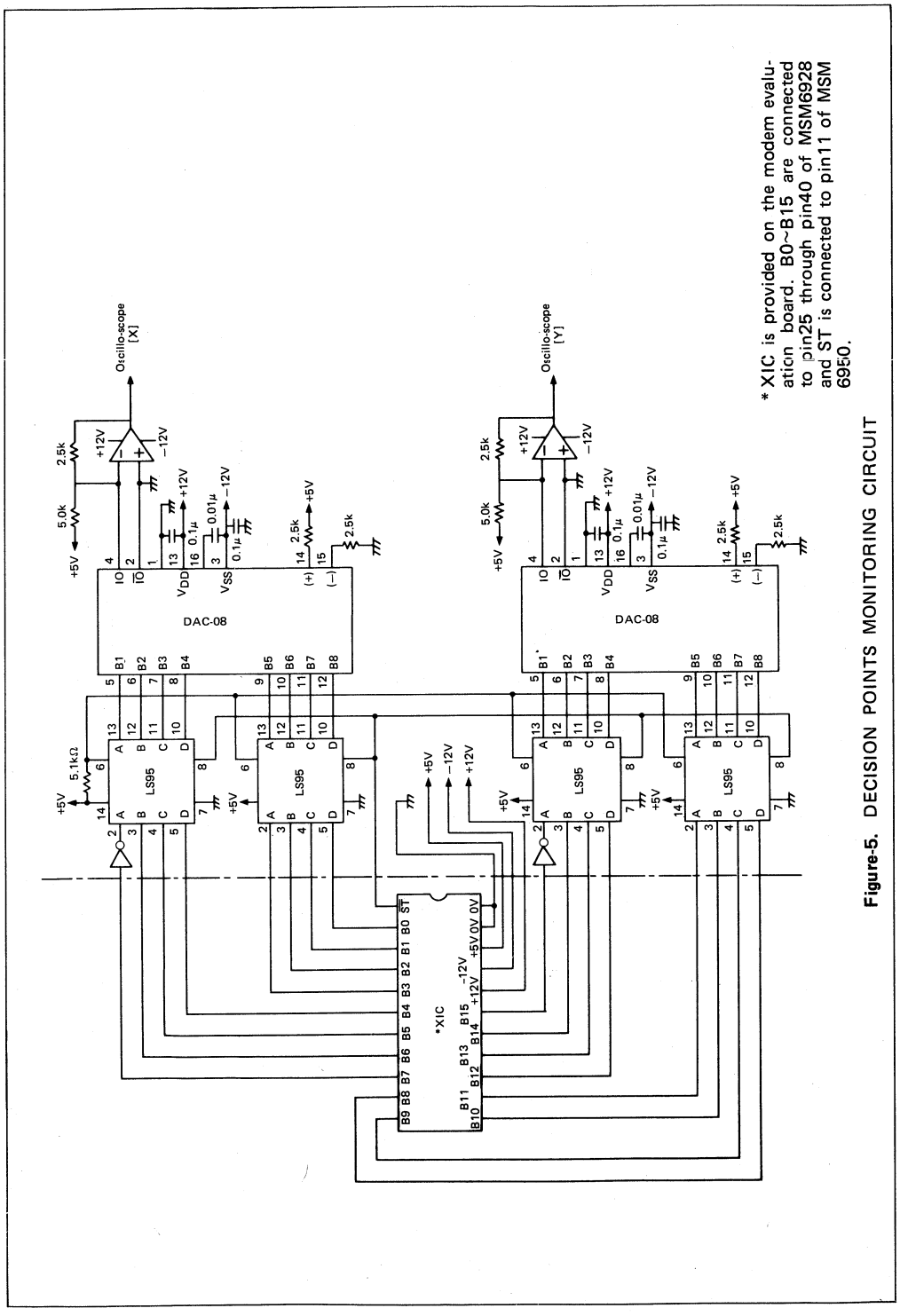
OKI PC MODEM 212A **Figure-3**

At first, it is required to put a 22 pin — IC socket into XIC's holes by soldering.

Figure-4 shows how to connect the external monitoring circuit (drawn in figure-5) through the XIC's socket.



OKI PC MODEM 212A **Figure-4**



* XIC is provided on the modem evaluation board. B0~B15 are connected to pin25 through pin40 of MSM6928 and ST is connected to pin11 of MSM 6950.

Figure-5. DECISION POINTS MONITORING CIRCUIT

CHIP SET FOR 2400 bps FULL DUPLEX MODEM

(0 ~ 300 bps, 1200 bps or 2400 bps IN FULL OR HALF DUPLEX MODE)

INTRODUCTION TO OKI PC MODEM 224

This chip set allows computers and terminals to communicate via telephone lines with other computers and terminals by using the additional microprocessor as the controller through an RS-232-C port. It operates on-line in full-duplex at a rate of 2400, 1200, 0 – 300 bps. It is compatible with CCITT V.22-bis, V.22, Bell 212A modem system.

This chip set consists of 5 LSIs. MSM80C51-98/99 (MICROCONTROLLER: MCU), MSM-6928-07 (Digital Signal Processor: DSP), MSM6950 (Analog Front End: AFE) and MSM-61077 (Gate Array: GA) and this chip set is hereafter called OKI PC MODEM 224.

Figure 1 shows the typical configuration of the 2400 bps full-duplex intelligent modem system. It consists of two blocks; One is the controller, and another is the original MODEM. As an intelligent data communications system just like the Smartmodem 2400 (Hayes Microcomputer Products, Inc.), the controller analyzes and executes commands and sends results codes in optional English word or decimal digit form. Therefore, this controller plays the role of the command interpreter, and also sets up the status of the original MODEM operation.

The OKI PC MODEM 224 is the original MODEM designed to construct the intelligent high-performance modem system, hence it needs the controller whose role is to set up the status and to define the several kinds of modes of modem operation. The interface between OKI PC MODEM 224 and the controller is designed to have flexibility and also to be adjustable. Using this chip set and the controller, a low-cost and compact-size intelligent modem system at 2400 bps in full-duplex can be realized easily.

III

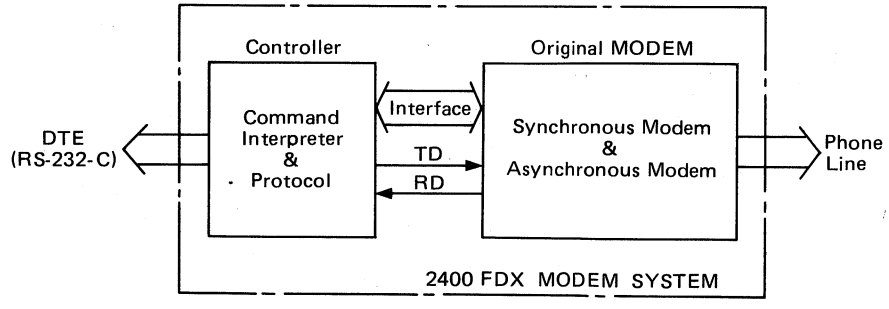


Figure 1 Typical configuration of 2400 FDX MODEM

FUNCTIONAL BLOCK DIAGRAM

Figure 2 shows the functional block diagram of the OKI PC MODEM 224. It consists of two parts; One is the speed conversion, another is synchronous modem, so that the composite one operates as an asynchronous modem. OKI PC MODEM 224 consists of four LSI-chips; MSM80C51-98/99 (MICROCONTROLLER: MCU) is functioning as synchronous to synchronous conversion and modulation, MSM61077 is functioning as synchronous to asynchronous conversion and transceiver PLL, MSM6928-07 and MSM6950 are functioning as demodulation and analog front and (AD, DA, Filters), respectively.

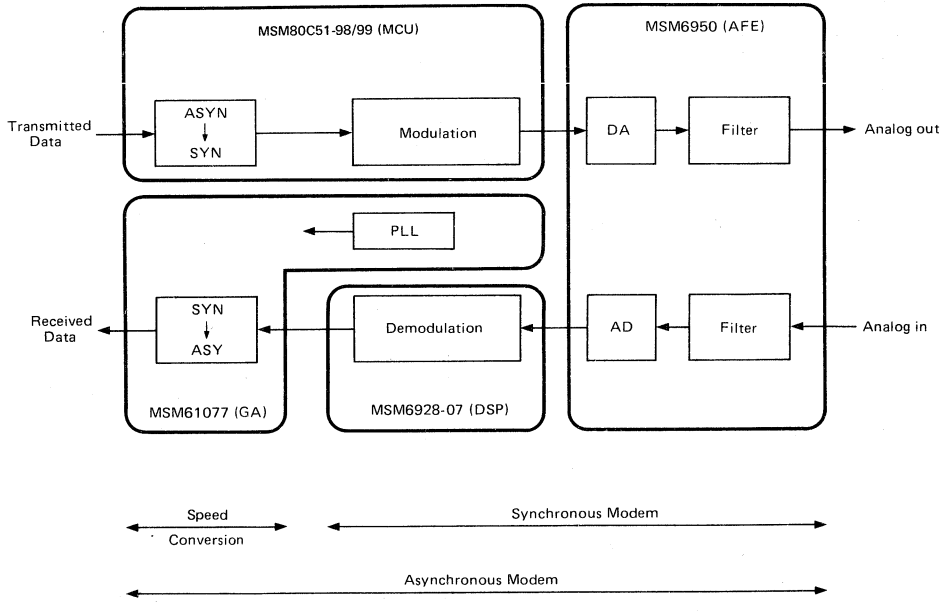


Figure 2 Functional block diagram of OKI PC MODEM 224

GENERAL CONTROL DATA FLOW

Figure 3 shows the schematic diagram of the control data flow. The data stream is divided into three groups; the first group is the parallel bit stream of approximate 3 bytes, that mainly control the operation modes of MSM80C51-98/99 (MICROCONTROLLER: MCU) and MSM6950, and that is the output port of MSM61077. The second one is the serial bit stream of 2 bytes, that define the status of MSM61077. The last one is the serial bit stream of 2 bytes, that are dealt as the input data of External Flags of DSP, and control the demodulation programing environments of MSM6928-07.

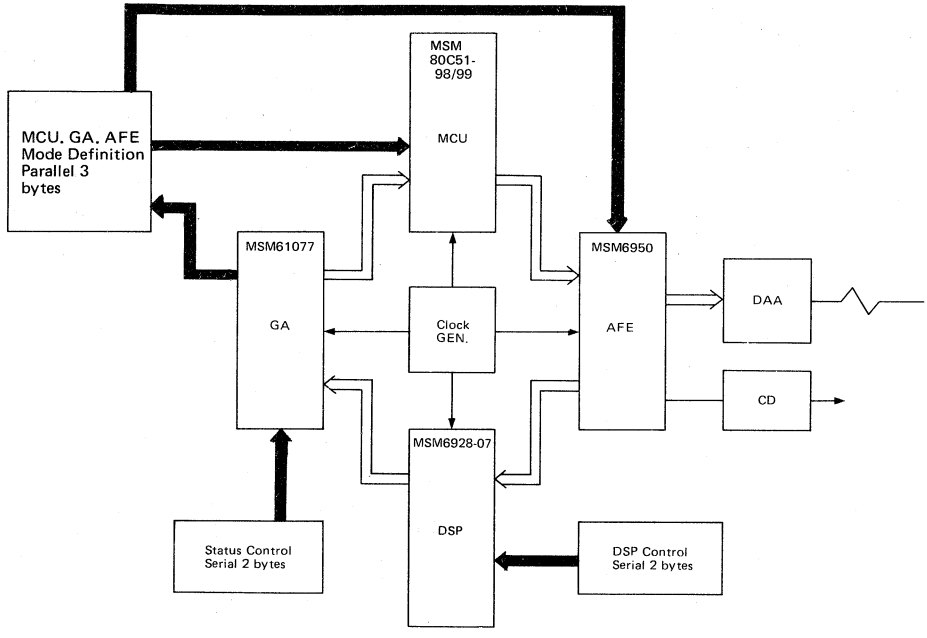


Figure 3 General control data flow

CONTROL DATA MAP

Figure 4 shows the control data map. Each map is represented by the elliptic circle, and is classified into the functional roles. The groups A-D correspond to each LSI chip.

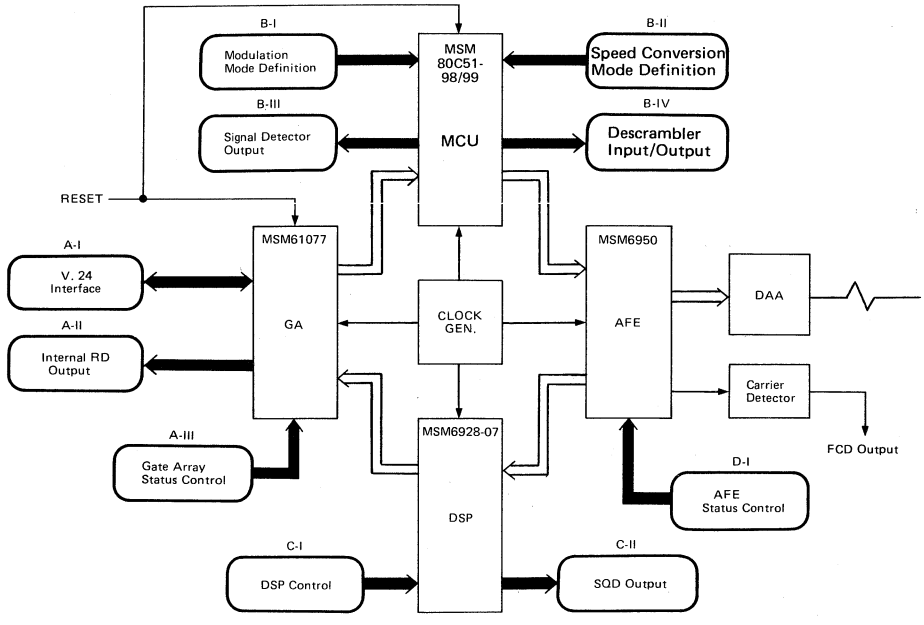


Figure 4 Control data map

1) Group A (MSM61077)

A-I)

Group A-I are fundamental CCITT V.24 interfaces, that are TD (Transmitted Data), RD (Received Data), $\overline{ST1}$ (transmitter timing from DTE), $\overline{ST2}$ (transmitter timing from DCE), and $\overline{RT}$ (Receiver timing).

A-II)

Group A-II are received data outputs directly given from the demodulator, that are D1 (Internal RD. . .PSK), D0 (Internal RD. . .FSK). Those outputs are used when evaluating the demodulator performance, or synchronous modem operation.

A-III)

Group A-III are the serial control data inputs, that are SDATA (control DATA), GSTB (Strobe clock), SCLK (Shift clock). The input data of SDATA are 16 bits data stream, whose assignments are described in the General Description.

Table 1 Control data of Group A (MSM61077)

Group A	Name	I/O	Function	Note
V.24 Interface (A-I)	TD	I	Transmitted Data	
	RD	O	Received Data	
	$\overline{ST1}$	I	Transmitter Timing	From DTE to DCE
	$\overline{ST2}$	O	Transmitter Timing	From DCE to DTE
	$\overline{RT}$	O	Receiver Timing	
Internal RD (A-II)	D0	O	Internal RD (PSK)	
	D1	O	Internal RD (FSK)	
	REQF	O	Enable D0 and D1	Also enable RDIN (B-IV)
Gate Array Status Control (A-III)	SDATA	I	Data	
	GSTB	I	Strobe Clock	
	SCLK	I	Shift Clock	Same as SCLK in C-I

III

2) Group B (MSM80C51-98/99)

B-I)

Group B-I are the modulation mode definitions, that are described briefly in the item of Control Data Table and also in details afterwards.

B-II)

Group B-II are the mode definitions of Asynchronous to Synchronous Speed Conversion, that are 1/2.3 (a rate of speed tolerance), SAS0-2 (character bit length selection). They are described in details in the item of the General Description.

B-III)

Group B-III are the special signal detector outputs, that are TRCD (S1 data detection specified in CCITT V.22 bis, S158 (TRCD timer selection), US1D (Unscrambled Mark detection). The S1 data is detected by means of observing the threshold energy level at some frequencies points, and detection periods are selected to 50 msec or 80 msec by S158 according to the cases of handshake sequence and retrain sequence. The US1D is detected through the descramble operation.

B-IV)

Group B-IV are the descrambler output port assignments, that are REQF (Enable RDIN, D0-1), RDIN (descrambler output at DSP0=1, or descrambler input at DSP0=0), ACK (Latch clock for RDIN, D0-1). Those are used when detecting unscrambled or scrambled mark at the handshake sequence through the descrambler operation.

Table 2 Control data of Group B (MSM80C51-98/99)

Group B	Name	I/O	Function	Note
Modulation Mode Definition (B-I)	INRS	I	Enable Transmitter	FSK, PSK, DTMF, etc.
	FSPS	I	Tone Select	
	DTA	I	These pins define the several kinds of modulation modes. Please see the paper described in detail.	
	DTB	I		
	MCP3	I		
	DOP2	I		
	SCP1	I		
	DSP0	I		
	DSS	I		
	A/O	I	Answer/Originate	
Speed Conversion Mode Definition (B-II)	1/2.3	I	Speed tolerance	+1.0%/-2.5% or +2.3%/-2.5%
	SAS2	I	Character Bit Length	
	SAS1	I		
	SAS0	I		
Signal Detector Output (B-III)	TRCD	O	S1 Data Detection	Specified in CCITT V.22-bis
	S158	I	TRCD Timer Select	50 msec/80 msec
	US1D	O	Unscrambled 1 Detection	
Descrambler Input/Output (B-IV)	RDIN	O	Descrambler Output (DSP0=1) Descrambler Input (DSP0=0)	
	ACK	O	Latch Clock for RDIN	Latch Clock for D0, D1 (A-II)

III

3) Group C (MSM6928-07)

C-I)

Group C-I are the serial control data inputs, that are EXTFLG (control DATA), DSTB (Strobe clock), SCLK (Shift clock). The input data of EXTFLG are 16 bits data stream, whose assignments are described in details in the items of General Description and Appendix B.

C-II)

Group C-II are the data signal quality detector outputs, that are SQDA (Demodulator has no convergence), SQDB (threshold level detection of bit error rate).

Table 3 Control data of Group C (MSM6928-07)

Group C	Name	I/O	Function	Note
DSP Control (C-I)	EXTFLG	I	Data	
	DSTB	I	Strobe clock	
	SCLK	I	Shift clock	Same as SCLK in A-III
SQD Output (C-II)	SQDA	O	Data signal quality	No convergence
	SQDB	O	Data signal quality	Threshold level

4) Group D (MSM6950)

D-I)

Group D-I are the status control data, DT (formation of call progress tone loop), PT (formation of DTMF tone loop), LT (formation of analog loop back), GT (guard tone selection), A/O (Answer/originate). Those are described in details in the item of General Description.

Table 4 Control data of Group D (MSM6950)

Group D	Name	I/O	Function	Note
AFE Status Control (D-I)	DT	I	Call progress tone loop	
	PT	I	DTMF tone loop	
	LT	I	Analog loop back	
	GT	I	Guard tone select	
	MODE	I	Answer/originate	

FEATURES OF OKI PC MODEM 224

- CCITT V.22-bis (2400, 1200).
- CCITT V.22 (1200, 600)
- Bell 212A (1200, 300 bps).
- Synchronous Mode operations; 2400, 1200, 600 bps +/- 0.01%.
- Asynchronous mode operations; 2400, 1200, 600 bps +1%, -2.5% (+2.3%, -2.5%) 0-300 bps (FSK).
- Character length; 8, 9, 10, 11 bits.
- 2w-full duplex, and half-dupiex.
- DTE interfaces of V.24 are TTL compatible.
- Included powerful Adaptive Equalizer.
- Tone transmitting capability;
  DTMF tone
  Guard tone (550,1800 Hz)
  Answer back tone (2100, 2225 Hz)
- Test loop facility; Digital loop, Analog loop, Remote Digital loop.
- All CMOS chips.
- Power Supplies; +5.0V, -5.0V.
- Typical Power Dissipation; 500 mW.

LIST OF CHIP SET

Table 5

Type No.	Function	Power Dissipation, Unit: mA				Package	
		Min	Typ	Max	Condition	DIP	FLAT
MSM6950	Analog Front End	–	12	20	+5 V	42 pin	56 pin
		–	11	20	-5 V		
MSM6928-07	DSP for demodulation, Adaptive equalizer and AGC control	–	35	40	+5V	42 pin	60 pin
MSM61077	Timing PLL, Random logic, Speed conversion	–	–	40	+5 V	–	60 pin
MSM80C51-98/99	Modulator, Scrambler/descrambler Speed conversion	12	16	20	+5V	40 pin (–98)	44 pin (–99)

III

OKI PC MODEM 224 BLOCK DIAGRAM

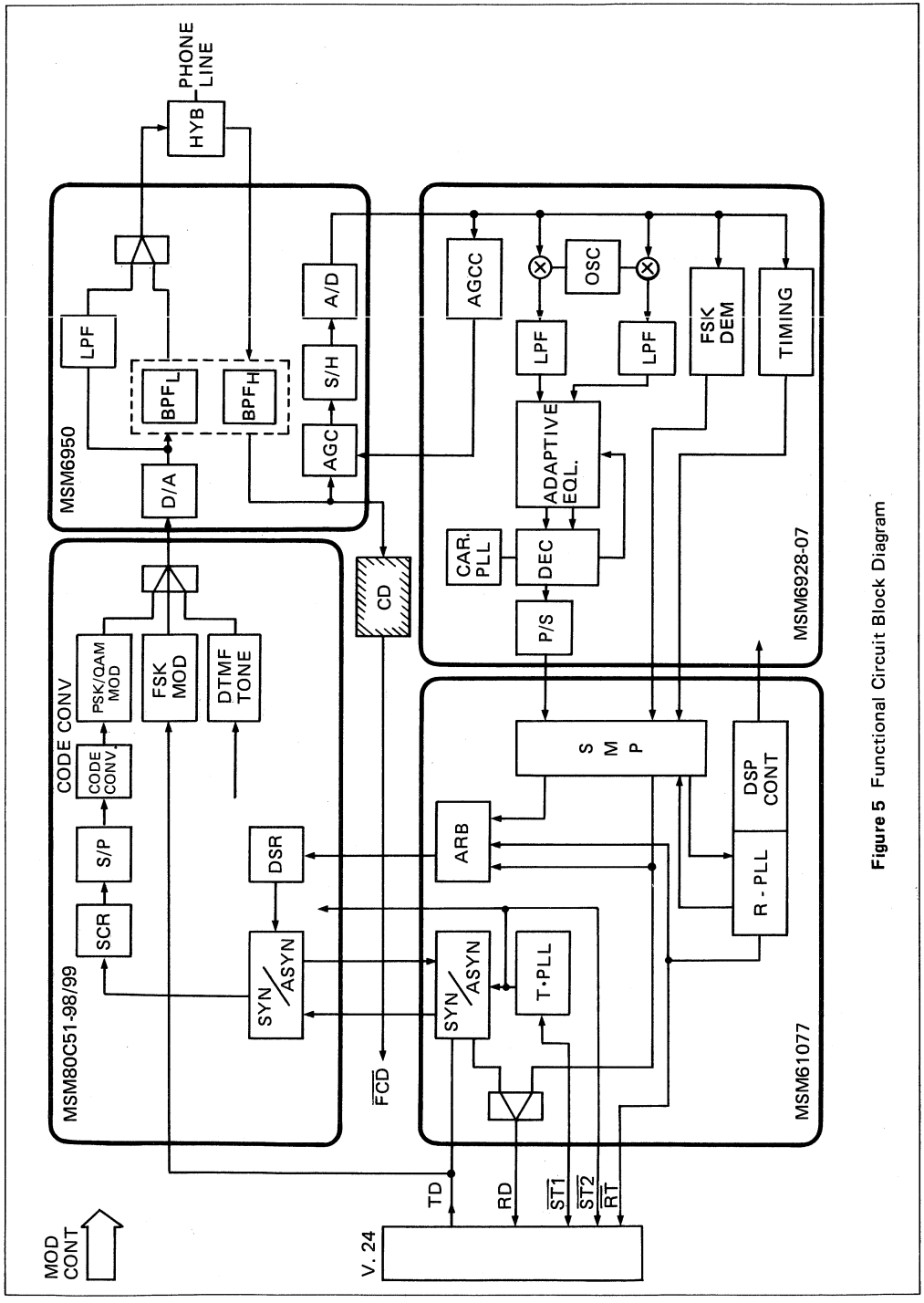


Figure 5 Functional Circuit Block Diagram

OKI PC MODEM 224 APPLICATION CIRCUIT

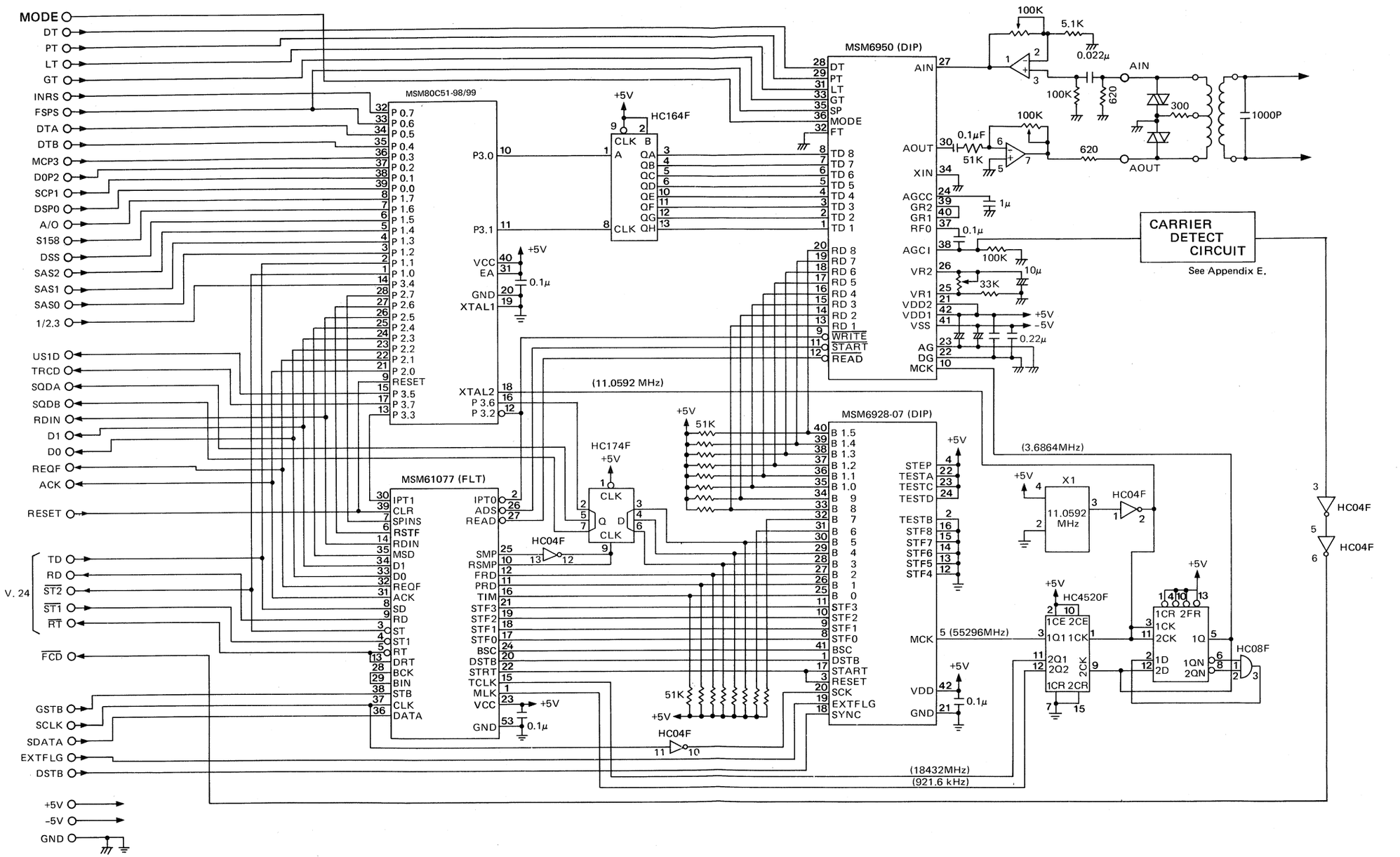


Figure 6 OKI PC MODEM 224 Application Circuit

INTERFACE SIGNAL DESCRIPTION

<table>
<tr><th>Interface</th><th>I/O</th><th>Description</th></tr>
<tr><td>DT
PT
LT
GT
MODE</td><td>I</td><td>MSM6950 (AFE) mode definition.
<table>
<tr><th colspan="2">Operation mode</th><th>DT</th><th>PT</th><th>GT</th><th>LT</th><th>MODE</th></tr>
<tr><td colspan="2">ORIGINATE (Transmit—Lowband)</td><td>1</td><td>1</td><td>X</td><td>0</td><td>0</td></tr>
<tr><td rowspan="3">ANSWER (Transmit —Highband)
Note: Guard tones shall be transmitted when DT=PT=0 only.</td><td>No guard tone</td><td>1</td><td>1</td><td>X</td><td>0</td><td>1</td></tr>
<tr><td>Guard tone; 550 Hz</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>Guard tone; 1800 Hz</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td colspan="2">DTMF tone, Answer Tone</td><td>0</td><td>1</td><td>1</td><td>0</td><td>X</td></tr>
<tr><td rowspan="2">Analog loop back</td><td>Highband</td><td>X</td><td>X</td><td>X</td><td>1</td><td>0</td></tr>
<tr><td>Lowband</td><td>X</td><td>X</td><td>X</td><td>1</td><td>1</td></tr>
</table>
Note 4)</td></tr>
<tr><td>A/O</td><td>I</td><td>Answer/originate selection
0; ORG (Transmit—Lowband)
1; ANS (Transmit—Highband)</td></tr>
<tr><td>INRS</td><td>I</td><td>0; Transmitter enable
1; Transmitter disable</td></tr>
<tr><td>FSPS</td><td>I</td><td>0; FSK modulation, Answer tone, DTMF tone
1; PSK, QAM modulation</td></tr>
<tr><td>DTA
DTB</td><td>I</td><td>
<table>
<tr><th>DTB/DTA</th><th>0</th><th>1</th></tr>
<tr><td>0</td><td>DTMF</td><td>FSK</td></tr>
<tr><td>1</td><td>Answer</td><td>FSK (mark)</td></tr>
</table>
<table>
<tr><th>DTB/DTA</th><th>0</th><th>1</th></tr>
<tr><td>0</td><td>Reversals (Note 2)</td><td>Data</td></tr>
<tr><td>1</td><td>S1 data (Note 1)</td><td>Mark</td></tr>
</table>
</td></tr>
<tr><td>MCP3</td><td>I</td><td rowspan="4">○ DTMF tone (DTA = 0, DTB = 0)
Refer to Table 6
○ Answer tone (DTA = 0, DTB = 1)
Refer to Table 7</td><td>Scrambler/descrambler instigation Note 3)
0; OFF 1; ON</td></tr>
<tr><td>DOP2</td><td>I</td><td>● See DSS column</td></tr>
<tr><td>SCP1</td><td>I</td><td>Scrambler control
0; Unscramble
1; Scramble</td></tr>
<tr><td>DSP0</td><td>I</td><td>Descrambler control
0; Undescramble
1; Descramble</td></tr>
<tr><td></td><td></td><td colspan="2">Note 1) S1 data: Unscrambled repetitive double dibit pattern of 00 and 11 at 1200 bps.
Note 2) Reversals: Alternating binary ones and zeros.
Note 3) To detect a sequence of 64 consecutive ones and to invert the next input. During Handshake and Remote DC Loop instigation, MCP3 must be Low.
Note 4) When analog loop back, MODE assignment is in reverse for A/O assignment.</td></tr>
</table>

<table>
<tr><th>Interface</th><th>I/O</th><th>Description</th></tr>
<tr><td>DSS</td><td>I</td><td>Data signalling rate selection
(Valid when PSK modulation)

<table>
<tr><th colspan="2">Data signalling rate</th><th>DSS</th><th>D0P2</th></tr>
<tr><td rowspan="2">2400 bps</td><td>QAM</td><td>0</td><td>0</td></tr>
<tr><td>Special Signals (invalid when DTA=1, DTB=0)</td><td>0</td><td>1</td></tr>
<tr><td>1200 bps</td><td>PSK (4 phases)</td><td>1</td><td>0</td></tr>
<tr><td>600 bps</td><td>PSK (2 phases)</td><td>1</td><td>1</td></tr>
</table>
Refer to Table 10 for details.</td></tr>
<tr><td>1/2.3</td><td>I</td><td>Speed conversion tolerance (Asynchronous mode)
0; +1.0% -2.5%
1; +2.3% -2.5%</td></tr>
<tr><td>RESET</td><td>I</td><td>Reset
0; Normal operation
1; Reset</td></tr>
<tr><td>S158</td><td>I</td><td>Timer selection of S1 data detection
0; 50 msec (Handshake)
1; 80 msec (Retraining start signal detect)</td></tr>
<tr><td>SAS2

SAS1

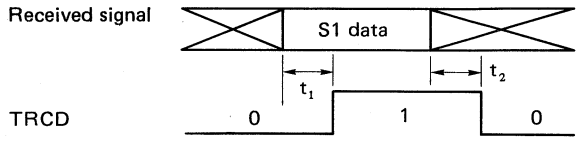
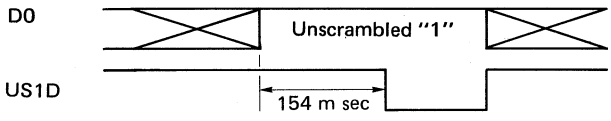
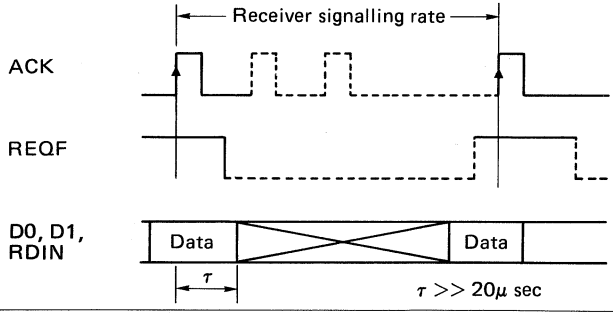
SAS0</td><td>I

I

I</td><td>Character bit length select

<table>
<tr><th colspan="3">Operation mode</th><th>SAS2</th><th>SAS1</th><th>SAS0</th></tr>
<tr><td colspan="2" rowspan="2">Synchronous</td><td></td><td>0</td><td>0</td><td>0</td></tr>
<tr><td></td><td>0</td><td>0</td><td>1</td></tr>
<tr><td rowspan="5">Asynchronous</td><td rowspan="2">BELL</td><td>9 bits</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>10 bits</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td rowspan="3">CCITT</td><td>8 bits</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>9 bits</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>10 bits</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td></td><td>11 bits</td><td>1</td><td>1</td><td>1</td></tr>
</table></td></tr>
<tr><td>$\overline{FCD}$</td><td>O</td><td>Fast carrier detection
0; CD – ON
1; CD – OFF

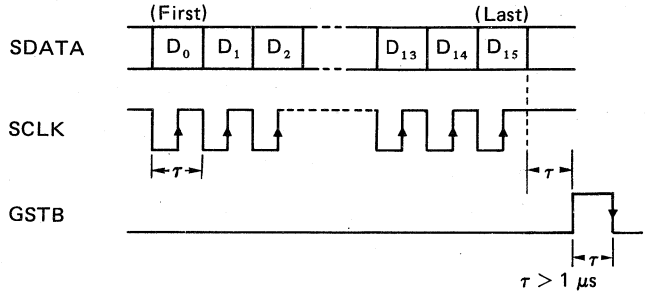
Note) Carrier detect circuit must be provided using the discrete components. Refer to Figure 6.</td></tr>
<tr><td>SQDA</td><td>O</td><td>Signal quality detector A (Optional function)
(Retrain request)
0; Normal quality
1; Abnormal quality</td></tr>
</table>

Interface	I/O	Description
SQDB	O	Signal quality detector B (Optional function) (Bit error rate) 0; BER (predictive) is under $10^{-3}/10^{-4}$ 1; BER (predictive) is over $10^{-3}/10^{-4}$ See SQDC in Table 9.
TRCD	O	S1 data detector output 0; Not detect 1; Detect t_1 : 50 or 80 ms (Selected by S158) $t_2 \leq 10$ ms 
US1D	O	Unscrambled mark detect output To detect unscrambled mark (digital "1") for 154 ms.  (Valid when $\overline{FCD}$ = "0")
ACK	O	Latch clock for D0, D1, RDIN. (Valid when REQF = 1) 
REQF	O	Status indicator of D0, D1 and RDIN data 0; Invalid 1; Valid
D0	O	Internal RD (PSK) (Undescrambled RD) 0; Space 1; Mark
D1	O	Internal RD (FSK) 0; Space 1; Mark

III

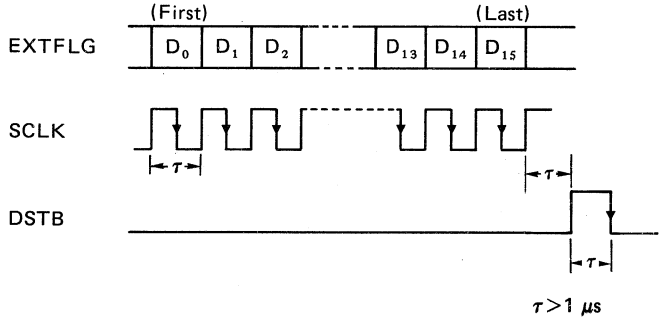
Interface	I/O	Description
RDIN	O	Descrambler input/output DSP0 = 0; RDIN is the undescrambled data. DSP0 = 1; RDIN is the descrambled data.
TD (V.24 interface)	I	Transmitted data 0; Space 1; Mark
$\overline{ST1}$ (V.24 interface)	I	Transmitter signal element timing input (to MODEM)
$\overline{ST2}$ (V.24 interface)	O	Transmitter signal element timing output (from MODEM)
RD (V.24 interface)	O	Received data 0; Space 1; Mark
$\overline{RT}$ (V.24 interface)	O	Receiver signal element timing output (from MODEM)
AOUT	O	Transmit analog signal output (to phone line)
AIN	I	Receive analog signal input (from phone line)

Interface	I/O	Description
SDATA	I	1. Serial control data for MSM61077 (GA)
SCLK	I	
GSTB	I	



Note: As for the description of $D_0 \sim D_{15}$, refer to the Table 8.

Interface	I/O	Description
DSTB	I	2. Serial control data for MSM6928-07 (DSP)
EXTFLG	I	



Note: As for the description of $D_0 \sim D_{15}$, refer to the Table 9.

Interface	I/O	Description
+5 V		Positive power supply
-5 V		Negative power supply
GND		Ground, 0V

Note) Higher dual power supplies, for instance, ±12V may be necessary for the analog line interface circuit when the transmit and receive analog signal level cannot be satisfied with ±5V power supplies.

Table 6 DTMF Tone

MCP 3	DOP 2	SCP 1	DSP 0	Symbol	Lowband Frequency	Highband Frequency
0	0	0	0	1	697 Hz	1209 Hz
0	0	0	1	2	697	1336
0	0	1	0	3	697	1477
0	0	1	1	4	770	1209
0	1	0	0	5	770	1336
0	1	0	1	6	770	1477
0	1	1	0	7	852	1209
0	1	1	1	8	852	1336
1	0	0	0	9	852	1477
1	0	0	1	0	941	1336
1	0	1	0	*	941	1209
1	0	1	1	#	941	1477
1	1	0	0	A	697	1633
1	1	0	1	B	770	1633
1	1	1	0	C	852	1633
1	1	1	1	D	941	1633

III

Table 7 Answer Tone

MCP 3	DOP 2	SCP 1	DSP 0	Answer Tone Frequency
–	–	–	0	2100 Hz
–	–	–	1	2225 Hz

Table 8 MSM61077 Serial Control Data Table

No.	Name	Description
D0	TESTA	0; Normally set at digital "L" level. 1; Test mode. In the testing mode of this I.C., digital "H" have to be applied
D1	DSS1	Data signalling rate select 0; 2400 bps 1; 1200/600 bps (refer to D7)
D2	SDCLP	Enable GASAS, SWLA, SWLB 0; Disable note 1) 1; Enable
D3	GA123	Speed conversion tolerance selection 0; +1%/–2.5% 1; +2, 3%/–2.5%
D4	GAVB	Speed conversion method selection 0; CCITT 1; Bell
D5	CD1	Receive timing PLL control 0; Free run 1; Normal operation
D6	CD2	Lock in time control of receive timing PLL 0; Slow 1; Fast
D7	DSSO	Data signalling rate select 0; 1200 bps 1; 600 bps
D8	GADC	Received Data (RD) select 0; Asynchronous (Receiver speed converter output) 1; Synchronous (Direct demodulator output) Note 2)
D9	GASAS	Speed conversion control 0; Asynchronous (Enable speed converters) 1; Synchronous (Disable speed converters) Note 3)
D10	GALSHS	Transmission mode control for AFE (6950) 0; 600/1200/2400 bps 1; 300 pbs, DTMF, Answer Tone Note 4)
D11	GASLSH	Originate or answer mode select 0; Answer (Transmit – Highband) 1; Originate (Transmit – Lowband)

No.	Name	Description
D12	SWLA	Character bit length (Asynchronous mode)
D13	SWLB	

SWLB	SWLA	Character Length
0	0	8 bits
0	1	9 bits
1	0	10 bits
1	1	11 bits

No.	Name	Description
D14	STA	Transmit element timing select
D15	STB	

STB	STA	Transmit timing
0	0	$\overline{ST}_2$
0	1	
1	0	$\overline{ST}_1$
1	1	$\overline{RT}$

Note 1) When SDCLP=0, don't change GASAS, SWLA, and SWLB. Keep the previous status. If changing GASAS, SWLA and SWLB when SDCLP=0, mis-operating may happen in the IC.
Note 2) In case of receiving FSK signal, GADC must be HIGH.
In case of synchronous operation (PSK, QAM), Both GADC and GASAS must be HIGH.
In case of asynchronous operation (PSK, QAM), Both GADC and GASAS must be LOW.
Note 3) Speed converters mean SYN/ASYN and ASYN/SYN converters.
Note 4) When GADC=1, if GALSHS=1, RD is demodulated FSK signal.
if GALSHS=0, RD is demodulated PSK or QAM signal.

Table 9 MSM6928-07 Serial Control Data Table

<table>
<tr><th>No.</th><th>Name</th><th>Description</th></tr>
<tr><td>D0</td><td>XFCD</td><td>FCD (carrier detect) signal for Demodulator
0; OFF (Set 0 when $\overline{FCD}$ = 1)
1; ON (Set 1 when $\overline{FCD}$ = 0)</td></tr>
<tr><td>D1</td><td>TAPH</td><td>AEQL operation control
0; Active
1; Hold</td></tr>
<tr><td>D2
D3</td><td>DSS0
DSS1</td><td>Demodulator data signalling rate select
<table>
<tr><th>DSS1</th><th>DSS0</th><th colspan="2">Mode</th></tr>
<tr><td>0</td><td>0</td><td rowspan="2">16 values QAM</td><td rowspan="2">2400 bps</td></tr>
<tr><td>0</td><td>1</td></tr>
<tr><td>1</td><td>0</td><td>4 phase PSK</td><td>1200 bps</td></tr>
<tr><td>1</td><td>1</td><td>2 phase PSK</td><td>600 bps</td></tr>
</table>
Note) Not related to FSK mode.</td></tr>
<tr><td>D4
D5</td><td>EGC0
EGC1</td><td>AEGL tap coefficient control
<table>
<tr><th>EGC1</th><th>EGC0</th><th>α</th></tr>
<tr><td>0</td><td>0</td><td>α_1</td></tr>
<tr><td>0</td><td>1</td><td>α_2</td></tr>
<tr><td>1</td><td>0</td><td>α_3</td></tr>
<tr><td>1</td><td>1</td><td>α_4</td></tr>
</table>
See Appendix B.
Note) α_4 = 0 (Tap hold)</td></tr>
<tr><td>D6</td><td>AQID</td><td>Adaptive equalizer (AEQL) reset
0; Reset (Set the center tape)
1; Normal operation
See Appendix B.</td></tr>
<tr><td>D7</td><td>PLCR</td><td>Carrier PLL reset
0; Reset
1; Normal operation</td></tr>
</table>

<table>
<tr><th>No.</th><th>Name</th><th>Description</th></tr>
<tr><td>D8</td><td>PLEN</td><td>Carrier PLL enable
0; Disable
1; Enable</td></tr>
<tr><td>D9</td><td>SANSORG</td><td>Originate/answer mode select for receiver
0; Answer (Receive – Lowband)
1; Originate (Receive – Highband)</td></tr>
<tr><td>D10
D11</td><td>AGCT0
AGCT1</td><td>AGC circuit control coefficients
<table>
<tr><th>AGCT1</th><th>AGCT0</th><th>β</th></tr>
<tr><td>0</td><td>0</td><td>β_1</td></tr>
<tr><td>0</td><td>1</td><td>β_2</td></tr>
<tr><td>1</td><td>0</td><td rowspan="2">β_3</td></tr>
<tr><td>1</td><td>1</td></tr>
</table>
See Appendix B.</td></tr>
<tr><td>D12</td><td>SQDC</td><td>Threshold level selection for SQDB
0; High ($\sim 10^{-3}$)
1; Low ($\sim 10^{-4}$)
See Appendix B.
NOTE) Does not mean to measure the bit error rate itself.</td></tr>
<tr><td>D13</td><td>SQDEN</td><td>LPF accumulate register clear for SQDA and SQDB
(signal quality detecter)
0; Normal operation
1; Reset
See Appensix B.</td></tr>
<tr><td>D14</td><td>TRCDC</td><td>Threshold level for S1 data detection
0; Low (Handshake)
1; High (Retrain)</td></tr>
<tr><td>D15</td><td>XFCD1</td><td>DSP software reset except for AGC control
0; Normal operation
1; Reset</td></tr>
</table>

III

Table 10 shows the summary of transmitter mode definition. Table 11 shows the category of control data.

In table 11, Initial Installation means the initialization procedure at power ON, or at make up call. Call Progress means dialing procedure concerning the transmitting DTMF tone and detecting call progress tones. Handshake means Handshake sequence specified in the CCITT recommendation or BELL 212A Critera. Test Loop means testing procedure specified in the CCITT recommendation or BELL 212A Critera.

Monitor means the output signals which the controller should observe during handshake sequence or data mode. Each control data is classified into these categories, and some of control data belong to different categories in duplicate.

Please note that each control data will be mainly controlled in each procedure, but in special case, may be controlled in other procedure.

Table 10 Transmitter Mode Definition Table

X : Irrespective of 1/0
1 : Logical High
0 : Logical Low

Operations			INRS	FSPS	DTA	DTB	MCP3	DOP2	SCP1	DSP0	DSS	GA		
												DSS1	DSS0	GALSHS
Transmitter Disable			1	X	X	X	X	X	X	X	X	X	X	X
DTMF Tone			0	0	0	0	See table 6				X	X	X	1
Answer Tone			0	0	0	1	See table 7				X	X	X	1
DATA	FSK	300 bps	0	0	1	0	X	X	X	X	X	X	X	1
	PSK	600 bps	0	1	1	0	1	1	1	1	1	1	1	0
		1200 bps	0	1	1	0	1	0	1	1	1	1	0	0
	QAM	2400 bps	0	1	1	0	1	0	1	1	0	0	X	0
Special Signal	PSK	S1 data*	0	1	0	1	0	0	0	X	1	1	0	0
			0	1	0	1	0	1	0	X	0	0	X	0
		USR/SCR-1*	0	1	1	1	0	0	0/1	X	1	1	0	0
			0	1	1	1	0	1	0/1	X	0	0	X	0
		Reversals*	0	1	0	0	0	0	0	X	1	1	0	0
			0	1	0	0	0	1	0	X	0	0	X	0

* When DOP2 = 1 and DSS = 0, Data Signalling Rate between DTE and Modem is at 2400 bps.
But, Modulation Rate is maintained at 1200 bps. These mode shall be difined in the handshake sequence.

Table 11 Category of Control Data

		Initial Installation	Call Progress	Hand-shake	Test Loop	Monitor	Notes
Parallel Control Data	DT		○	○			DTMF Tone Loop, Dial Tone Loop, with or without Guard Tone.
	PT		○	○			
	LT				○		When LT = 1, AC Loop will be formed in 6950.
	GT	○					
	MODE	○					
	A/O	○			○		When AC Loop Test, Transmitter mode must be in reverse.
	INRS		○	○			Transmitter mode definition • DTMF, Answer Tone, • FSK, PSK, QAM • Unscramble, Scramble Mark • Data Signalling Rate
	FSPS		○	○			
	DTA		○	○			
	DTB		○	○			
	MCP3		○	○			
	DOP2		○	○			
	SCP1		○	○			
	DSP0		○	○			
	DSS		○	○			
	1/2.3	○					
	RESET	○					
	S158			○			S158 shall be controlled as same as TRCDC.
	SAS2	○					
	SAS1	○					
	SAS0	○					
	$\overline{FCD}$					○	$\overline{FCD}$ status shall be always sensed in real-time.
	SQDA					○	Controller should observe SQD output frequently in order to request Retrain sequence if necessary.
	SQDB					○	
	TRCD					○	
	US1D					○	In Data mode, US1D shall be used to detect RDL requirement.
	ACK					○	
	REQF					○	
	D0					○	By observing D0, D1, and RDIN at the same time, Controller can recognize whether received signal is unscramble-1, scramble-1 or FSK mark.
	D1					○	
	RDIN					○	
	TD			○		○	These signals are V.24 interfaces. Controller shall intermediate to accomodate these signals to the proper V.24 interface timing and status.
	$\overline{ST1}$			○		○	
	$\overline{ST2}$			○		○	
	RD			○		○	
	$\overline{RT}$			○		○	
	AOUT						Analog input and output in 6950.
	AIN						

		Initial Installation	Call Progress	Hand-shake	Test Loop	Monitor	Notes
GA Serial Control Data	TESTA	○					TESTA must be Logical Low.
	DSS1			○			
	SDCLP	○					
	GAL23	○					
	GAVB	○					
	CD1			○			Timing PLL of demodulator.
	CD2			○			
	DSS0			○			
	GADC			○			
	GASAS	○					
	GALSHS		○	○			GALSHS controls write clock of 6950.
	GASLSH	○			○		When AC Loop Test, GA mode must be in reverse.
	SWLA	○					
	SWLB	○					
	STA	○			○		In RDL, both STA and STB shall be Logical High.
	STB	○			○		
DSP Serial Control Data	XFCD			○			XFCD equals to negative logical state of $\overline{FCD}$.
	TAPH			○			Tap hold control for AEQL.
	DSS0			○			Data signalling rate of PSK/QAM demodulator in DSP.
	DSS1			○			These are no relationship with FSK demodulator in DSP.
	EGC0			○			Adaptive EQL control
	EGC1			○			
	AQID			○			
	PLCR			○			Carrier PLL control
	PLEN			○			
	SANSORG	○			○		
	AGCT0			○			AGC control
	AGCT1			○			
	SQDC	○					SQD control
	SQDEN			○			
	TRCDC			○			
	XFCD1			○			

HANDSHAKE SEQUENCE

Figure 7 to Figure 14 show the timing charts of control data in the Handshake Sequences as follows.

Figure 7	2400 bps	Orig. Modem	CCITT
Figure 8	2400 bps	Ans. Modem	CCITT
Figure 9	1200 bps	Orig. Modem	CCITT
Figure 10	1200 bps	Ans. Modem	CCITT
Figure 11	1200 bps	Orig. Modem	BELL
Figure 12	1200 bps	Ans. Modem	BELL
Figure 13	300 bps	Orig. Modem	BELL
Figure 14	300 bps	Ans. Modem	BELL

The timing charts of control data in CCITT 600 bps Orig./Ans. are same as those in CCITT 1200 bps Orig./Ans. except for data signalling rate assignments. In CCITT 600 bps, data signalling rate assignments, (DSS1, DSS0) of GA, (DSS1, DSS0) of DSP, and (DSS, DOP2) of MCU are logical high each other.

Before studying Handshake, please read the CCITT recommendations of V.22 and V.22-bis, also BELL 212A Critera carefully ! ! !

III

Supplementary Comments about Handshake Sequence.

(Originate Modem)

1) Originate modem shall wait the answer tone transmitted from the answer modem after dialing procedures. The answer tone detector of 2100 Hz is not incorporated in this chip set, therefore, carrier detection circuit is functioning as the detector. But the answer tone of 2225 Hz will be correctly detected by FSK demodulator in DSP through D1 output pin installed at GA.
2) AGC control should start after XFCD turning OFF to ON. After 20 ms, AGC output level deviation will be converged within a limited range.
3) In CCITT mode, Carrier PLL control of PLEN and PLCR should be controlled 20 ms later at the head of unscramble-1 in order to detect unscramble-1 correctly.
4) There are two methods to recognize unscramble-1. One is to observe US1D output, and the other is to observe D0 output.
5) AEQL control should start 100 ms after the end of S1 data (2400) or the end of unscramble-1 (1200). Because it takes 100 ms for timing PLL to be locked in a tolerance range.

6) In 2400 bps establishment, after recognizing S1 data each other, Data Signalling Rate for DTE shall be changed to 2400 bps. From this time, Data Signalling Rate of GA will be changed to 2400 bps, and also Data Signalling Rate between GA and MCU will be changed to 2400 bps. Transmitter should, however, transmit the signal of S1 data or scramble-1 at 1200 bps. At this time, special signal transmitting mode is prepared. When DOP2=1 and DSS=0, Data Signalling Rate is at 2400 bps, but modulation is maintained on 4 phase at 1200 bps. In this case, transmitter decimates the incoming signal at 2400 bps, and keeps modulation on 4 pahse PSK at 1200 bps.

(Answer Modem)

1) Generally speaking, Answer modem should adopt own data signalling rate to the opposite modem (Originate modem). Therefore, Answer modem must observe the several kinds of incoming signals at the same time because Answer modem can't know whether Originate modem is set on 300 bps, 1200 pbs, or 2400 pbs. In this case, the first judgement will be decided when detecting the first incoming signal, that is S1 data, scramble-1, or FSK mark (1270 Hz).
   In this situation, when DSP0 is set on High, S1 data, scramble-1, and FSK mark can be detected at the same time through TRCD, RDIN, D1 outputs, respectively.

2) In Answer modem, AGC control, carrier PLL control, and AEQL control are almost same as those of Originate modem, but those control sequences are not separated unlike the Originate modem. As shown in the timing charts, each sequence should be controlled orderly (control after control).

3) In 1200 bps/BELL establishment, scramble-1 signal should be detected while transmitting Answer tone. In this case, the state of DSP0 concerning to descrambler control will be neglected because of Low state of FSPS. Hence, descrambler is uncontrollable externally at this time. But, if DSP0 is set on High before FSPS turning to OFF, the previous state (that is logical High) of DSP0 will be memorized in MCU, and as the result, descrambled output data will appear at RDIN.

4) In FSK receiving, the control sequence concerning about carrier PLL, timing PLL and AEQL of demodulator will not be cared.

5) In Data mode, US1D output shall be used as interrupt signal for controller to reply remote DC loop test requirement of the opposite modem.

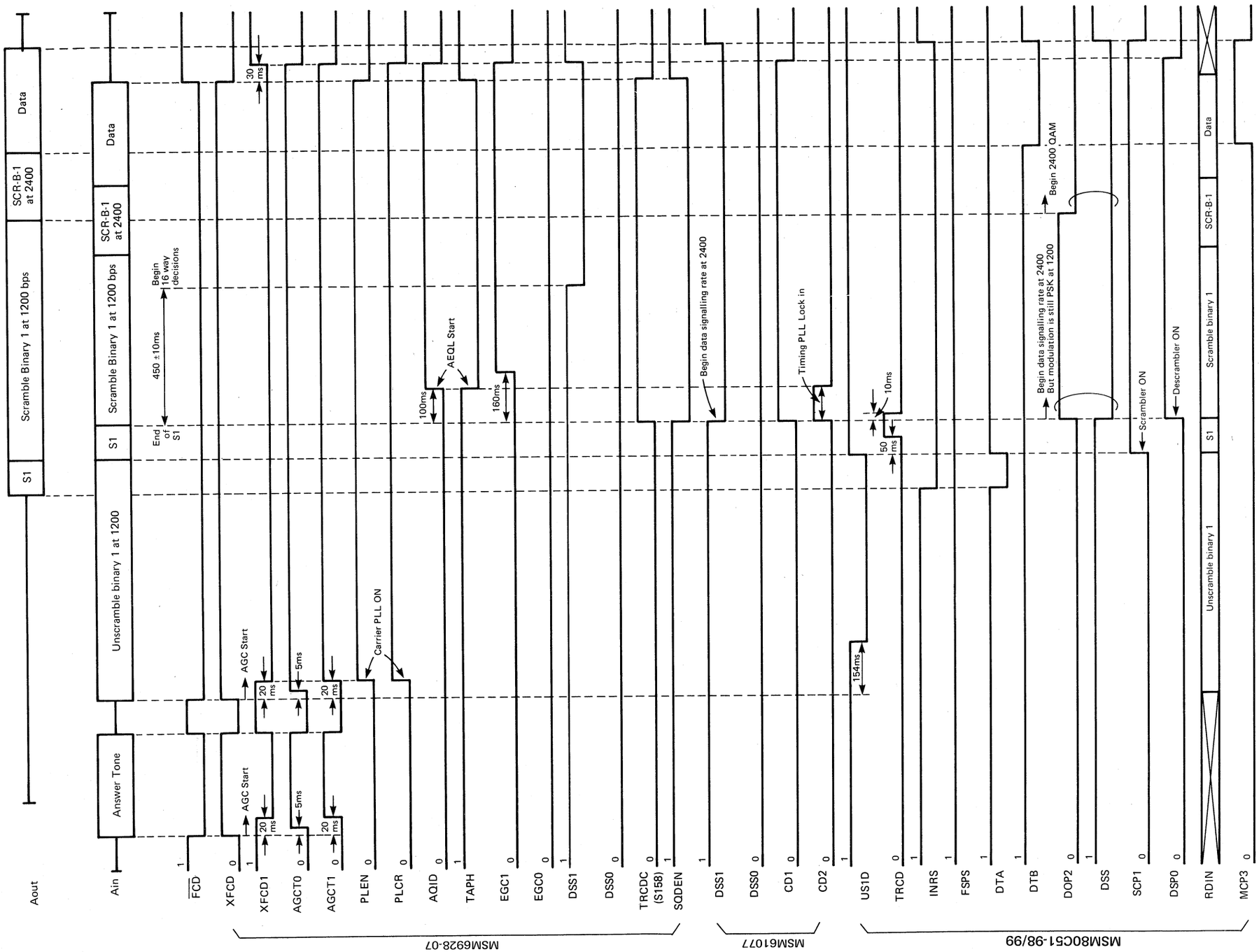


Figure 7 CCITT 2400 bps (Originate)

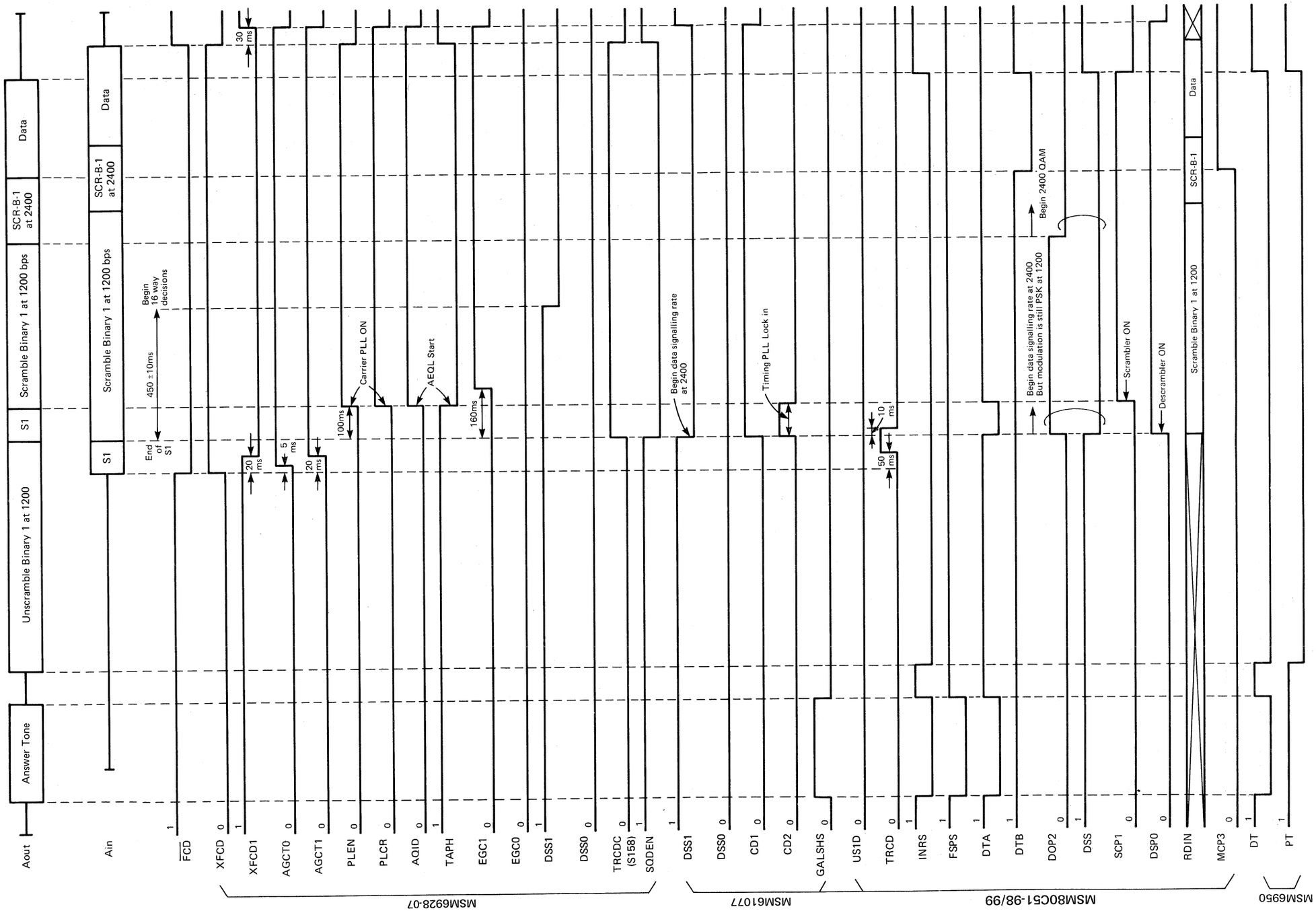


Figure 8 CCITT 2400 bps (Answer)

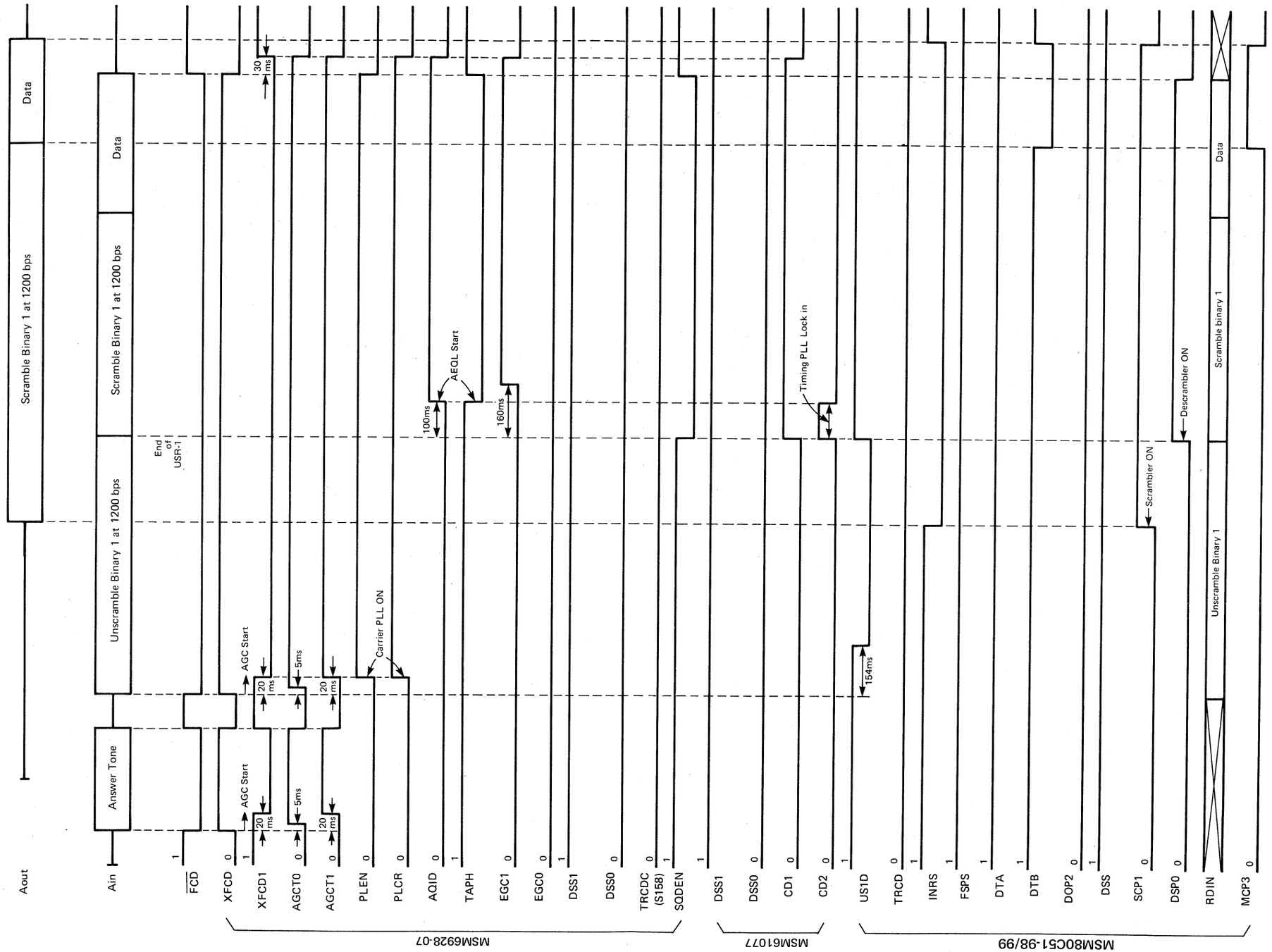


Figure 9 CCITT 1200 bps (Originate)

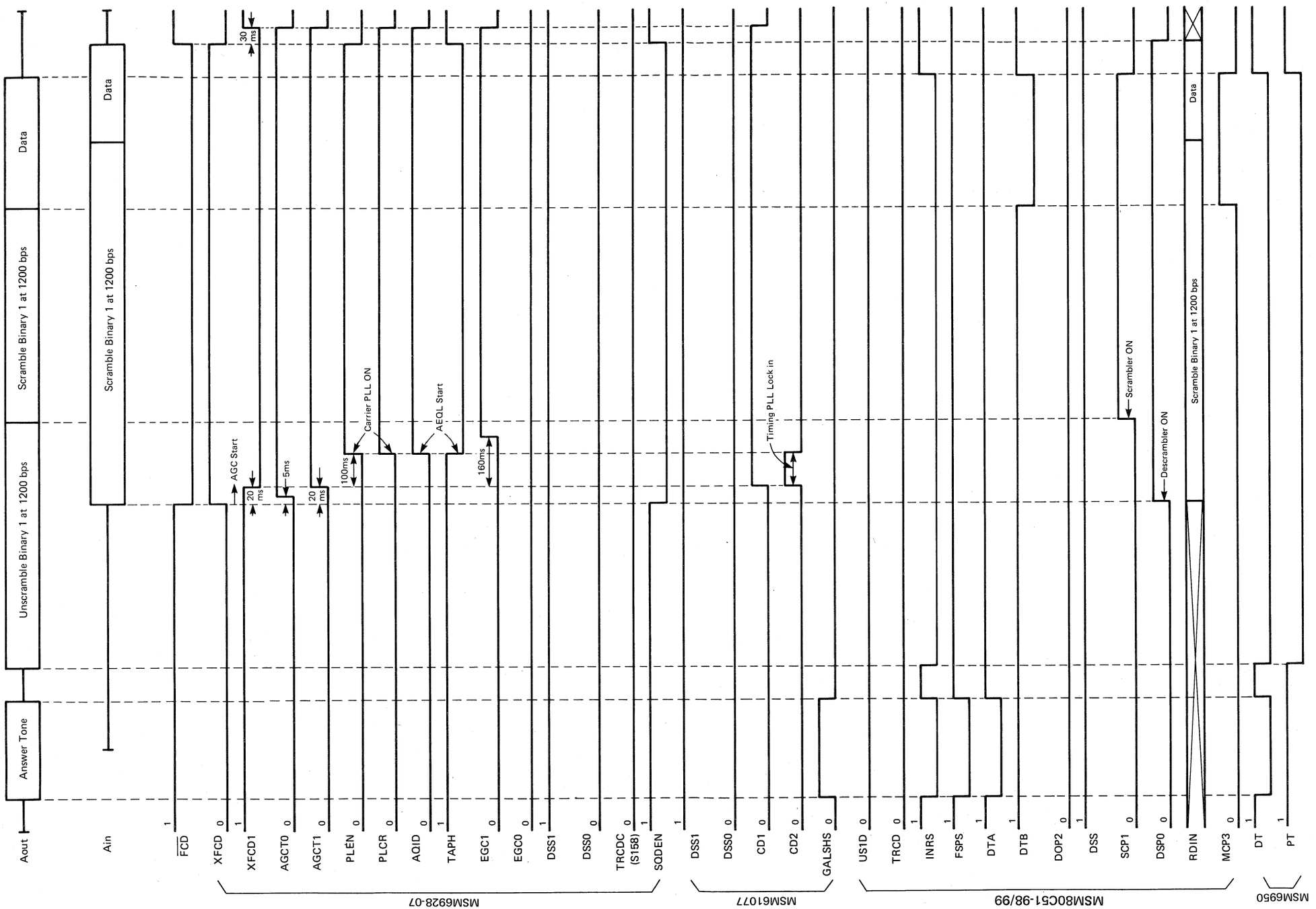


Figure 10 CCITT 1200 bps (Answer)

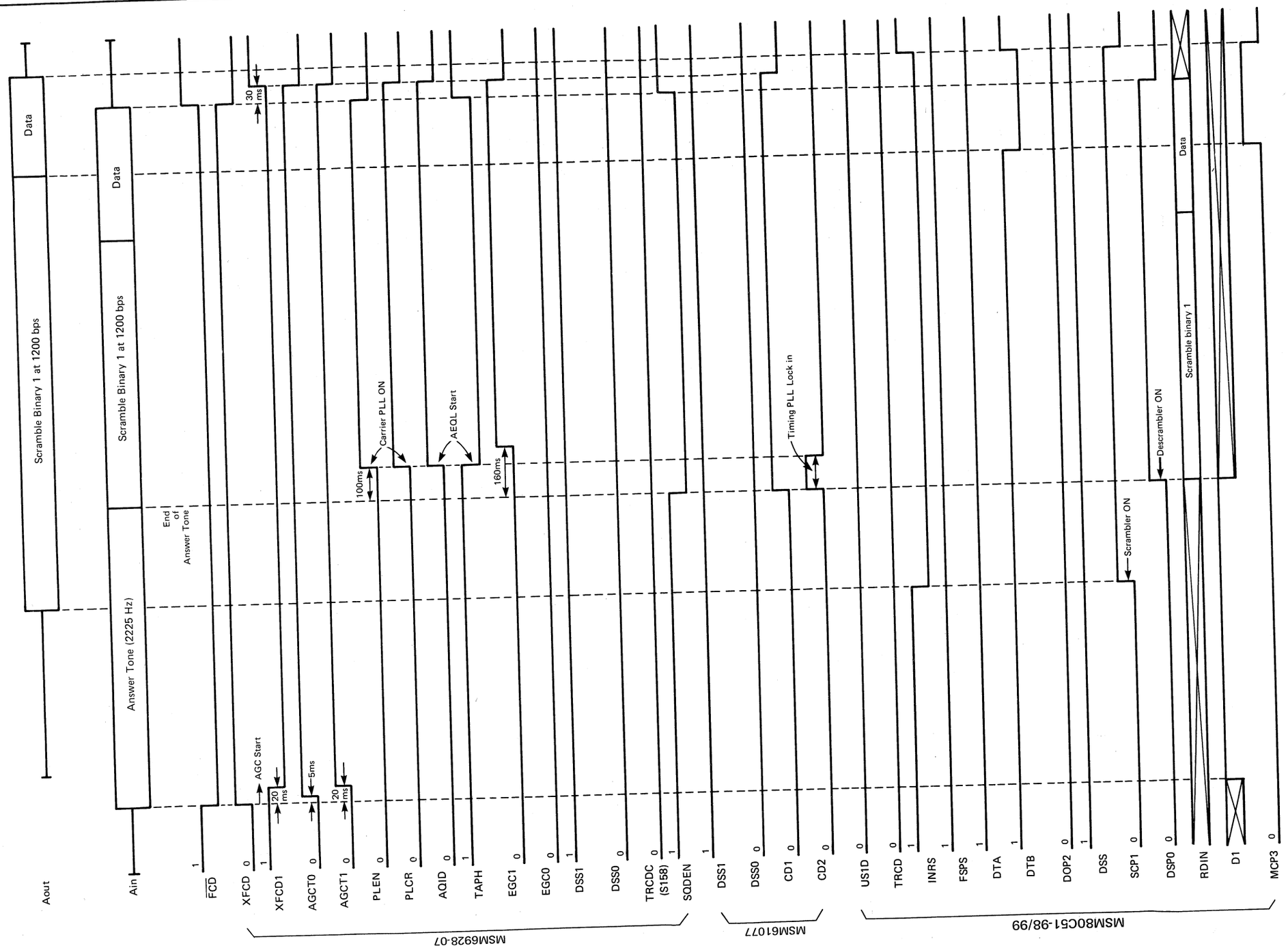
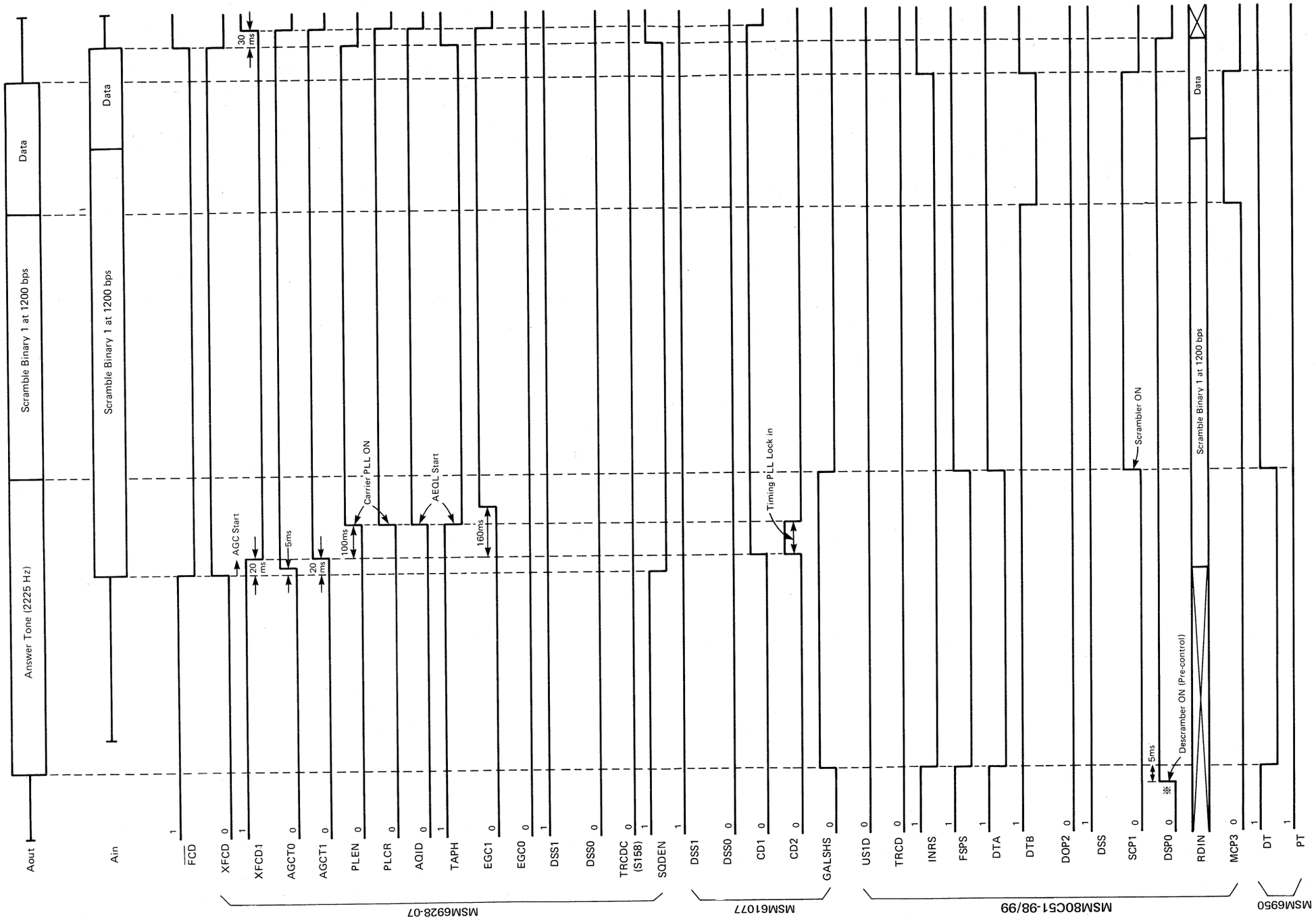
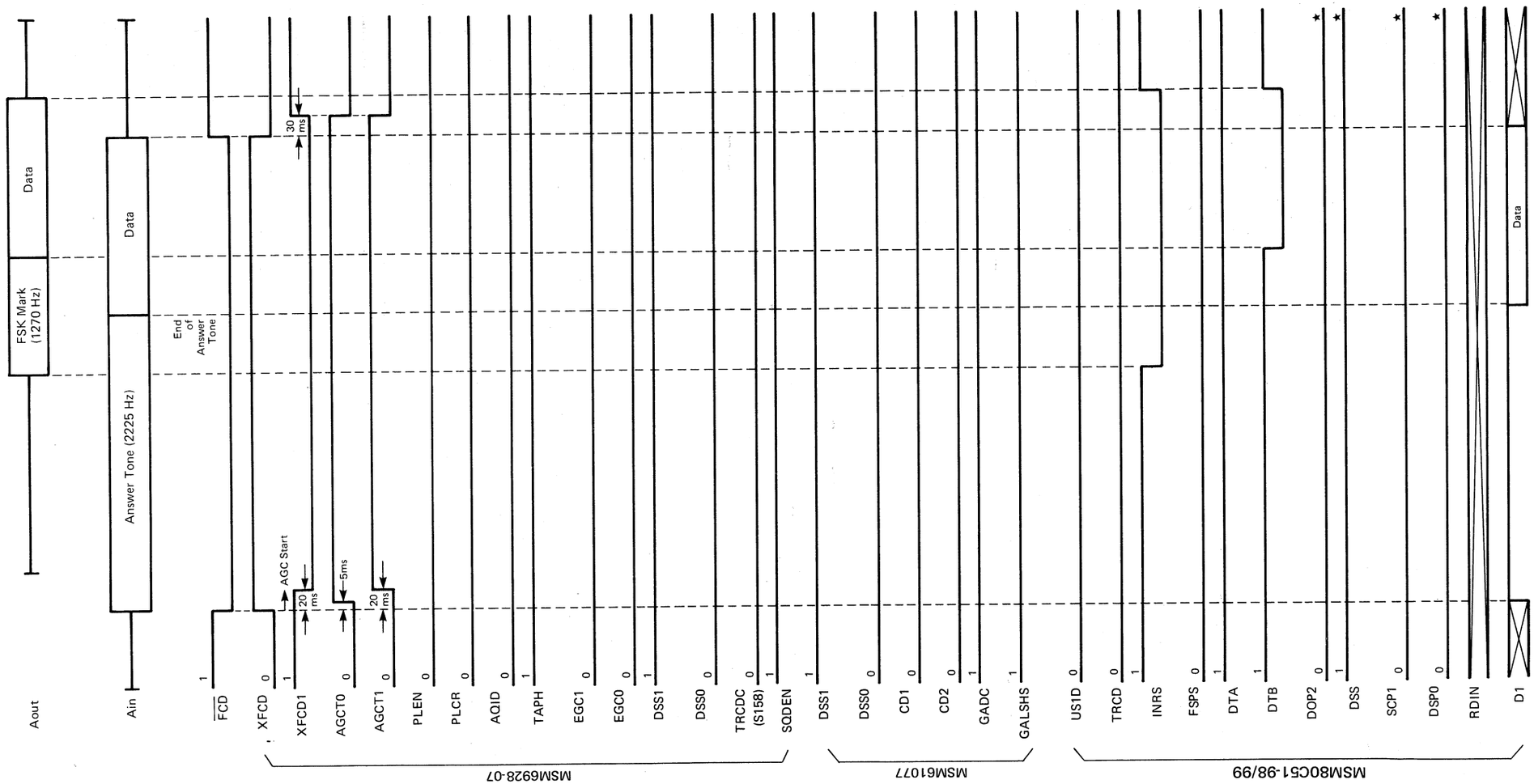


Figure 11 BELL 1200 pbs (Originate)



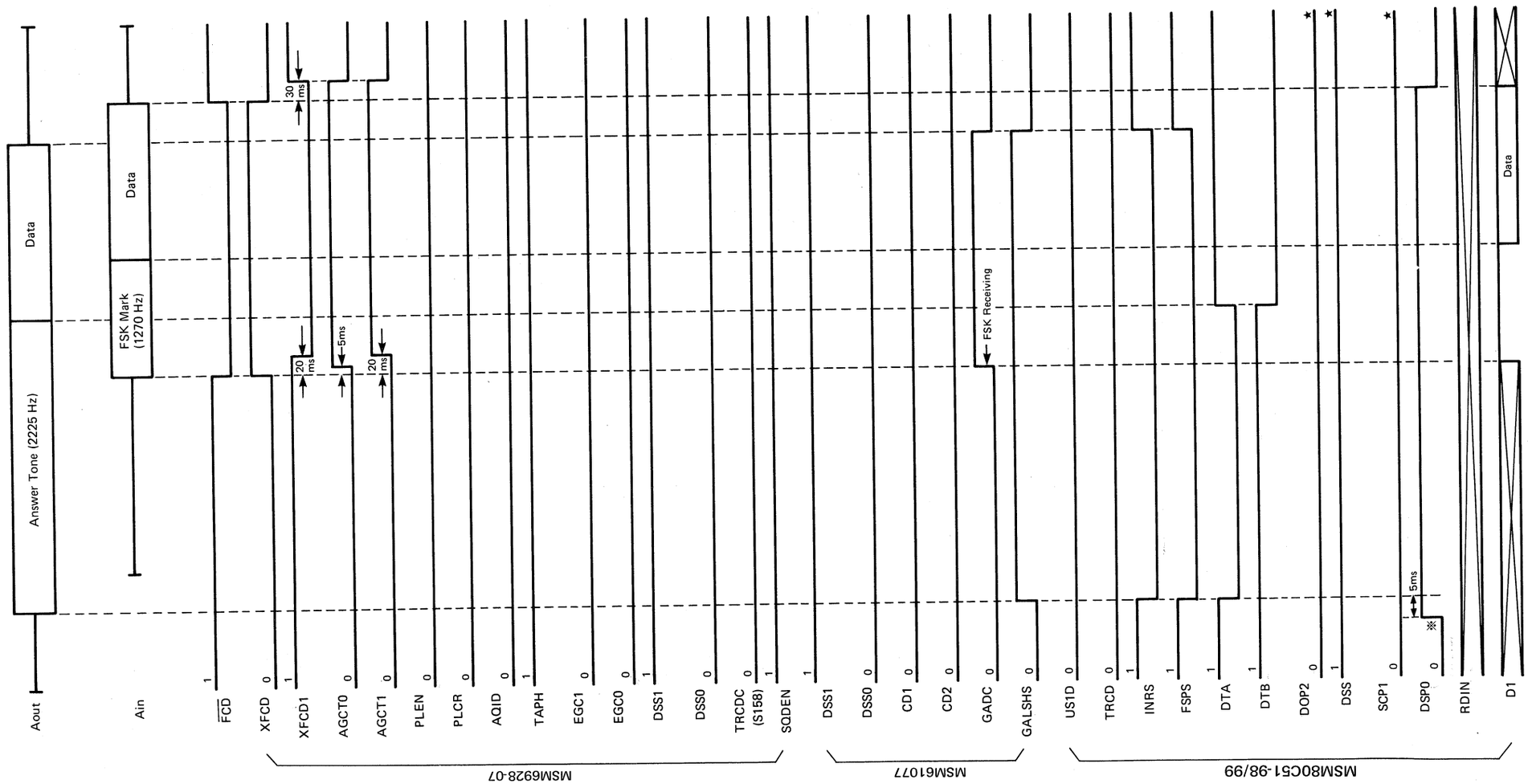
* Since descrambler control of DSP0 will be disabled while transmitting Answer Tone (FSPS=0), DSP0 should be set on High before FSPS goes Low.
This pre-control of DSP0 allows descrambler to be enabled (descrambler ON).

Figure 12 BELL 1200 bps (Answer)



★ This status doesn't be cared.

Figure 13 BELL 300 bps (Originate)



* Pre-control of DSP0 for descrambler (When orig. modem declares 300 bps, this pre-control shall be insignificant.).
★ This status doesn't be cared.

Figure 14 BELL 300 bps (Answer)

CONTROLLER FOR COMMAND INTERPRETTING AND HANDSHAKE SEQUENCING, PHONE LINE INTERFACE

The chip set provides only the original MODEM functions as described, therefore, it is necessary to implement the controller with software, some network control circuit and phone line interface.

Figure 6 (Application circuit) includes only the original MODEM functions, and does not show the additional functions which are required to realize the stand-alone MODEM.

Figure 15 shows one example of the block diagram for it.

OKI wishes to support customers for the design of the whole modem, and intends to provide an example of the controller and command interpretter with software.

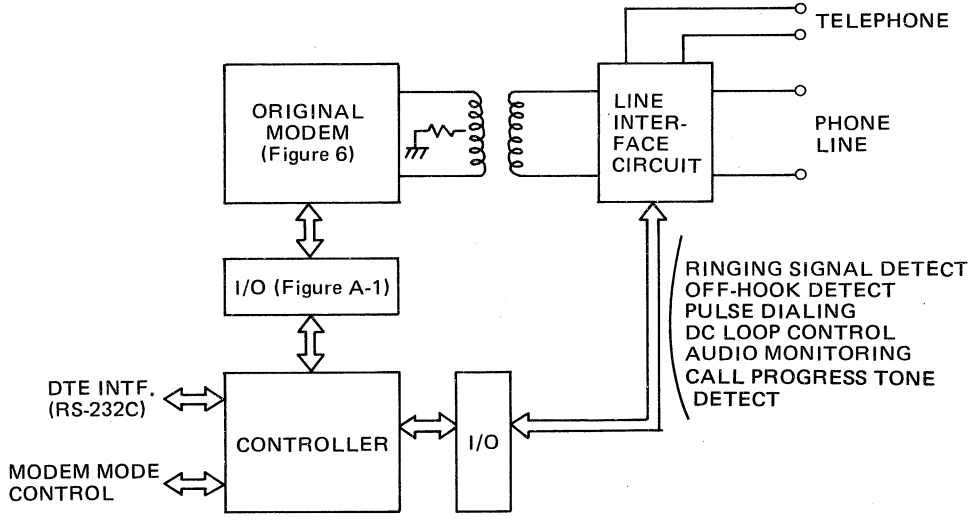


Figure 15 Intelligent MODEM block diagram

III

APPENDIX A

Figure A-1 shows the example of the interface circuit between the controller and the OKI PC MODEM 224. The main function of this circuit is to convert the serial bits stream into the parallel bits stream. MSM82C55 acts as to expand the output port of the controller, that is 1 byte to 3 bytes. And some gates, latch (HC574F) are auxilialy prepared to supply the diagnostic signals (TRCD, US1D, ... etc) to the controller.

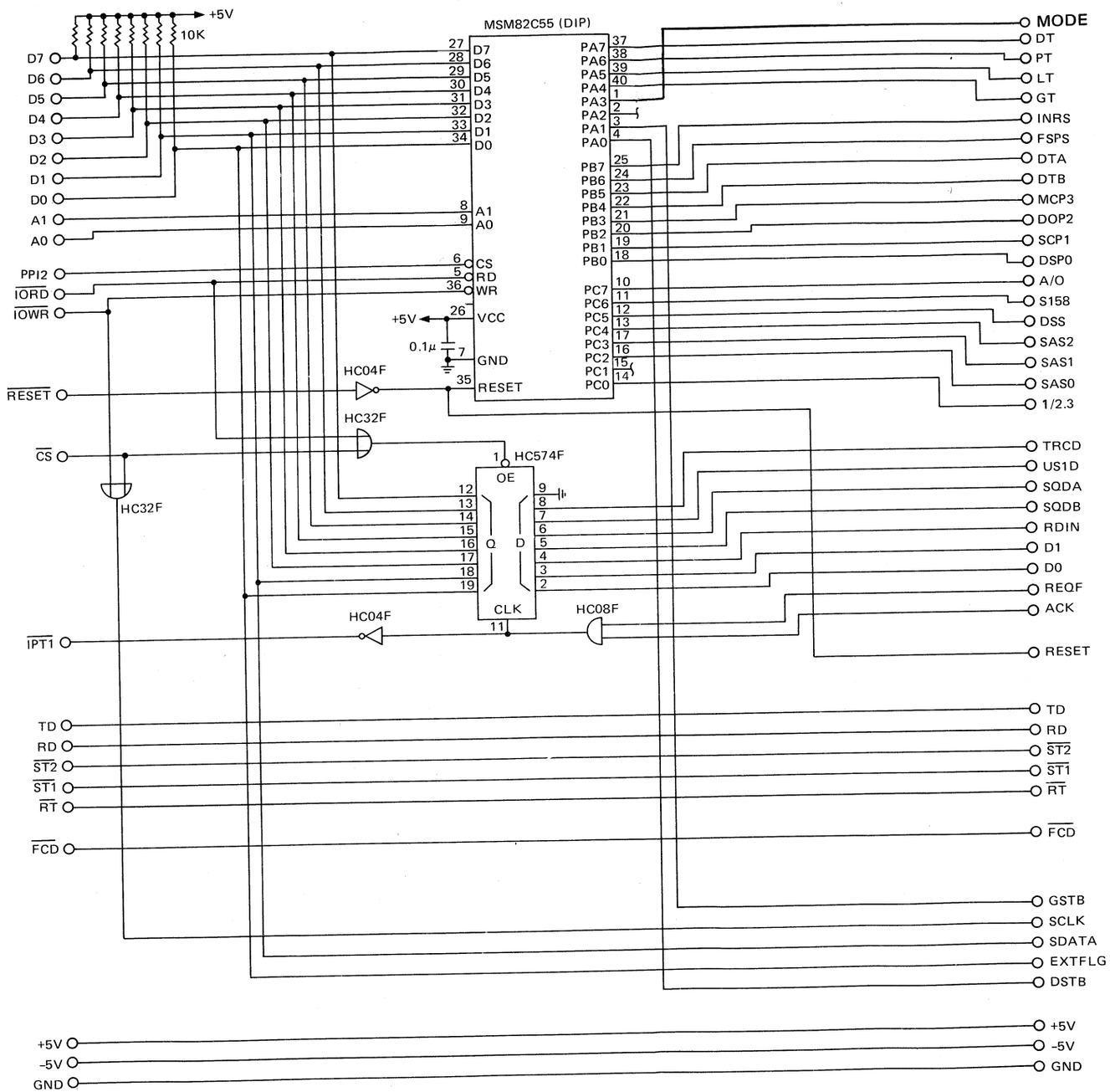


Figure A-1 An example of the interface circuit between OKI PC MODEM 224 and controller

APPENDIX B

Figure B-1 shows the functional block diagram of the demodulator (MSM6928-07).

In many cases, the demodulator functions are masked and uncontrollable, therefore, their performance largely depends on the chip itself. In case of the OKI PC MODEM 224, however, some blocks in the Fig. B-1 are controllable and adjustable to adapt the demodulating environment with flexibility, so that the demodulation performance, that is the convergence ability of the adaptive equalizer, or bit error rate, could be improved.

The OKI PC MODEM 224 allows the following functions to be controllable and adjustable.

1) AGC Control
2) Signal Quality Detector
3) Carrier PLL
4) Adaptive Equalizer

Items of 1), 2), 4) are described in details as follows.

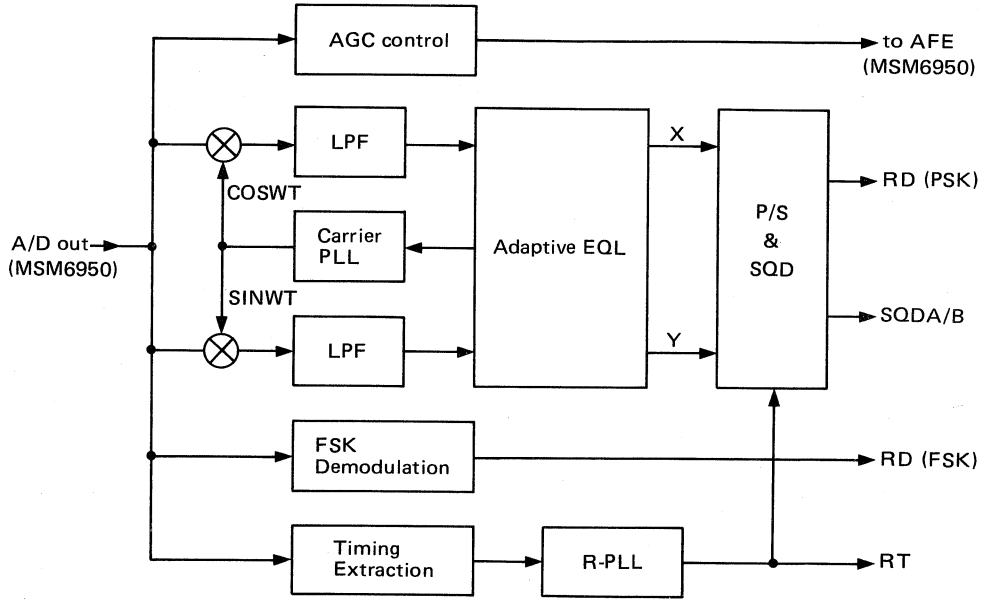


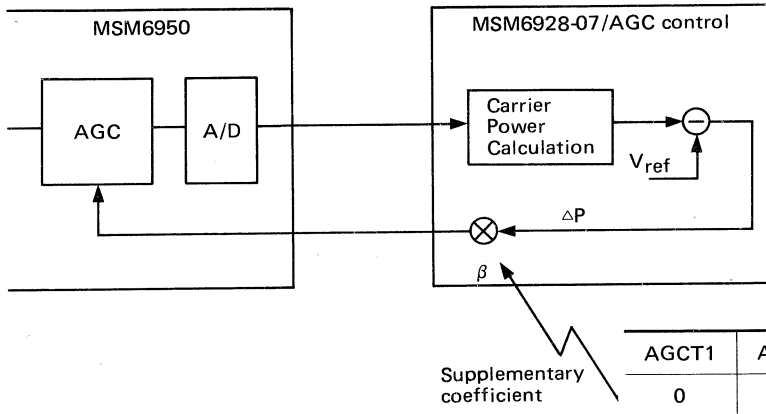
Figure B-1 Functional block diagram of demodulator

(i) AGC Control

Figure B-2 shows the schematic explanation of the AGC control given to the AFE through DSP output port. These control are done by the following processes.

1) Calculating the carrier power of the present input signal.
2) Comparing the power value with the predetermined reference value (Vref).
3) Feeding the subtracted value back to the AFE.

When the FCD (carrier detection) turn OFF to ON, the error value is immediately fed back to the AFE to chase the input signal. But, when the input carrier level become into the steady, we had not better control the error value frequently because DSP could follow the carrier deviation sensitively even though it might be the instant carrier loss or its ripple. Therefore, the feed back quantity should be decreased at that time. Beta 1-3 are supplementary coefficient multiplied by the error value, and selected by AGCT0-1 listed in the table.



AGCT1	AGCT0	β
0	0	β_1
0	1	β_2
1	0	β_3
1	1	

Note: $0 < \beta_3 < \beta_2 < \beta_1 < 1$

Figure B-2 AGC control

(II) Signal Quality Detector Output

DSP includes the self-diagnosis function for the demodulated signal quality as shown in the Fig. B-3. Both SQDA and SQDB are output results of its function. The error value of the area decision is passed through the digital lowpass filter with a large time constant as a integlator, the output of which is compared with the predetermined threshold level by the digital comparator.

The comparator-A compares the LPF output with Vr1, and outputs the result of SQDA, which means that the status of demodulator is no convergence when it turns to the logical High level. This information shall be used for the retrain requirement to the opposite modem.

The comparator-B compares the LPF output with Vr2 or Vr3, and outputs the result of SQDB. Either Vr2 or Vr3 is selected as the threshold level for comparator-B by the control signal of SQDC. The SQDB means that the bit error rate of the demodulator section might be seemed to overreach the rate of 10^{-3} or 10^{-4} when it turns to the logical High level.

Please note that the Vr2 and Vr3 which correspond to the preset rate of 10^{-3} and 10^{-4} respectively are experimental values so that there are some difference between a measurement value and a predictive value.

As mentioned before, the LPF has a large time constant, therefore, the internal accumulated register of LPF can be cleared by the SQDEM to avoid the large transient time responses.

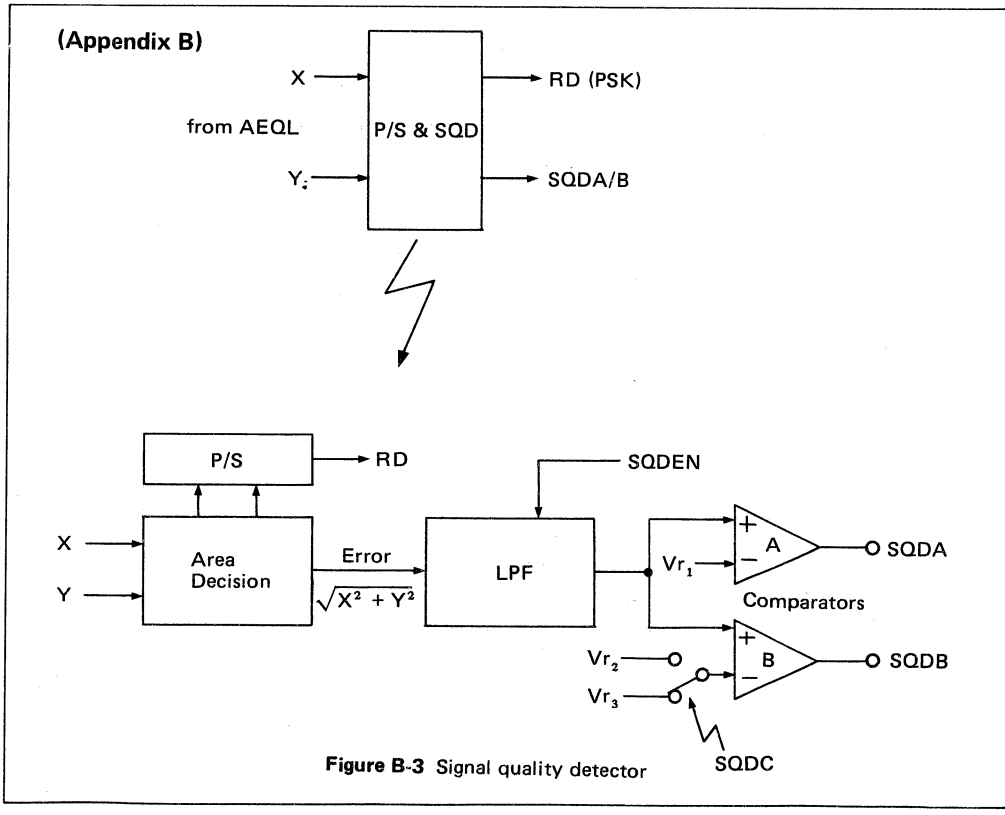
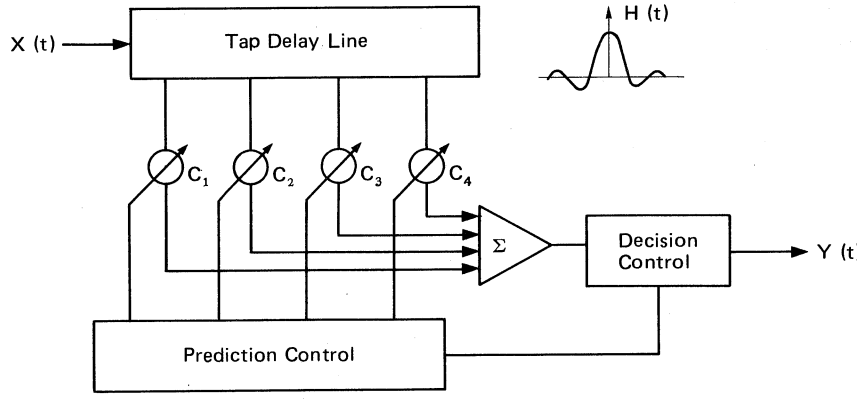


Figure B-3 Signal quality detector

(III) Adaptive Equalizer

In the demodulator, the adaptive equalizer takes an important charge of it on to determine its performance, and also has sophisticated functions. The OKI PC MODEM 224 adopts the MSE (Mean Square Error) method as the algorism of Adaptive Equalizer. Figure B-4 shows the schematic diagram of adaptive equalizer. When the FCD (carrier detection) turns OFF to ON, the adaptive equalizer begins to study the actual line condition in the training sequence, and determines the adaptive tap coefficients of the equalizer. At that time, to set the center value to tap coefficients of the equalizer (AQID = 0) would not only provide good convergence for demodulator speedy, but facilitate the following processes of equalizer algorism. And then, we should immediately renew the tap coefficients by adding or subtracting the error value. However, after the training sequence, we had not better change the tap coefficients frequently because Equalizer could follow the line environment changes sensitivity ever though it might be a little bit change caused by the frequency hit, jitter, or some other factors. Alpha 1~4 are supplementary coefficient multiplied by the error value, and selected by EGC0-1 listed in the table.



C_i (i = 1 ~ 4) ← $C_i + \alpha \cdot \triangle C_i$

Error value

Supplementary coefficient

Setting up center value (AQID = 0)

EGC1	EGC0	α
0	0	α_1
0	1	α_2
1	0	α_3
1	1	α_4

Note: $0 = \alpha_4 < \alpha_3 < \alpha_2 < \alpha_1 < 1$

Figure B-4 Adaptive equalizer

APPENDIX C
Initial Adjustment

Trimming for Reference Voltage

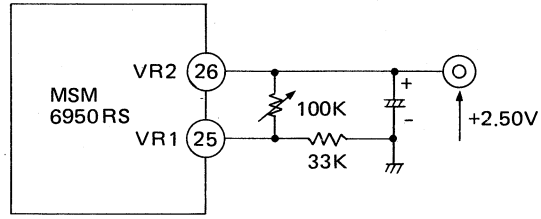


Figure C-1

VR2 should be trimmed so that the DC voltage on pin 26 becomes +2.50 V.

Adjustment for Transmit/Receive Signal Level

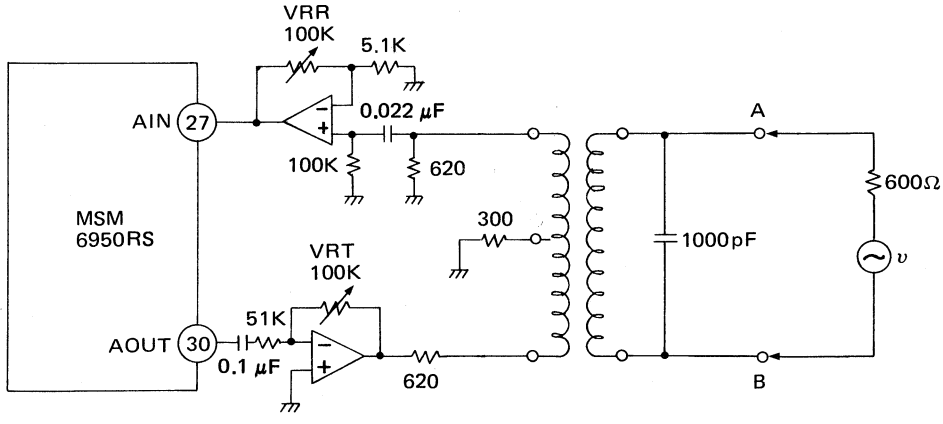


Figure C-2

First, connect a 600 Ω signal source to the transformer (normally 1200 Hz).

Next, make the signal source level minimum and make the modem send the single tone signal to the phone line through the hybrid transformer.

Then, tune VRT so that the signal between point A and B should become −10 dBm.

Stop the modem to send the transmit signal, and set the signal level between point A and B at −10 dBm by increasing the signal source output level.

Then, tune VRR so that the signal on AIN (pin 27) should be 0 dBm.

Note 1: 0 dBm = 0.775 Vrms
The input impedance of a level meter used for measurments must be "High".

Note 2: The mode of the level meter should be "Balance" when measuring the signal level between point A and B.
"Unbalance" mode should be used when measuring the signal level on AIN (pin 27), AOUT (pin 30).

APPENDIX D

Decision Point Monitoring

Decision point monitoring is the practical evaluation method.

It can be easily performed by using XIC provided on the evaluation board and the external monitoring circuit.

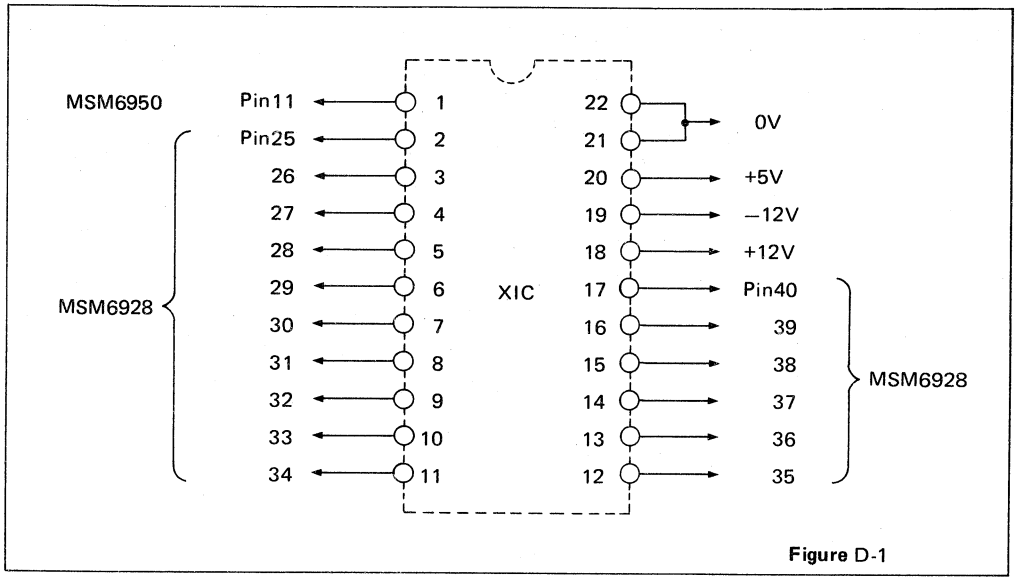


Figure D-1

At first, it is required to put a 22 pin – IC socket into XIC's holes by soldering.

Figure D-2 shows how to connect the external monitoring circuit (drawn in figure D-3) through the XIC's socket.

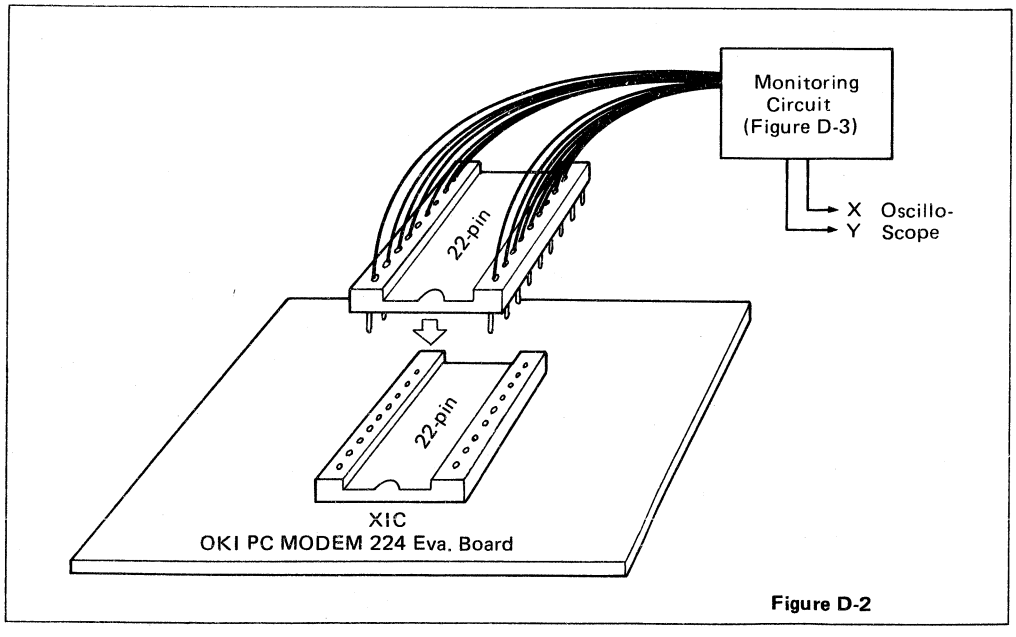


Figure D-2

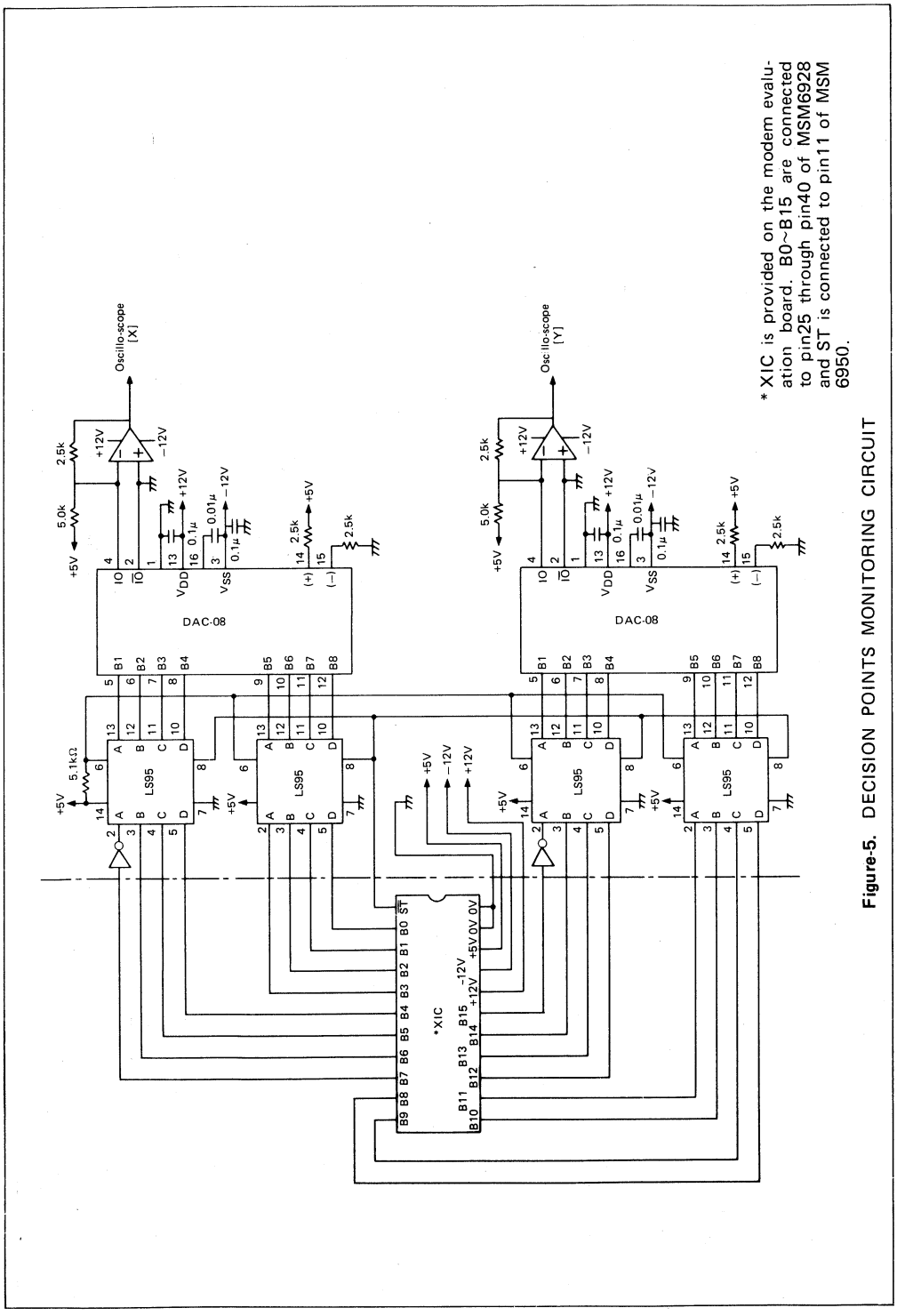


Figure-5. DECISION POINTS MONITORING CIRCUIT

APPENDIX E

The chip set does not include the carrier detect function, therefore, it is necessary to implement this function using discrete components.

Figure E-1 shows an example of carrier detect circuit. In this circuit, OPA 4½ requires the power supply voltages of more than ±9V. When using ±5V for operational amplifier, it is necessary to re-design this circuit, especially for the part of threshold detector with hysteresis constructed by OPA 4½.

For normall 2400 bps modem systems, it is difficult to apply ±5V as power supply voltages for line interface circuit. Because QAM modulated analog signal has the peak factor for the wave form and ±5V are too low to guarantee the linearity of the QAM analog signal. For 300 bps (FSK) and 1200 bps (PSK) modem systems, ±5V power supplies may be used for the line interface circuit. So, when the chip set is applied for 300 or 1200 bps systems and the power supply voltages are ±5V, the carrier detect circuit shown in Figure E-1 can not be applied without re-designning.

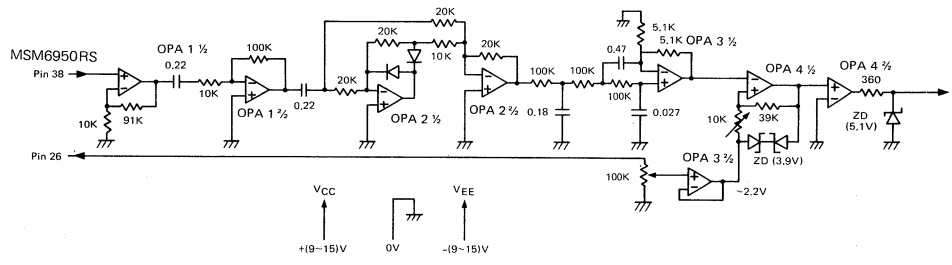


Figure E-1 An example of external carrier detect circuit

III

MSM6928-06

DSP FOR 1200 BPS FULL DUPLEX MODEM CHIP SET

GENERAL DESCRIPTION

The MSM6928-06 is a digital signal processor which is used as a demodulator in the chip for 1200 bps full duplex modem based on Bell 212A standard or CCITT V22 standard.

The MSM6928-06 operates as a PSK demodulator, FSK demodulator, FCD detector etc by using the digital signal processing method and it transmits the AGC signal to the MSM6950 (Analog Front End).

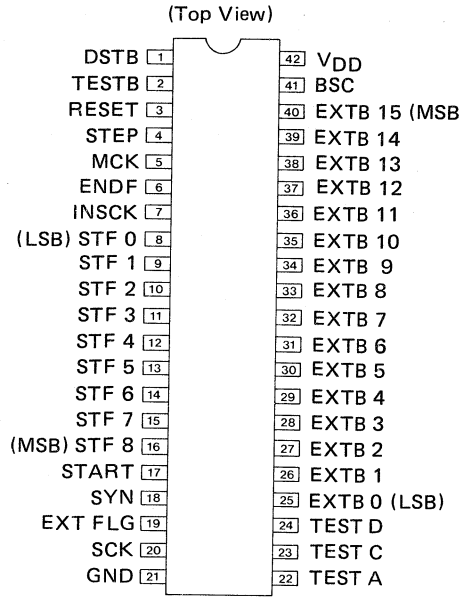
The MSM6928-06 is fabricated by OKI's low power consumption CMOS silicon gate technology. By utilizing MSM6928-06 together with MSM6950, MSM80C31 (Modulator), MSM61057 (Asynchronous/Synchronous Switching, etc.), MSM81C55 and MSM2764 (or MSM27C64), an intelligent modem system based on Bell 212A or CCITT V.22 standard can be realized easily.

FEATURES

- PSK Demodulation
  The received signal is multiplied with an internal demodulation carrier, and input to the next stage PDF, as a baseband signal. The PDF output is generated as the demodulated PSK-RD after the line distortion, is corrected by an automatic equalizer.
- FSK Demodulation
  The received signal is demodulated through a BPF, a delay detector, and an LPF, and then output as FSK-RD.
- FCD Detection
  In the FCD detection block, the level of the input signal is calculated and compared with a threshold level. The detection result is output as FCD.
- AGC
  In the AGC block, the power of the input signal is calculated and its difference from the reference voltage is output as the control signal for the Analog-Front-End variable control.
- 42 pin plastic DIP package or 60 pin plastic flat package.

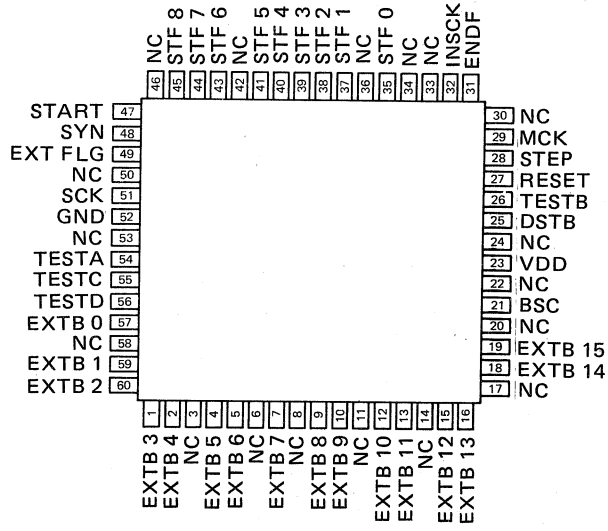
PIN CONFIGURATION

MSM6928-06RS



42 pin DIP package

MSM6928-06GS



60 pin FLAT package

III

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Item	Symbol	Rating	Unit	Remark
Power Supply Voltage	V_{DD}	-0.3 ~ +7	V	
Input Voltage	V_{IN}	-0.3 ~ V_{DD}	V	
Power Dissipation	Pd	1.0	W	
Operating Temperature Range	Top	-10 ~ +70	°C	
Storage Temperature Range	TsT	-55 ~ +150	°C	

Guaranteed Operating Range

Item	Symbol	Rating	Unit	Remark
Power Supply Voltage	V_{DD}	+4.75 ~ 5.25	V	
Ambient Temperature Range	Ta	0 ~ +60	°C	

Static Electrical Characteristics

V_{DD} = 5 V ±5%, Ta = 0 ~ 60°C

Item	Symbol	Condition	Limit			Unit	Remark
			Min	Typ	Max		
Output Voltage	V_{OH} V_{OL}	I_Q = -40 μA I_Q = 1.6 mA	4.2 -0.3	–	V_{DD} 0.4	V	–
Input Voltage	V_{IH} V_{IL}	–	2.4 -0.3	–	V_{DD} 0.8	V	–
Input Leakge Current	I_{IL}	GND < V_{IN} < V_{DD}	–	–	±10	μA	–
Bus Output Voltage	BV_{OH} BV_{OL}	I_Q = -80 μA I_Q = 1.6 mA	4.2 –	–	– 0.4	V	–
Bus Input Voltage	BV_{IH} BV_{IL}	–	2.4 –	–	– 0.8	V	–
Bus Input Leakage Current	B_{IL}	GND < V_{IN} < V_{DD}	–	–	±10	μA	@ BUS OFF Condition
Operating Current	I_{DDQ}	–	–	35	40	mA	MCK: 5529.6 kHz
Quiescent Current	I_{DDS}	–	–	–	0.3	mA	MCK: OFF

Dynamic Electrical Characteristics

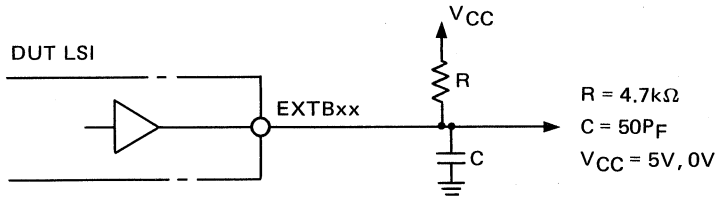
Item	Symbol	Condition	Limit		Unit	Remark
			Min	Max		
BSC-EXTB						
Delay Time	TD	Timing Chart A	–	200	ns	Common to EXTB 0 ~ EXTB 15
Rise Time	TR		–	100		Refer to Figure 1
Fall Time	TF		–	100		
DSTB-EXTB						
Pusle Width	T_W	Timing Chart B	300	–	ns	Refer to Figure 1
Setup Time	T_{SET}		100	–		
Hold Time	T_{HOLD}		100	–		
SCK-SIN						
Pulse Width	T_W	Timing Chart C	180	–	ns	Refer to Figure 2
Setup Time	T_{SET}		100	–		
Hold Time	T_{HOLD}		100	–		
SCY-SYN						
Pulse Width	T_W	Timing Chart D	180	–	ns	Refer to Figure 2
Setup Time	T_{SET}		100	–		
Hold Time	T_{HOLD}		100	–		
START-START FLAG						
Pulse Width	T_W	Timing Chart E	1300	–	ns	Refer to Figure 3
Setup Time	T_{SET}	MCK = 5529.6 kHz $\pm 1 \times 10^{-4}$	100	–		
Hold Time	T_{HOLD}		100	–		
MCK						
Rise Time	TR	Timing Chart F	–	30	ns	Refer to Figure 3
Fall Time	TF_1		–	30		
Duty Ratio	T1/T2		95	105	%	
Frequency	FM		5529	5530	kHz	

III

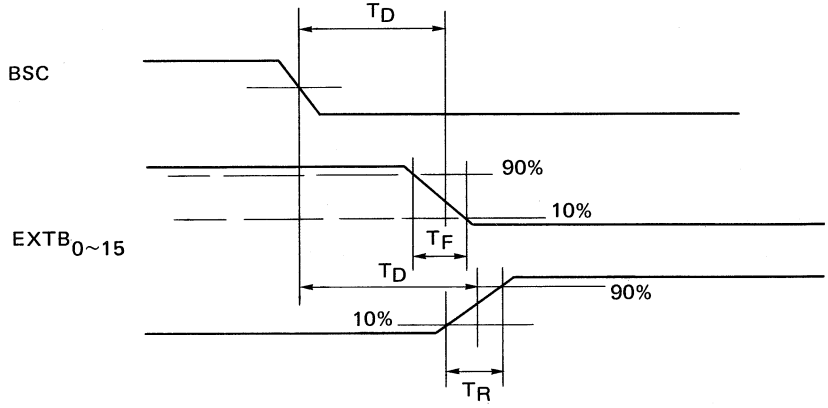
PIN DESCRIPTION

Pin Name	Pin No.		I/O	Function
	RS	GS		
DSTB	1	25	IN	Loads the signal on EXT Bus into Input Register. ⌐↑
TESTB	2	26	IN	Test signal. Loads the signal on internal bus into Output Register. 1: Load, 0: Normal
RESET	3	27	IN	Operation start instruction signal. Operation in synchronization with ⌐↑ 1: Stop, 0: Operation start
STEP	4	28	IN	Selects either of continuous operation and single step operation. 1: Continuous operation (Normal) 0: Single step operation
MCK	5	29	IN	Master clock signal, normally 5529.6 kHz.
ENDF	6	31	OUT	Program specifying sync signal.
INSCK	7	32	OUT	Machine cycle sync signal.
STF 0	8	35	IN	External specifying address signal 2^0 (LSB)
STF 1	9	37	IN	External specifying address signal 2^1
STF 2	10	38	IN	External specifying address signal 2^2
STF 3	11	39	IN	External specifying address signal 2^3
STF 4	12	40	IN	External specifying address signal 2^4
STF 5	13	41	IN	External specifying address signal 2^5
STF 6	14	43	IN	External specifying address signal 2^6
STF 7	15	44	IN	External specifying address signal 2^7
STF 8	16	45	IN	External specifying address signal 2^8 (MSB)
START	17	47	IN	Operation starting sync signal. Loads external specifying address.
SYN	18	48	IN	Causes the serially input jump condition to be loaded into EXT FLG Register in the parallel form.
EXT FLG	19	49	IN	Serially input jump condition. This signal is loaded into S/P on the negative-going edge of SCK.
SCK	20	51	IN	Serially input jump condition loading clock.
GND	21	52	—	Ground.

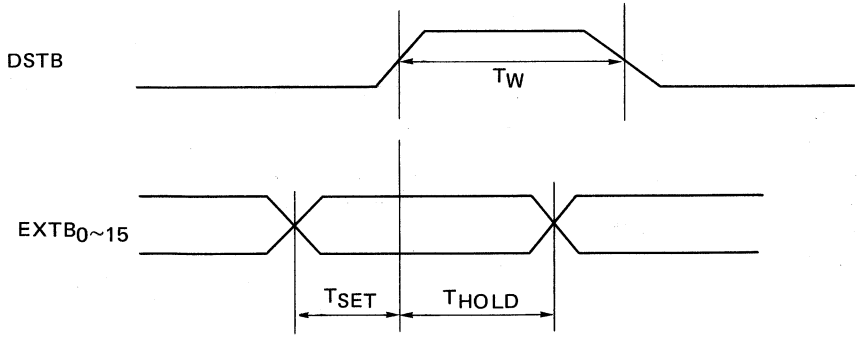
Pin Name	Pin No.		I/O	Function
	RS	GS		
TESTA	22	54	IN	Test signal. Holds Program Counter. 0: Hold, 1: Normal
TESTC	23	55	IN	Test signal.
TESTD	24	56	IN	Test signal.
EXTB 0	25	57	I/O	External bidirectional bus 2^0 (LSB)
EXTB 1	26	59	I/O	External bidirectional bus 2^1
EXTB 2	27	60	I/O	External bidirectional bus 2^2
EXTB 3	28	1	I/O	External bidirectional bus 2^3
EXTB 4	29	2	I/O	External bidirectional bus 2^4
EXTB 5	30	4	I/O	External bidirectional bus 2^5
EXTB 6	31	5	I/O	External bidirectional bus 2^6
EXTB 7	32	7	I/O	External bidirectional bus 2^7
EXTB 8	33	9	I/O	External bidirectional bus 2^8
EXTB 9	34	10	I/O	External bidirectional bus 2^9
EXTB 10	35	12	I/O	External bidirectional bus 2^{10}
EXTB 11	36	13	I/O	External bidirectional bus 2^{11}
EXTB 12	37	15	I/O	External bidirectional bus 2^{12}
EXTB 13	38	16	I/O	External bidirectional bus 2^{13}
EXTB 14	39	18	I/O	External bidirectional bus 2^{14}
EXTB 15	40	19	I/O	External bidirectional bus 2^{15} (MSB)
BSC	41	21	IN	External bidirectional bus specifying signal. 1: Input, 0: Output
V_{DD}	42	23	—	Power supply +5 V



Loading Condition

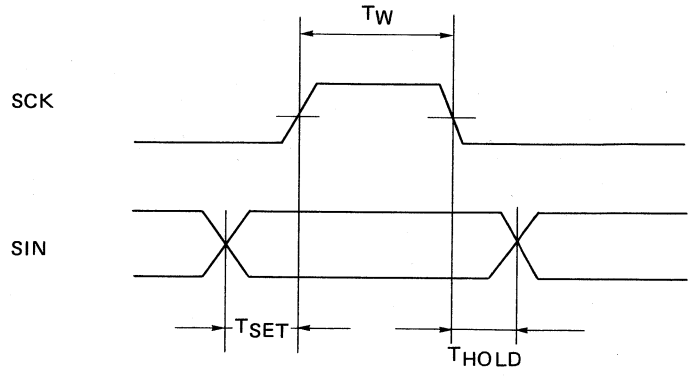


Timing Chart A

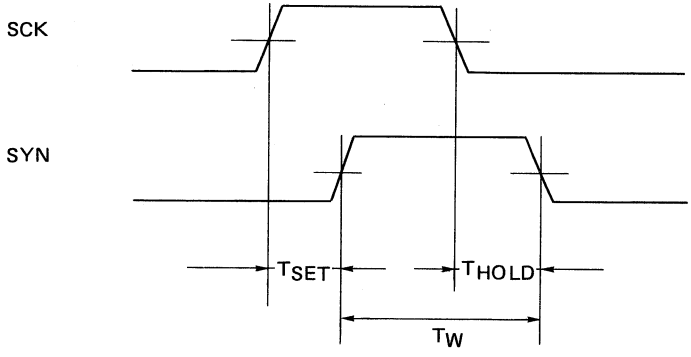


Timing Chart B

Figure 1 Test conditions and timing charts

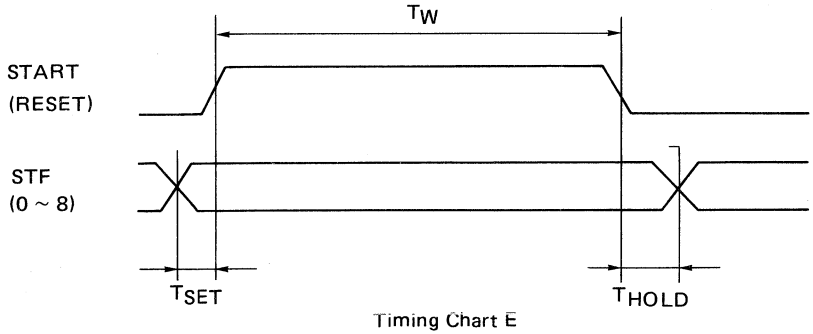


Timing Chart C

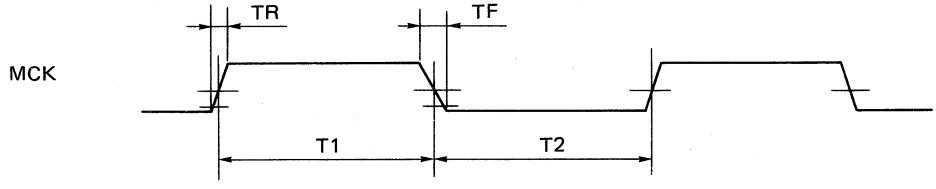


Timing Chart D

Figure 2 Test conditions and timing charts



Timing Chart E



DUTY = T1/T2

Timing Chart F

Note: The test pin conditions are shown below.

No.	Pin Name	Pin No.	Set Condition
1	TEST A	22	High
2	TEST B	2	Low
3	TEST C	23	High
4	TEST D	24	High
5	STEP	4	High

Figure 3 Test conditions and timing charts

MSM6928-06 APPLICATION

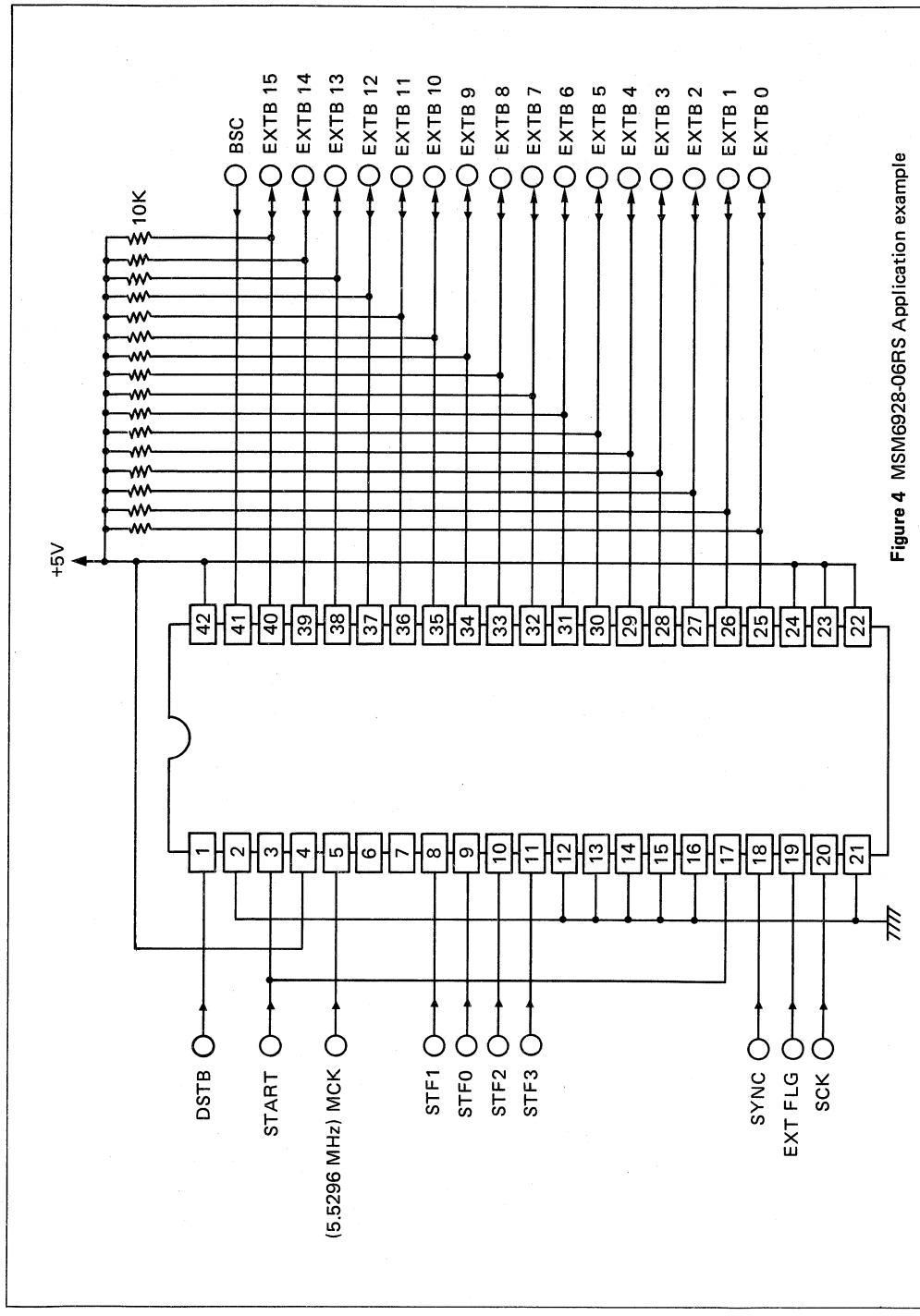


Figure 4 MSM6928-06RS Application example

III

TIMING CHARTS

Input/Output Data

Demodulating data (A/D output) and gain setting data for AGC are input and output via the bus every sampling period (STM). See Figure 5 and Figure 6.

Control Signals

Each baud rate (BTM) is divided into 12 (1 BTM = 12 STMs), and the start vectors are input from STF0-3 every STM. See Figure 7.

Mode specifications, such as data speed, ORG/ANS switching, and FCD selection, are input as 8-bit serial data. See Figure 8.

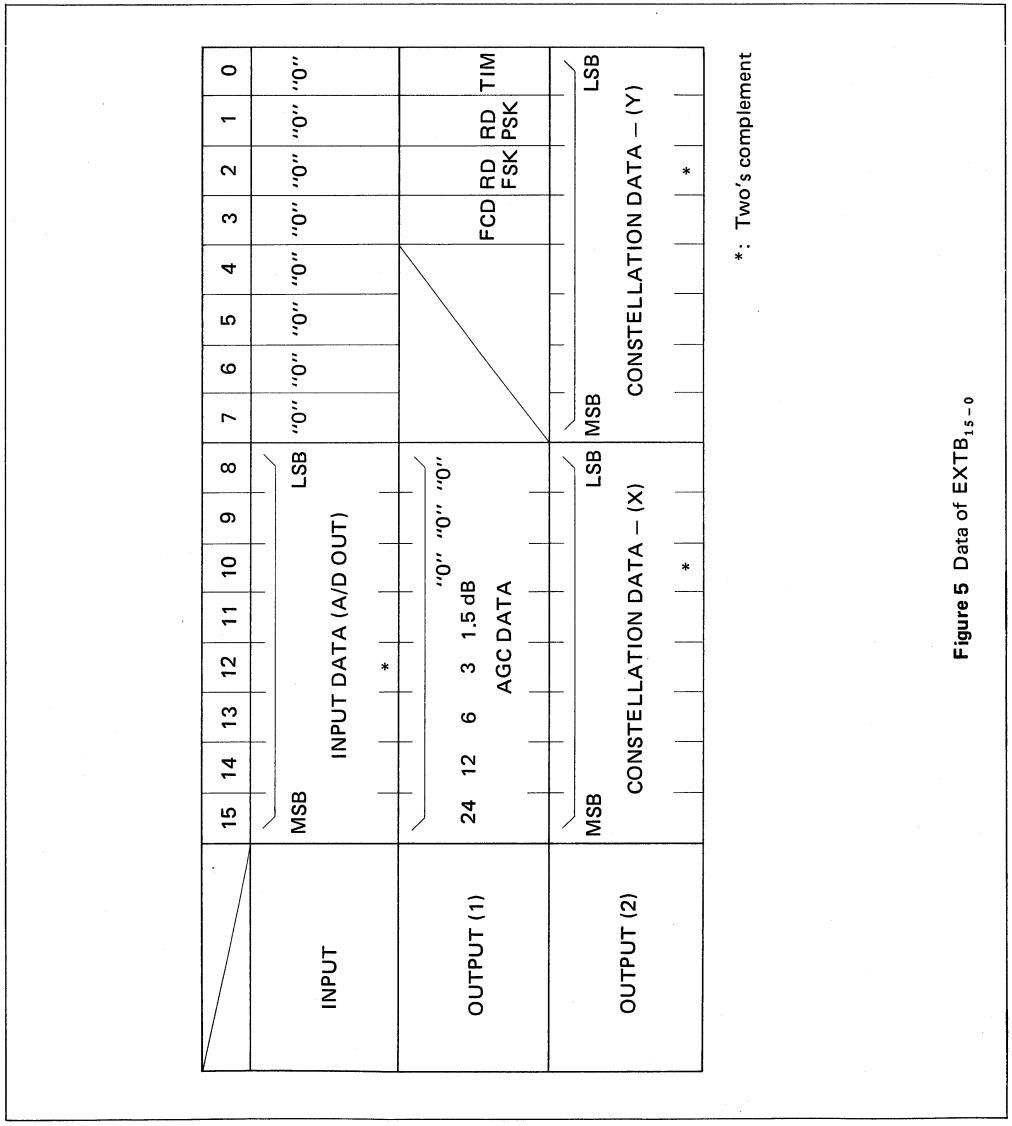


Figure 5 Data of $EXTB_{15-0}$

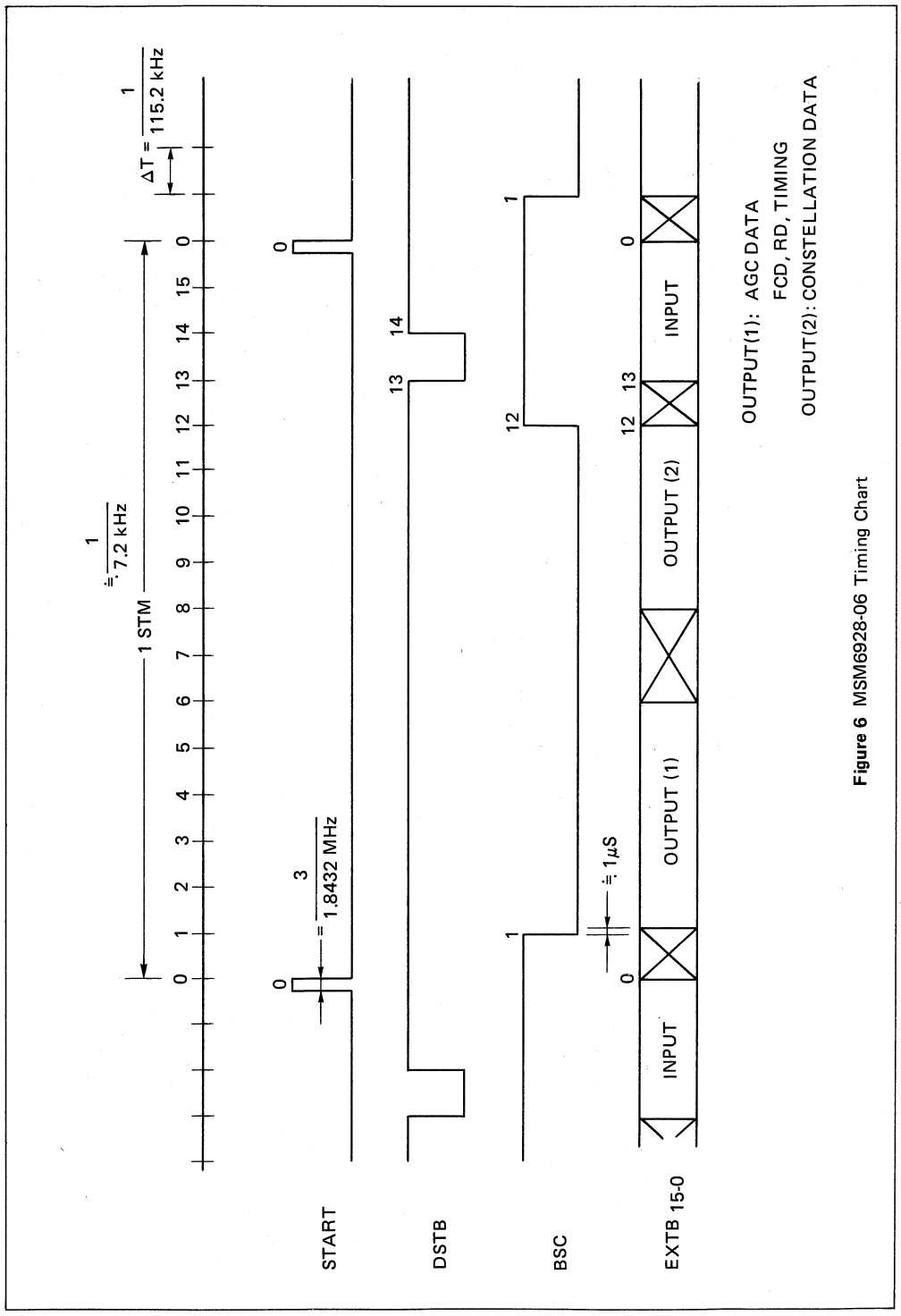


Figure 6 MSM6928-06 Timing Chart

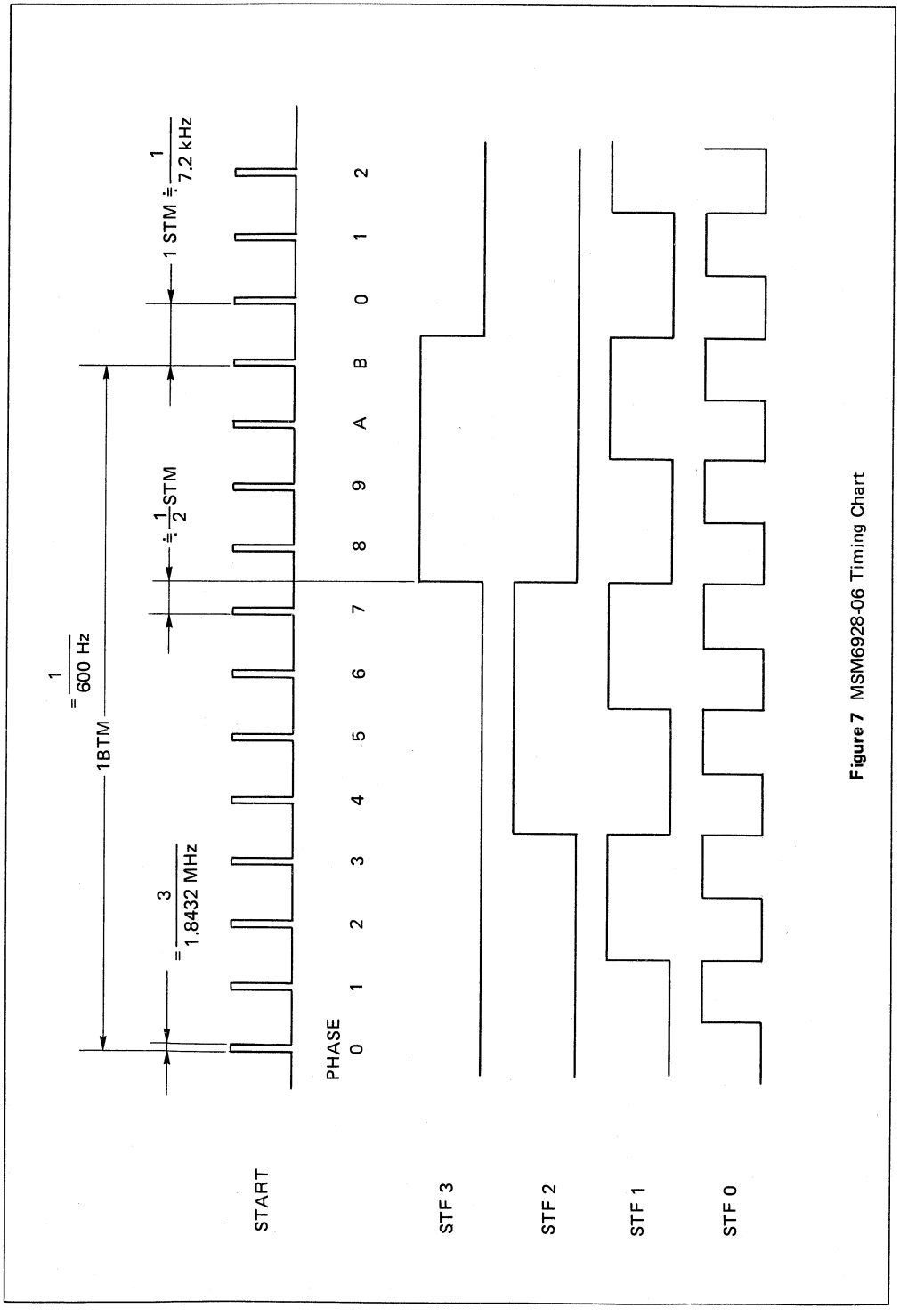


Figure 7 MSM6928-06 Timing Chart

	EXT FLG	Function	
D7~15	–	ANY	
D6	–	1: FIX	
D5	EXT-FCD	1: ON	0: OFF
D4	FCD SELECT	1: EXT-FCD	0: INT-FCD
D3	DATA SPEED	1: 600 bps	0: 1,200 bps
D2	A-EQL	1: OFF	0: ON
D1	FCD DETECT LEVEL	1: -35 dBm	0: -40 dBm
D0	ORG/ANS	1: ORIGINATE	0: ANSWER

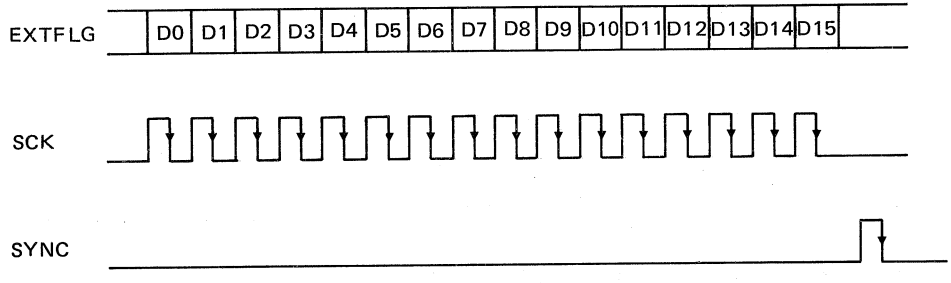


Figure 8 MSM6928-06 Timing Chart

MSM61057

GATE ARRAY FOR 1200 BPS FULL DUPLEX MODEM CHIP SET

GENERAL DESCRIPTION

The MSM61057 is a gate array LSI which is used in the chip set for 1200 bps full duplex modem based on Bell 212A or CCITT V. 22 standard.

The MSM61057 plays a role for asynchronous/synchronous converting, scrambler and descrambler in the 1200 bps full duplex modem system.

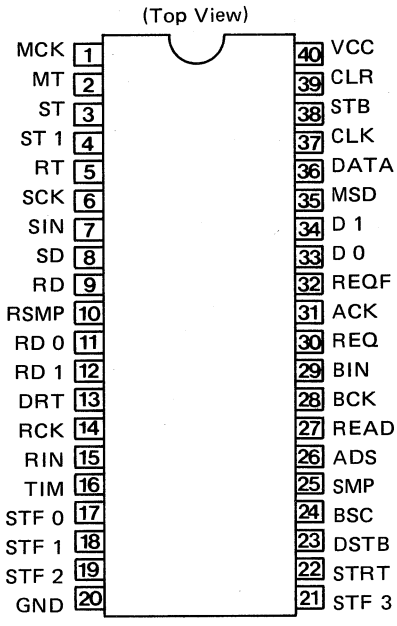
The MSM61057 is fabricated by OKI's low power consumption CMOS silicon gate technology. By utilizing MSM61057 together with MSM6928-06 (Digital Signal Processor – DSP used for Demodulator). MSM6950 (Analog Front End – AFE), MSM80C31 (Modulator), MSM81C55 and MSM2764 (or 27C64), an intelligent modem system based on Bell 212A or CCITI V. 22 standard can be realized easily.

FEATURES

- S. PLL:
  Built-in a Digital PLL for Transmit-Timing (ST). ST is output from this PLL in the synchronous mode.
- R. PLL:
  Built-in a Digital PLL for Receive-Timing (RT). Receive-Timing signals demodulated by the DSP are recovered in the PLL and output as RT.
- DSP Control:
  The DSP is controlled by a start signal, start vectors, and bus control signals.
- Sync/Async and Async/Sync Conversion:
  MSM61057 provides a part of the sync/async and async/sync converting function. But main conversion are carried out by the MSM80C31.
- AFE Control:
  MSM61057 controls the AFE's A/D and D/A conversion and AGC.
- 40 pin plastic DIP package or 60 pin plastic flat package.

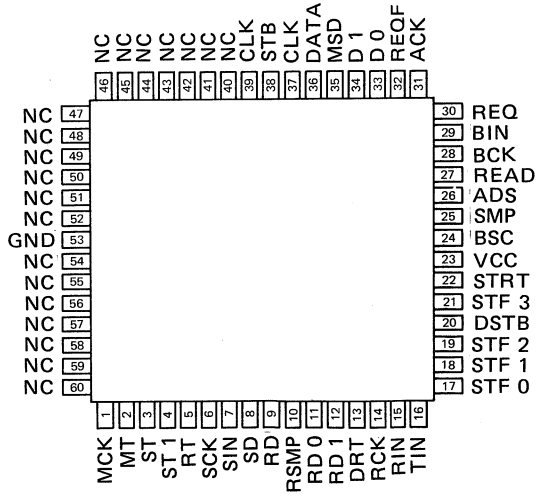
PIN CONFIGURATION

MSM61057RS



40 Pin DIP package

MSM61057GS



60 Pin FLAT package

BLOCK DIAGRAM

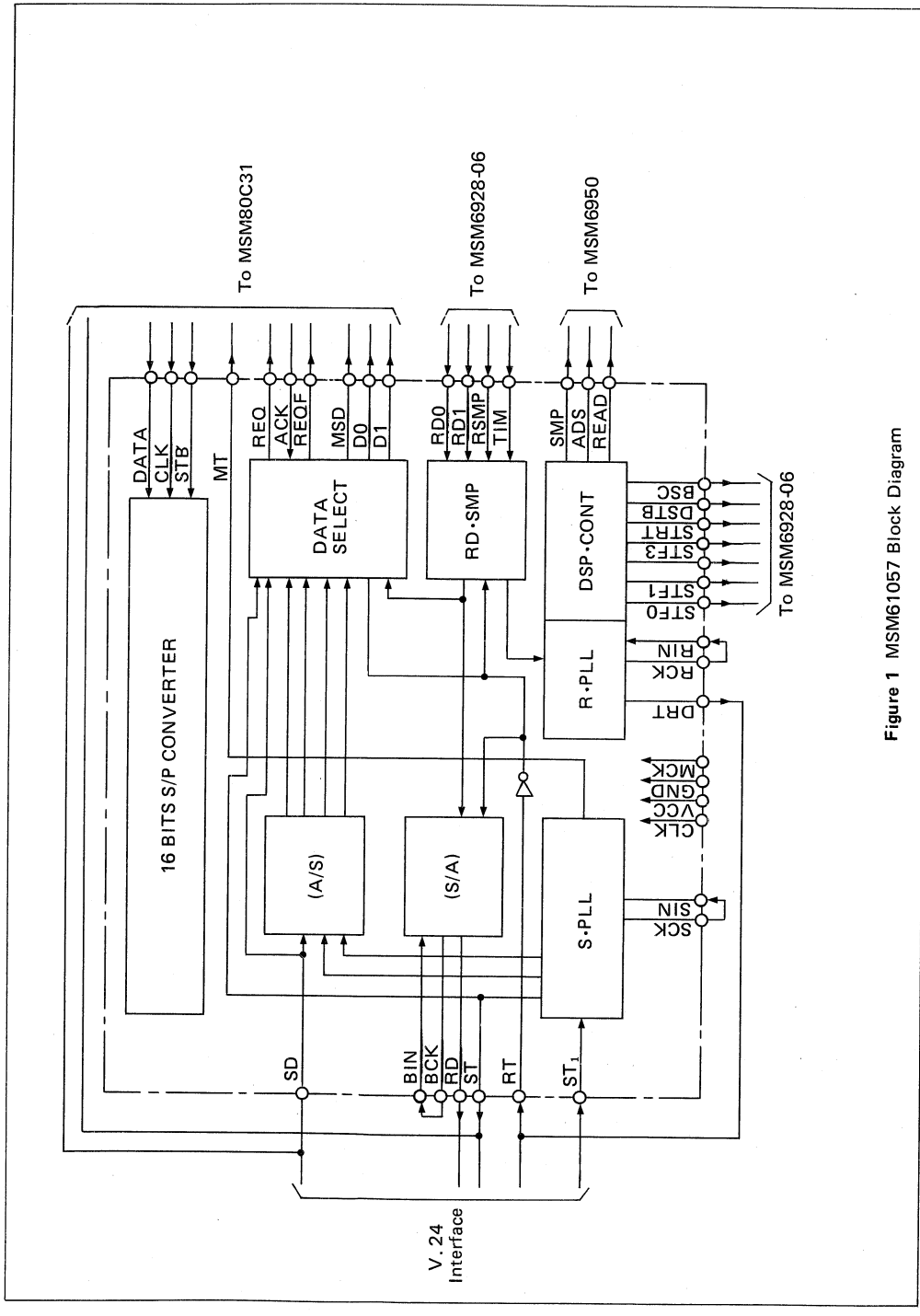
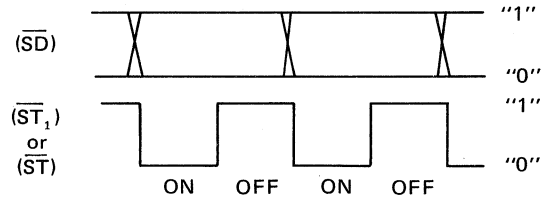
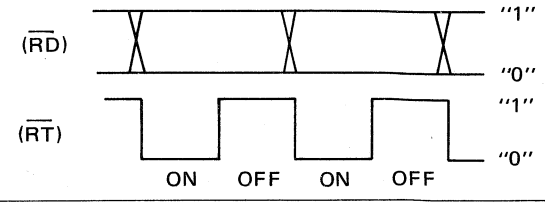


Figure 1 MSM61057 Block Diagram

ELECTRICAL CHARACTERISTICS

Please refer to that of MSM61000 series in OKI GATE ARRAY DATABOOK.

PIN DESCRIPTION

Pin Name	Pin No.		I/O	Function
	RS	GS		
MCK	1	1	I	Master clock input (921.6 kHz ±0.01%). The duty of this clock should be 50% ±5%.
MT	2	2	O	This clock is available for modulation and it indicates the sample timing of AFE and D/A data. See Fig. 2.
ST	3	3	O	1200/600 Hz clock output. This clock is synchronous to INTERNAL/ ST_1 /RT by setting ST A/B. See Fig. 2.
ST_1	4	4	I	External transmit timing input. (1200/600 Hz ±0.01%). If ST_1 is not used, ST should be held the digital "Low".
RT	5	5	I	Receive timing signal input.
SCK	6	6	O	These pins may be used for device tests only. In normal operation, SCK should be tied to SIN.
SIN	7	7	I	
SD	8	8	I	Transmit-Data ($\overline{SD}$) signal input. 
RD	9	9	O	Receive-Data ($\overline{RD}$) signal output. 
RSMP	10	10	I	This is used for sampling $\overline{PSKRD}$ and $\overline{FSKRD}$. RSMP should be made by inverting SAM in external.

Pin Name	Pin No.		I/O	Function
	RS	GS		
RD_0	11	11	I	$\overline{PSKRD}$ signal input. $\overline{PSKRD}$ is the PSK Receive-Data which is demodulated in DSP, and it is input via Data-Bus.
RD_1	12	12	I	$\overline{FSKRD}$ signal input. $\overline{FSKRD}$ is the FSK Receive-Data which is demodulated in DSP, and it is input via Data-Bus.
DRT	13	13	O	Data Rate Receive-Timing (RT) signal output. This pin should be tied to the RT.
RCK	14	14	O	These pins may be used for device tests only. In normal operation, they will be connected each other.
RIN	15	15	I	
TIM	16	16	I	This is the input pin for the receive-timing signal which is demodulated in DSP.
STF0	17	17	O	DSP vector signal outputs.
STF1	18	18	O	
STF2	19	19	O	
GND	20	23		Ground reference of V_{CC}.
STE3	21	21	O	DSP vector signal output.
STRT	22	22	O	DSP start signal output.
DSTB	23	20	O	This is one of the DSP control signals. When the signal turns to digital "High", Parallel Bus Dates are input to the DSP.
BSC	24	24	O	The DSP output control signal. During digital "Low", the DSP parallel Bus outputs will be enable.
SMP	25	25	O	DSP outputs are sampled by this signal.
ADS	26	26	O	A/D convertor start timing signal.
READ	27	27	O	A/D convertor data out timing signal.
BCK	28	28	O	These pins may be used for device tests only. In normal operation, BCK should be tied to BIN.
BIN	29	29	I	
REQ	30	30	O	When the interrupt to the MSM80C31 is requested, this output turns active "High"

Pin Name	Pin No.		I/O	Function
	RS	GS		
ACK	31	31	I	The timing diagram of these signals is shown in Fig. 3.
REQF	32	32	O	
D0	33	33	O	
D1	34	34	O	
MSD	35	35	O	
DATA	36	36	I	These pins are used to input the control signals from MSM80C31 See Fig. 1.
CLK	37	37	I	
STB	38	38	I	
CLR	39	39	I	During the CLR is active "High" all brocks may be initialized. In normal operation, this pin should be hold "Low".
V_{CC}	40	53		Supply voltage (+5 V nominal)

III

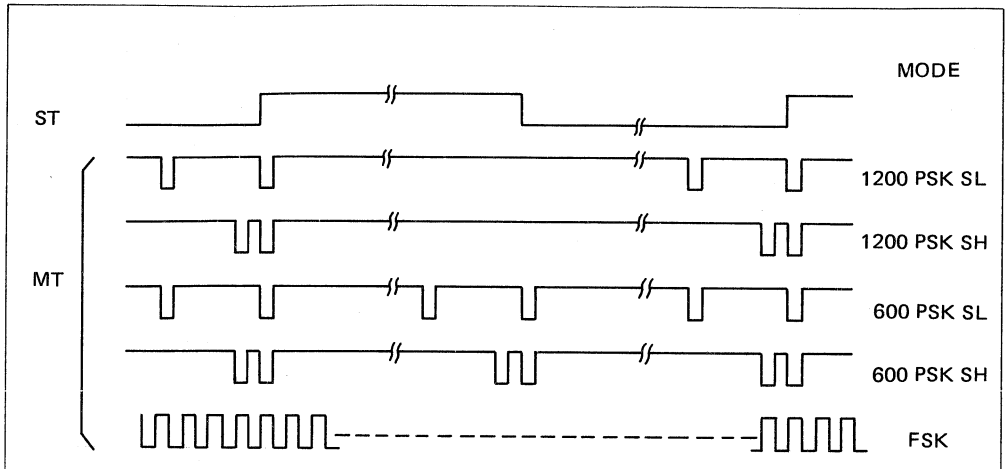


Figure 2 Timing Chart (1)

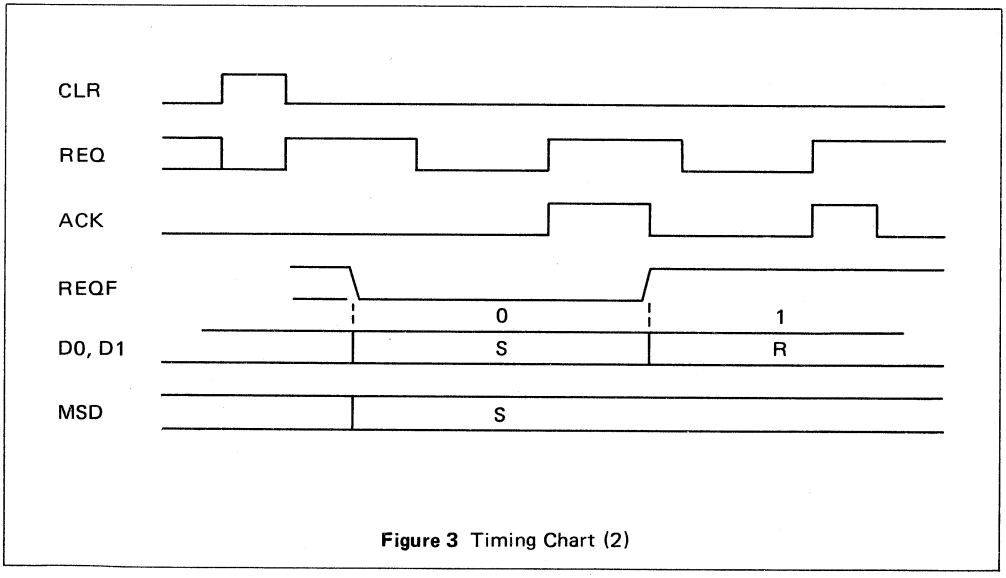


Figure 3 Timing Chart (2)

MODE				ST B	ST A	WL B	WL A	SL/SH	F/P	S/A	D/C =REC	DSS	CD 2	CD 1	V/B	1/2.3	S/P RD	S/P RSTF	S/P SPINS
BELL	H/S			○	○	○	○	1/0					1/0	0/1			○		
	300 FSK			○	○				1		1		1/0	0/1					
	1200^{+1} PSK ASYNC			○	○	○	○	1/0	0	0	0	0	1/0	0/1	1	0	○	○	○
	1200 PSK SYNC			○	○			1/0	0	1	1	0	1/0	0/1			○		
CCITT V22		H/S		○	○	○	○	1/0					1/0	0/1					
	B-II C-II	1200^{+1}	ASYNC	○	○	○	○	1/0	0	0	0	0	1/0	0/1	0	0	○	○	○
	B-II	$1200^{+2.3}$	ASYNC	○	○	○	○	1/0	0	0	0	0	1/0	0/1	0	1	○	○	○
	B-IV C-IV	600^{+1}	ASYNC	○	○	○	○	1/0	0	0	0	1	1/0	0/1	0	0	○	○	○
	B-IV	$600^{+2.3}$	ASYNC	○	○	○	○	1/0	0	0	0	1	1/0	0/1	0	1	○	○	○
	C-V	1205/1223 301/305	ASYNC	○	○	○	○	1/0	0	0	1	0	1/0	0/1	0		○	○	
		1200	SYNC	○	○			1/0	0	1	1	0	1/0	0/1	0		○		
		600	SYNC	○	○			1/0	0	1	1	1	1/0	0/1	0		○		
			INT·ST2	0	X	8	0	0									See Figure 5, 6, 7		
						9	0	1											
			ST2	1	0	10	1	0											
			RT2	1	1	11	1	1											

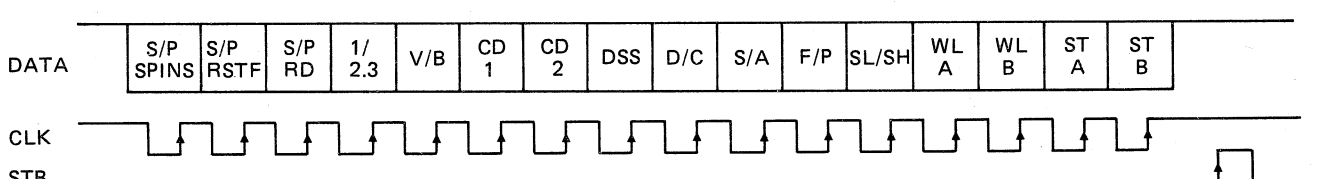
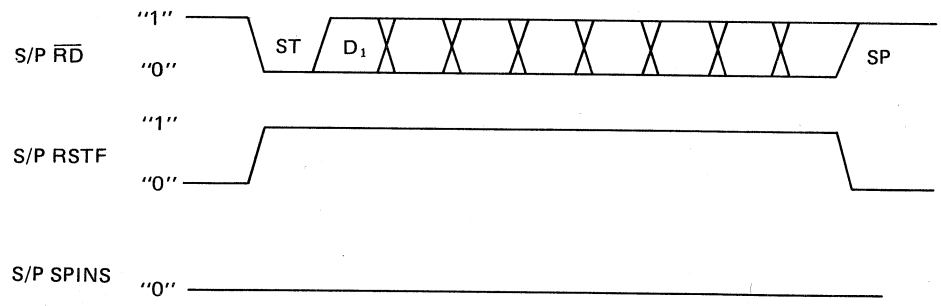
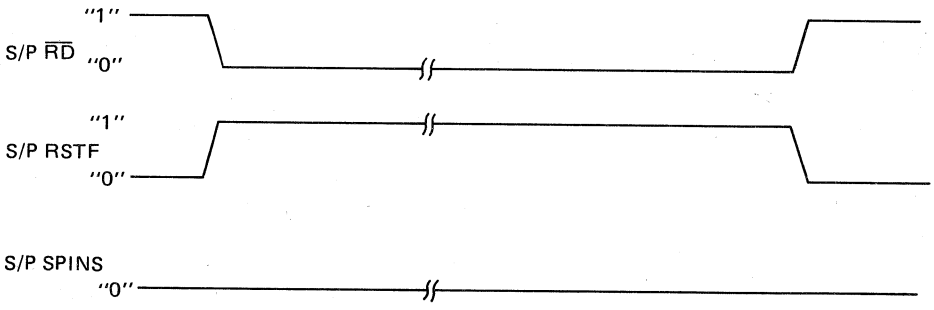


Figure 4



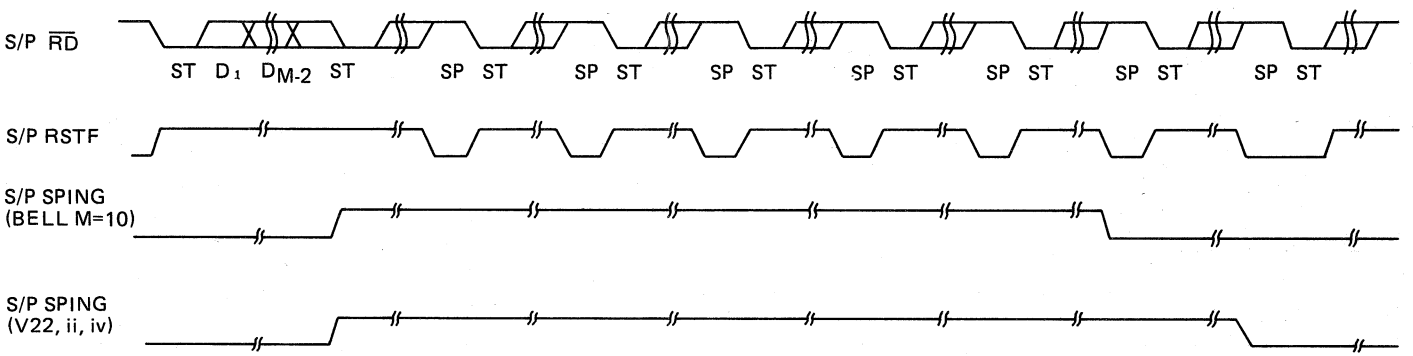
- S/P RSTF should be high for the duration of character length M (ST → SP) in both Bell 212A and V.22 modes ii, iii.
  Low to high transitions should be synchronized with ST of S/P $\overline{RD}$.
  High to low transitions should be synchronized with SP of S/P $\overline{RD}$.
- S/P SPINS should be low in both Bell 212A and V.22 modes ii, iv.

Figure 5 Receiving Normal Data



- S/P RSTF should be high for the duration of continuous A polarity, in both Bell 212A and V.22 modes.
- S/P SPINS should be low for the duration of continuous A polarity, in both Bell 212A and V.22 modes.

Figure 6 Receiving Break Signals



- S/P $\overline{RD}$ is as same as Fig. 5
- S/P RSTF is as same as Fig. 5; however, when SP is absent, continues high till receipt of the next SP.
- S/P SPINS should be high for three characters after detecting the absence of SP in V.22 ii, iv.
  High for seven characters after detecting the absence of SP in Bell M = 9.
  High for six characters after detecting the absence of SP in Bell M = 10.
  High for seven characters after detecting the absence of SP in V.22 ii, iv.

Figure 7 Detecting Stop Reinserts

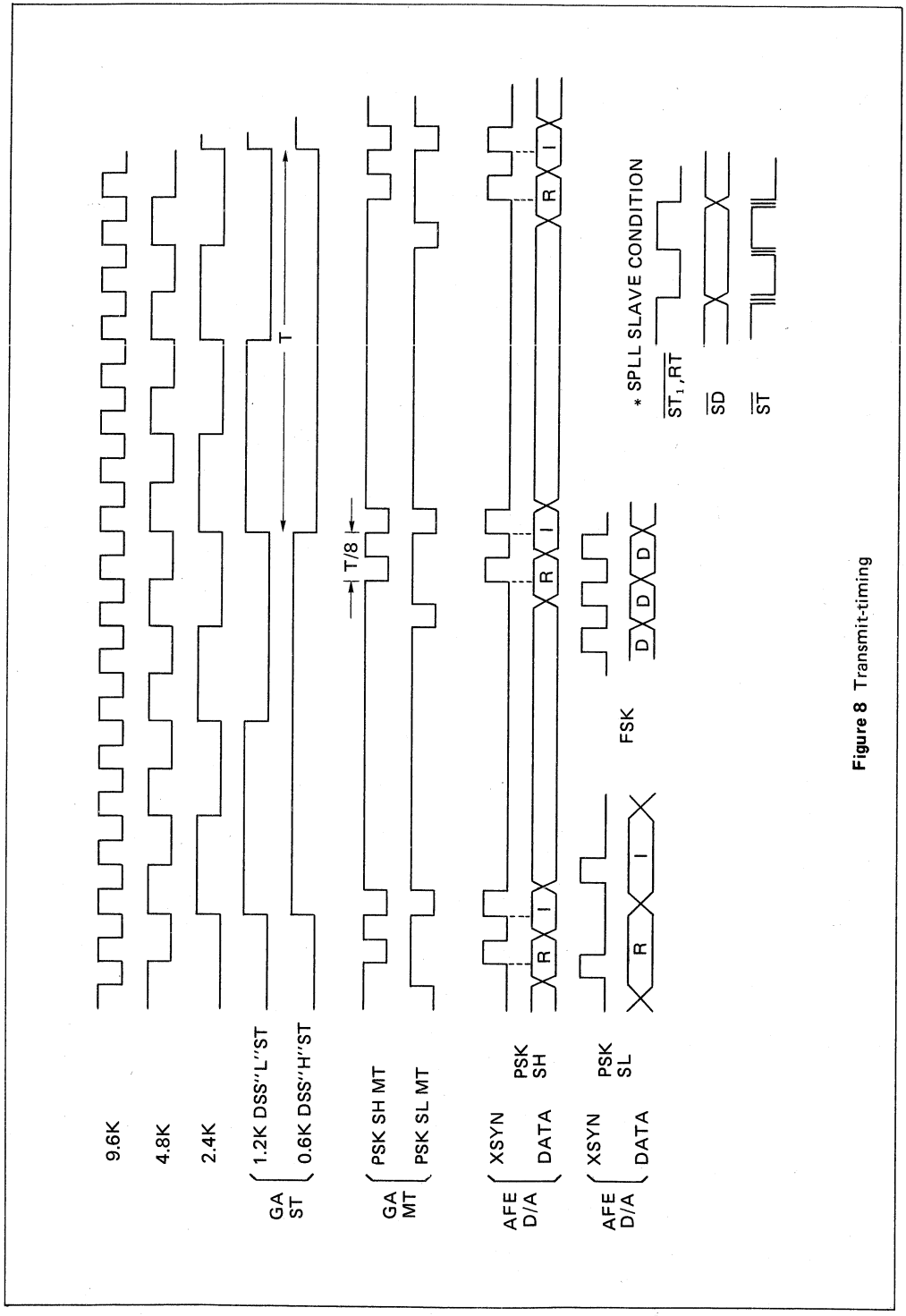


Figure 8 Transmit-timing

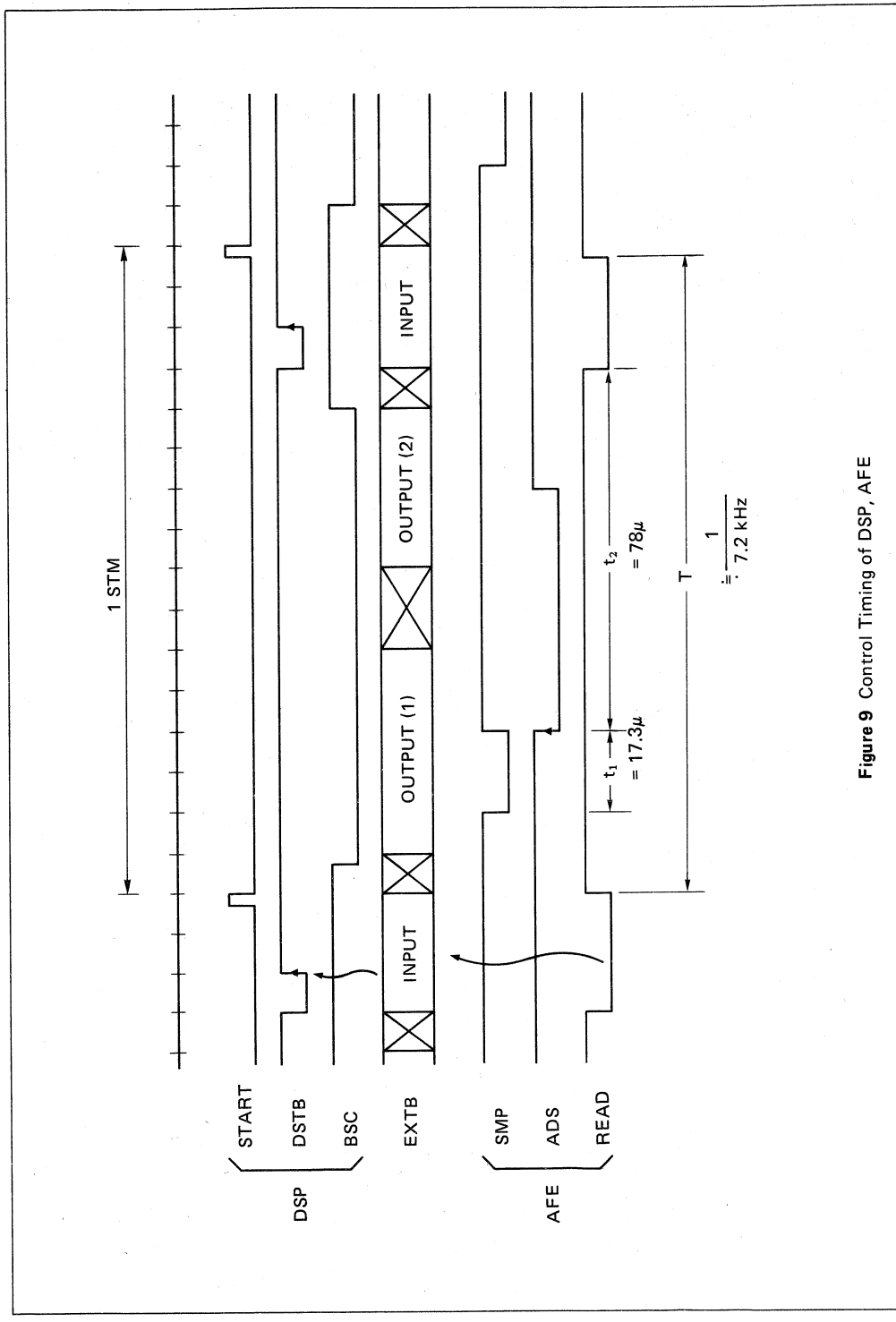


Figure 9 Control Timing of DSP, AFE

MSM6928-07

DSP FOR 2400 BPS FULL DUPLEX MODEM CHIP SET

GENERAL DESCRIPTION

The MSM6928-07 is a digital signal processor which is used as a demodulator in the chip for 2400 bps full duplex modem based on CCITT V.22 bis standard.

The MSM6928-07 operates as a QAM modulator, PSK demodulator, FSK demodulator, etc. by using the digital signal processing method and it transmits the AGC signal to the MSM6950 (Analog Front End).

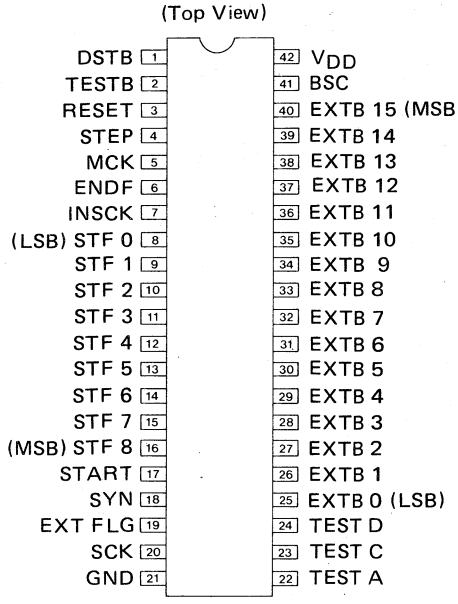
The MSM6928-07 is fabricated by OKI's low power consumption CMOS silicon gate technology. By utilizing MSM6928-07 together with MSM6950, MSM80C51-58 (Modulator), MSM61077 (Asynchronous/Synchronous Conversion, etc.), and external controller, an intelligent modem system based on CCITT V.22 bis standard can be realized easily.

FEATURES

- QAM/PSK Demodulation
  The received signal is multiplied with an internal demodulation carrier, and input to the next stage PDF, as a baseband signal. The PDF output is generated as the demodulated PSK-RD after the line distortion, is corrected by an automatic equalizer.
- FSK Demodulation
  The received signal is demodulated through a BPF, a delay detector, and an LPF, and then output as FSK-RD.
- AGC
  In the AGC block, the power of the input signal is calculated and its difference from the reference voltage is output as the control signal for the Analog-Front-End variable control.
- 42 pin plastic DIP package or 60 pin plastic flat package.

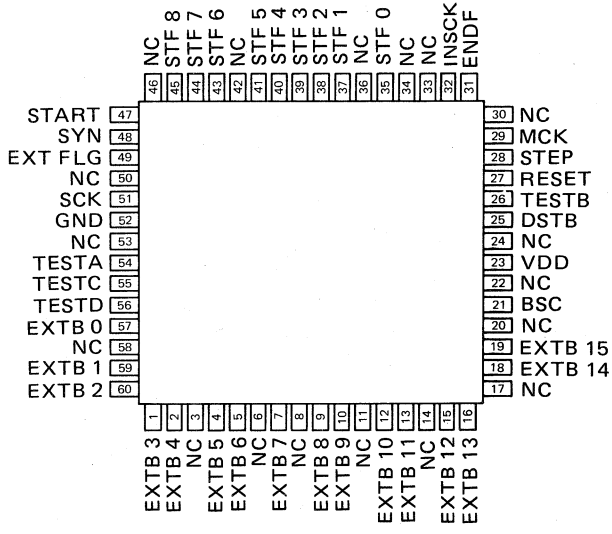
PIN CONFIGURATION

MSM6928-07RS



42 pin DIP package

MSM6928-07GS



60 pin FLAT package

III

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Item	Symbol	Rating	Unit	Remark
Power Supply Voltage	V_{DD}	-0.3 ~ +7	V	
Input Voltage	V_{IN}	-0.3 ~ V_{DD}	V	
Power Dissipation	Pd	1.0	W	
Operating Temperature Range	Top	-10 ~ +70	°C	
Storage Temperature Range	TsT	-55 ~ +150	°C	

Guaranteed Operating Range

Item	Symbol	Rating	Unit	Remark
Power Supply Voltage	V_{DD}	+4.75 ~ 5.25	V	
Ambient Temperature Range	Ta	0 ~ +60	°C	

Static Electrical Characteristics

V_{DD} = 5 V ±5%, Ta = 0 ~ 60°C

Item	Symbol	Condition	Limit			Unit	Remark
			Min	Typ	Max		
Output Voltage	V_{OH}	I_Q = -40 μA	4.2	–	V_{DD}	V	–
	V_{OL}	I_Q = 1.6 mA	-0.3		0.4		
Input Voltage	V_{IH}	–	2.4	–	V_{DD}	V	–
	V_{IL}		-0.3		0.8		
Input Leakge Current	I_{IL}	GND < V_{IN} < V_{DD}	–	–	±10	μA	–
Bus Output Voltage	BV_{OH}	I_Q = -80 μA	4.2	–	–	V	–
	BV_{OL}	I_Q = 1.6 mA	–		0.4		
Bus Input Voltage	BV_{IH}	–	2.4	–	–	V	–
	BV_{IL}		–		0.8		
Bus Input Leakage Current	B_{IL}	GND < V_{IN} < V_{DD}	–	–	±10	μA	@ BUS OFF Condition
Operating Current	I_{DDQ}	–	–	35	40	mA	MCK: 5529.6 kHz
Quiescent Current	I_{DDS}	–	–	–	0.3	mA	MCK: OFF

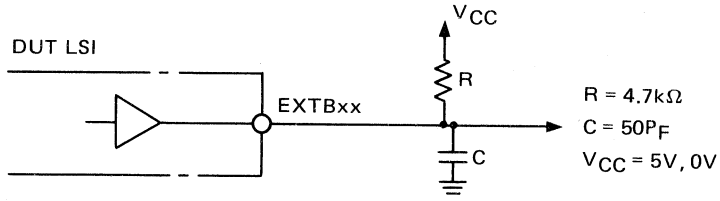
Dynamic Electrical Characteristics

Item	Symbol	Condition	Limit		Unit	Remark
			Min	Max		
BSC-EXTB						
Delay Time	TD	Timing Chart A	–	200	ns	Common to EXTB 0 ~ EXTB 15
Rise Time	TR		–	100		Refer to Figure 1
Fall Time	TF		–	100		
DSTB-EXTB						
Pusle Width	T_W	Timing Chart B	300	–	ns	Refer to Figure 1
Setup Time	T_{SET}		100	–		
Hold Time	T_{HOLD}		100	–		
SCK-SIN						
Pulse Width	T_W	Timing Chart C	180	–	ns	Refer to Figure 2
Setup Time	T_{SET}		100	–		
Hold Time	T_{HOLD}		100	–		
SCY-SYN						
Pulse Width	T_W	Timing Chart D	180	–	ns	Refer to Figure 2
Setup Time	T_{SET}		100	–		
Hold Time	T_{HOLD}		100	–		
START-START FLAG						
Pulse Width	T_W	Timing Chart E	1300	–	ns	Refer to Figure 3
Setup Time	T_{SET}	MCK = 5529.6 kHz $\pm 1 \times 10^{-4}$	100	–		
Hold Time	T_{HOLD}		100	–		
MCK						
Rise Time	TR	Timing Chart F	–	30	ns	Refer to Figure 3
Fall Time	TF_1		–	30		
Duty Ratio	T1/T2		95	105	%	
Frequency	FM		5529	5530	kHz	

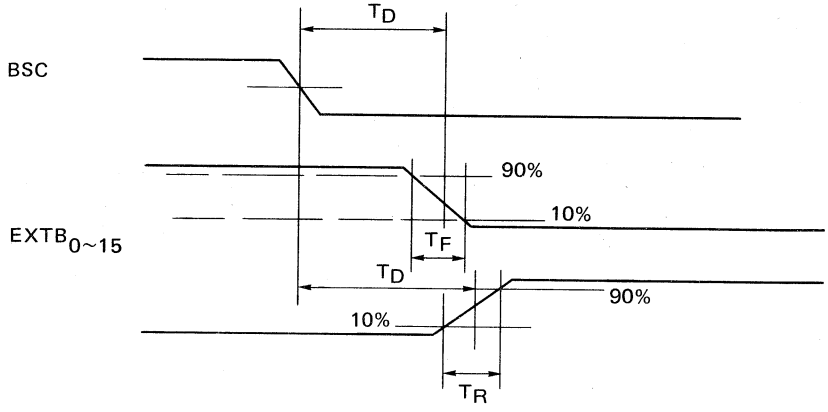
PIN DESCRIPTION

Pin Name	Pin No.		I/O	Function
	RS	GS		
DSTB	1	25	IN	Loads the signal on EXT Bus into Input Register. ⌐↑
TESTB	2	26	IN	Test signal. Loads the signal on internal bus into Output Register. 1: Load, 0: Normal
RESET	3	27	IN	Operation start instruction signal. Operation in synchronization with ⌐↓ 1: Stop, 0: Operation start
STEP	4	28	IN	Selects either of continuous operation and single step operation. 1: Continuous operation (Normal) 0: Single step operation
MCK	5	29	IN	Master clock signal, normally 5529.6 kHz.
ENDF	6	31	OUT	Program specifying sync signal.
INSCK	7	32	OUT	Machine cycle sync signal.
STF 0	8	35	IN	External specifying address signal 2^0 (LSB)
STF 1	9	37	IN	External specifying address signal 2^1
STF 2	10	38	IN	External specifying address signal 2^2
STF 3	11	39	IN	External specifying address signal 2^3
STF 4	12	40	IN	External specifying address signal 2^4
STF 5	13	41	IN	External specifying address signal 2^5
STF 6	14	43	IN	External specifying address signal 2^6
STF 7	15	44	IN	External specifying address signal 2^7
STF 8	16	45	IN	External specifying address signal 2^8 (MSB)
START	17	47	IN	Operation starting sync signal. Loads external specifying address.
SYN	18	48	IN	Causes the serially input jump condition to be loaded into EXT FLG Register in the parallel form.
EXT FLG	19	49	IN	Serially input jump condition. This signal is loaded into S/P on the negative-going edge of SCK.
SCK	20	51	IN	Serially input jump condition loading clock.
GND	21	52	–	Ground.

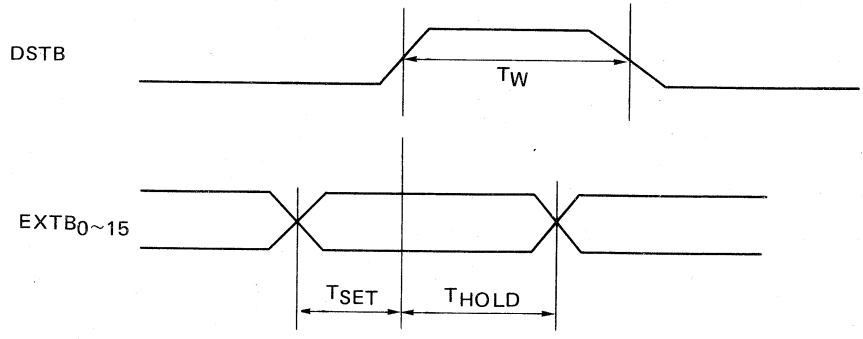
Pin Name	Pin No.		I/O	Function
	RS	GS		
TESTA	22	54	IN	Test signal. Holds Program Counter. 0: Hold, 1: Normal
TESTC	23	55	IN	Test signal.
TESTD	24	56	IN	Test signal.
EXTB 0	25	57	I/O	External bidirectional bus 2^0 (LSB)
EXTB 1	26	59	I/O	External bidirectional bus 2^1
EXTB 2	27	60	I/O	External bidirectional bus 2^2
EXTB 3	28	1	I/O	External bidirectional bus 2^3
EXTB 4	29	2	I/O	External bidirectional bus 2^4
EXTB 5	30	4	I/O	External bidirectional bus 2^5
EXTB 6	31	5	I/O	External bidirectional bus 2^6
EXTB 7	32	7	I/O	External bidirectional bus 2^7
EXTB 8	33	9	I/O	External bidirectional bus 2^8
EXTB 9	34	10	I/O	External bidirectional bus 2^9
EXTB 10	35	12	I/O	External bidirectional bus 2^{10}
EXTB 11	36	13	I/O	External bidirectional bus 2^{11}
EXTB 12	37	15	I/O	External bidirectional bus 2^{12}
EXTB 13	38	16	I/O	External bidirectional bus 2^{13}
EXTB 14	39	18	I/O	External bidirectional bus 2^{14}
EXTB 15	40	19	I/O	External bidirectional bus 2^{15} (MSB)
BSC	41	21	IN	External bidirectional bus specifying signal. 1: Input, 0: Output
V_{DD}	42	23	—	Power supply +5 V



Loading Condition

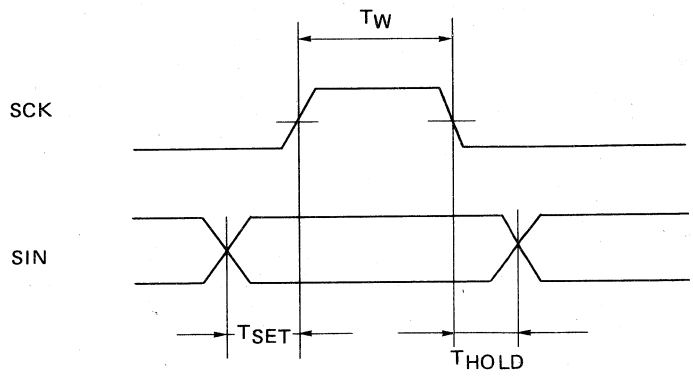


Timing Chart A

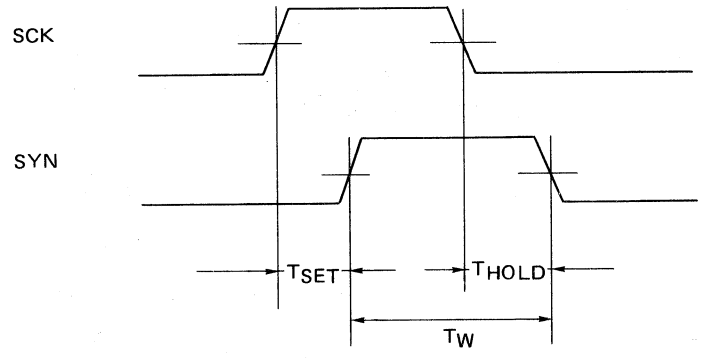


Timing Chart B

Figure 1 Test conditions and timing charts

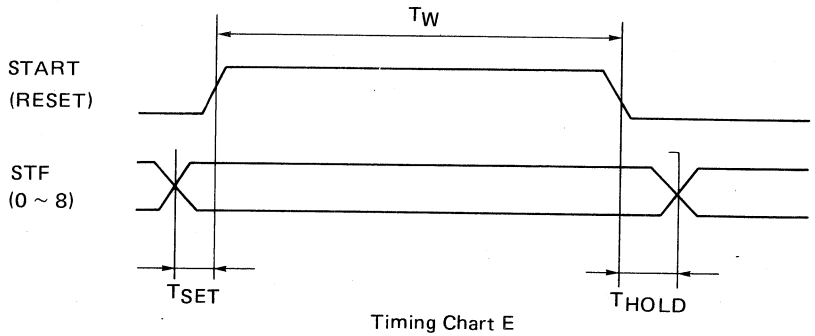


Timing Chart C

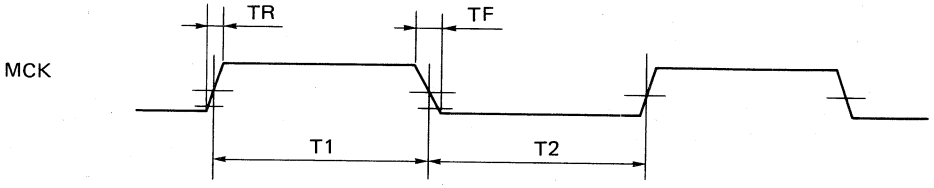


Timing Chart D

Figure 2 Test conditions and timing charts



Timing Chart E



DUTY = T1/T2

Timing Chart F

Note: The test pin conditions are shown below.

No.	Pin Name	Pin No.	Set Condition
1	TEST A	22	High
2	TEST B	2	Low
3	TEST C	23	High
4	TEST D	24	High
5	STEP	4	High

Figure 3 Test conditions and timing charts

MSM6928-07 APPLICATION

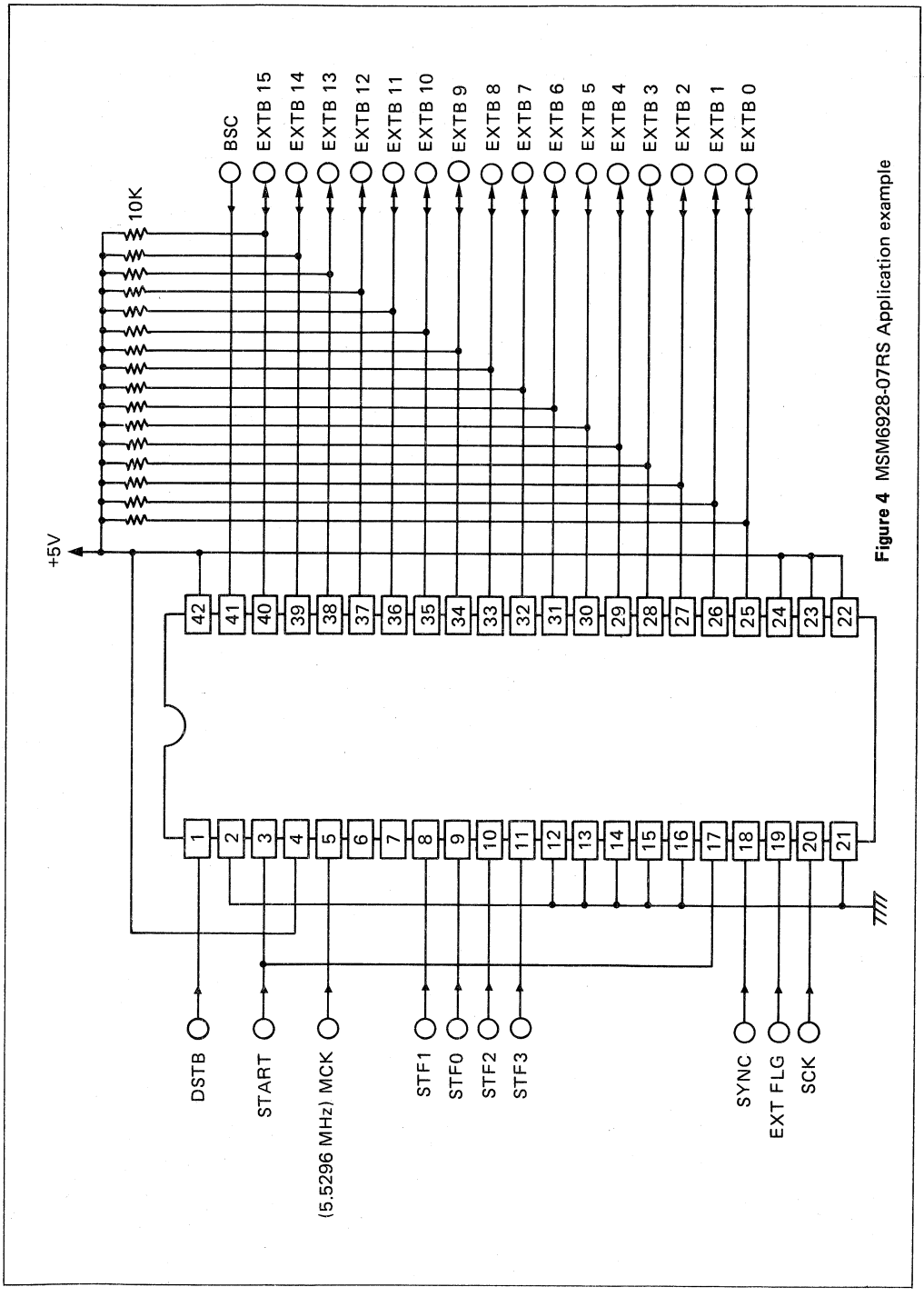


Figure 4 MSM6928-07RS Application example

III

TIMING CHARTS

Input/Output Data

Demodulating data (A/D output) and gain setting data for AGC are input and output via the bus every sampling period (STM). See Figure 5 and Figure 6.

Control Signals

Each baud rate (BTM) is divided into 12 (1 BTM = 12 STMs), and the start vectors are input from STF0-3 every STM. See Figure 7.

Mode specifications, such as data speed, ORG/ANS switching, and FCD selection, are input as 16-bit serial data. See Figure 8.

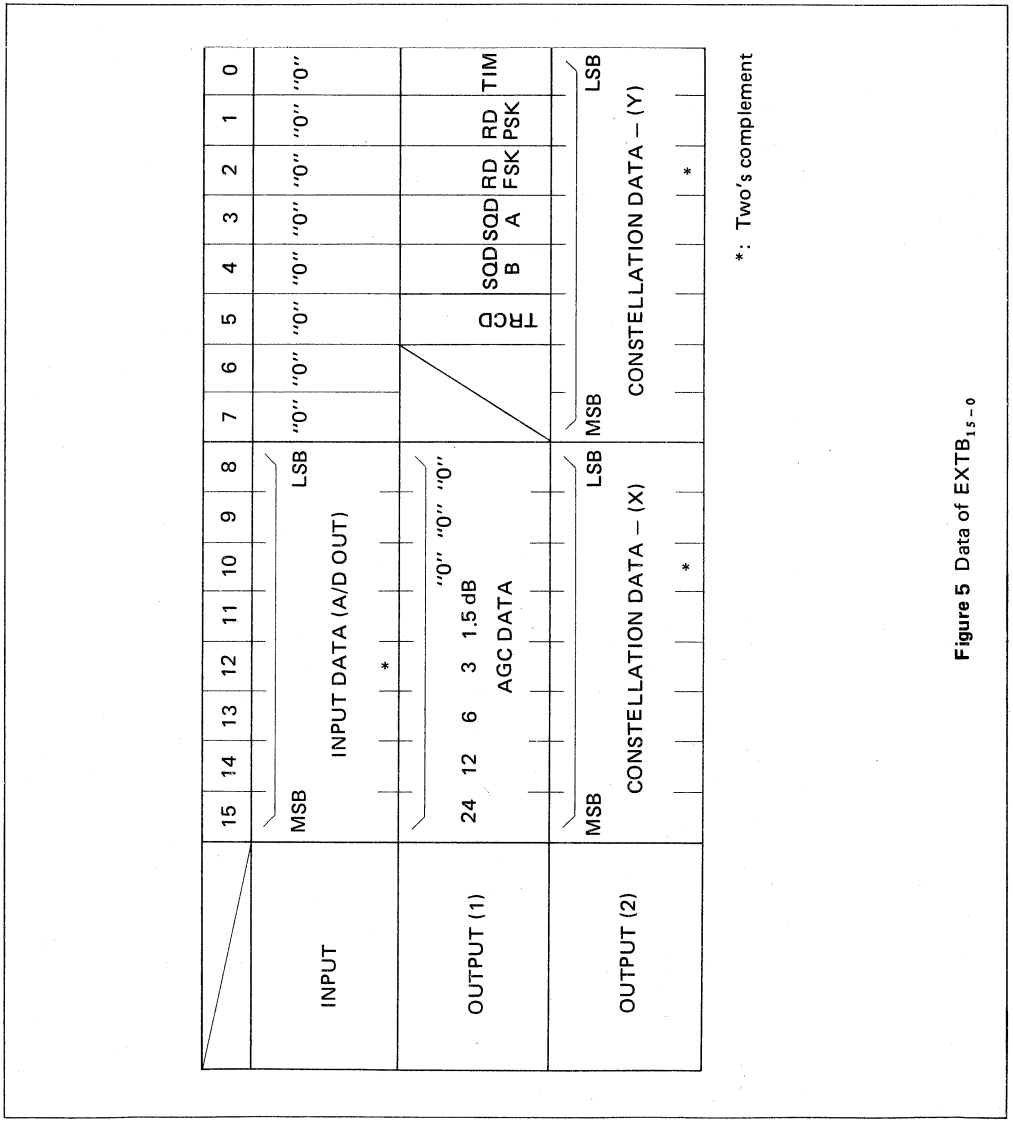


Figure 5 Data of $EXTB_{15-0}$

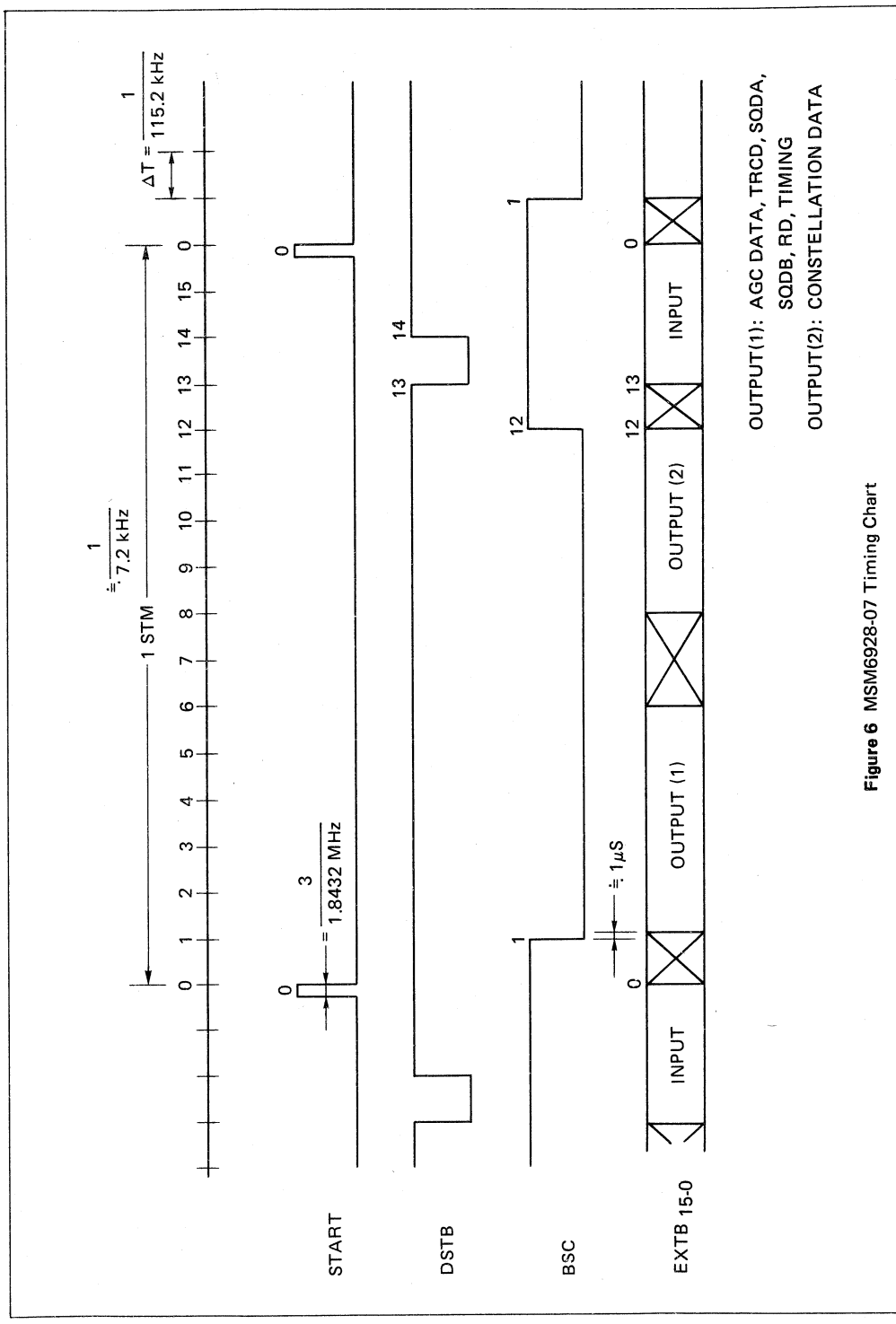


Figure 6 MSM6928-07 Timing Chart

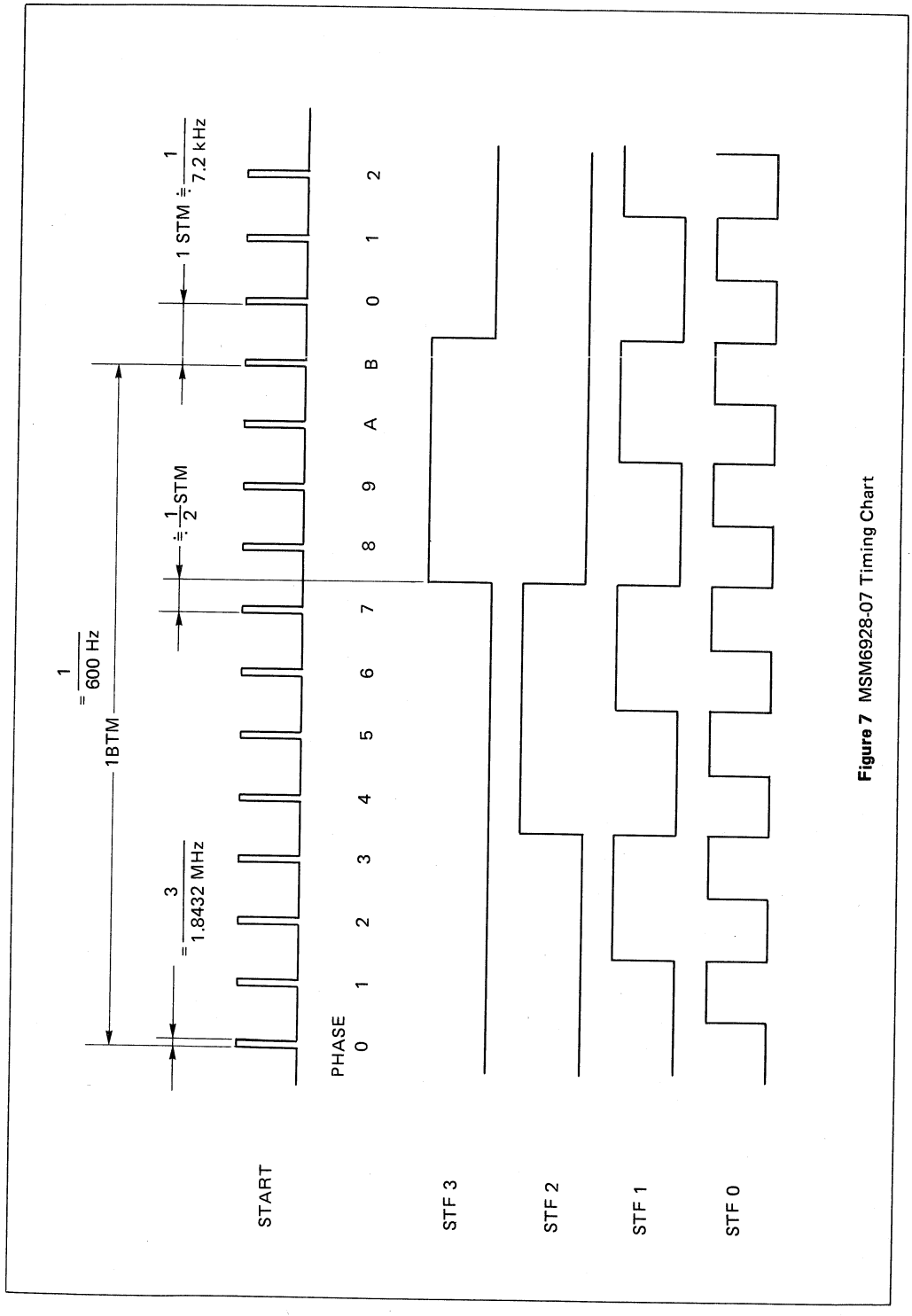


Figure 7 MSM6928-07 Timing Chart

No.	Name	Function
D0	XFCD	FCD (carrier detect) signal for Demodulator 0; OFF (Set 0 when $\overline{FCD}$ = 1) 1; ON (Set 1 when $\overline{FCD}$ = 0)
D1	TAPH	AEQL operation control 0; Active 1; Hold
D2	DSS0	Demodulator data signalling rate select Note) Not related to FSK mode.
D3	DSS1	

DSS1	DSS0	Mode	
0	0	16 values QAM	2400 bps
0	1		
1	0	4 phase PSK	1200 bps
1	1	2 phase PSK	600 bps

No.	Name	Function
D4	EGC0	AEGL tap coefficient control
D5	EGC1	

EGC1	EGC0	α
0	0	α_1
0	1	α_2
1	0	α_3
1	1	α_4

See Appendix B.

Note)
α_4 = 0 (Tap hold)

No.	Name	Function
D6	AQID	Adaptive equalizer (AEQL) reset 0; Reset (Set the center tape) 1; Normal operation See Appendix B.
D7	PLCR	Carrier PLL reset 0; Reset 1; Normal operation
D8	PLEN	Carrier PLL enable 0; Disable 1; Enable
D9	SANSORG	Originate/answer mode select for receiver 0; Answer (Receive — Lowband) 1; Originate (Receive — Highband)
D10	AGCT0	AGC circuit control coefficients
D11	AGCT1	

AGCT1	AGCT0	β
0	0	β_1
0	1	β_2
1	0	β_3
1	1	

See Appendix B.

No.	Name	Function
D12	SQDC	Threshold level selection for SCDB 0; High ($\sim 10^{-3}$) 1; Low ($\sim 10^{-4}$) See appendix B. NOTE) Does not mean to measure the bit error rate itself.
D13	SQDEN	LPF accumulate register clear for SQDA and SQDB (signal quality detecter) 0; Normal operation 1; Reset See Appendix B.
D14	TRCDC	Threshold level for S1 data detection 0; Low (Handshake) 1; High (Retrain)
D15	XFCD1	DSP software reset except for AGC control 0; Normal operation 1; Reset

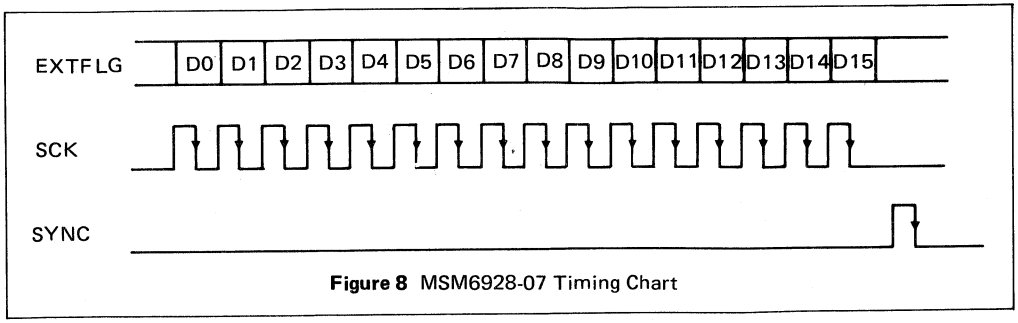


Figure 8 MSM6928-07 Timing Chart

MSM61077

GATE ARRAY FOR 2400 BPS FULL DUPLEX MODEM CHIP SET

GENERAL DESCRIPTION

The MSM61077 is a gate array LSI which is used in the chip set for 2400 bps full duplex modem based on Bell 212A, CCITT V. 22 and V.22-bis.

The MSM61077 plays a role for asynchronous/synchronous converting, scrambler and descrambler in the 2400 bps full duplex modem system.

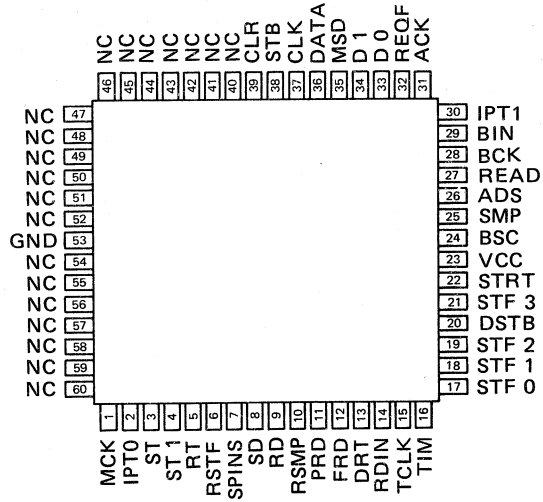
The MSM61077 is fabricated by OKI's low power consumption CMOS silicon gate technology. By utilizing MSM61077 together with MSM6928-07 (Digital Signal Processor – DSP used for Demodulator). MSM6950 (Analog Front End – AFE) and MSM80C51 (Modulator), an intelligent modem system based on Bell 212A or CCITT V.22 and V.22-bis can be realized easily.

FEATURES

- S. PLL:
  Built-in a Digital PLL for Transmit-Timing (ST). ST is output from this PLL in the synchronous mode.
- R. PLL:
  Built-in a Digital PLL for Receive-Timing (RT). Receive-Timing signals demodulated by the DSP are recovered in the PLL and output as RT.
- DSP Control:
  The DSP is controlled by a start signal, start vectors, and bus control signals derived from this GA.
- Sync/Async and Async/Sync Conversion:
  MSM61077 provides a part of the sync/async and async/sync converting function.
- AFE Control:
  MSM61077 controls A/D and D/A converters and AGC in AFE.
- 60 pin plastic flat package.

PIN CONFIGURATION

MSM61077GS-K



60 Pin FLAT package

III

BLOCK DIAGRAM

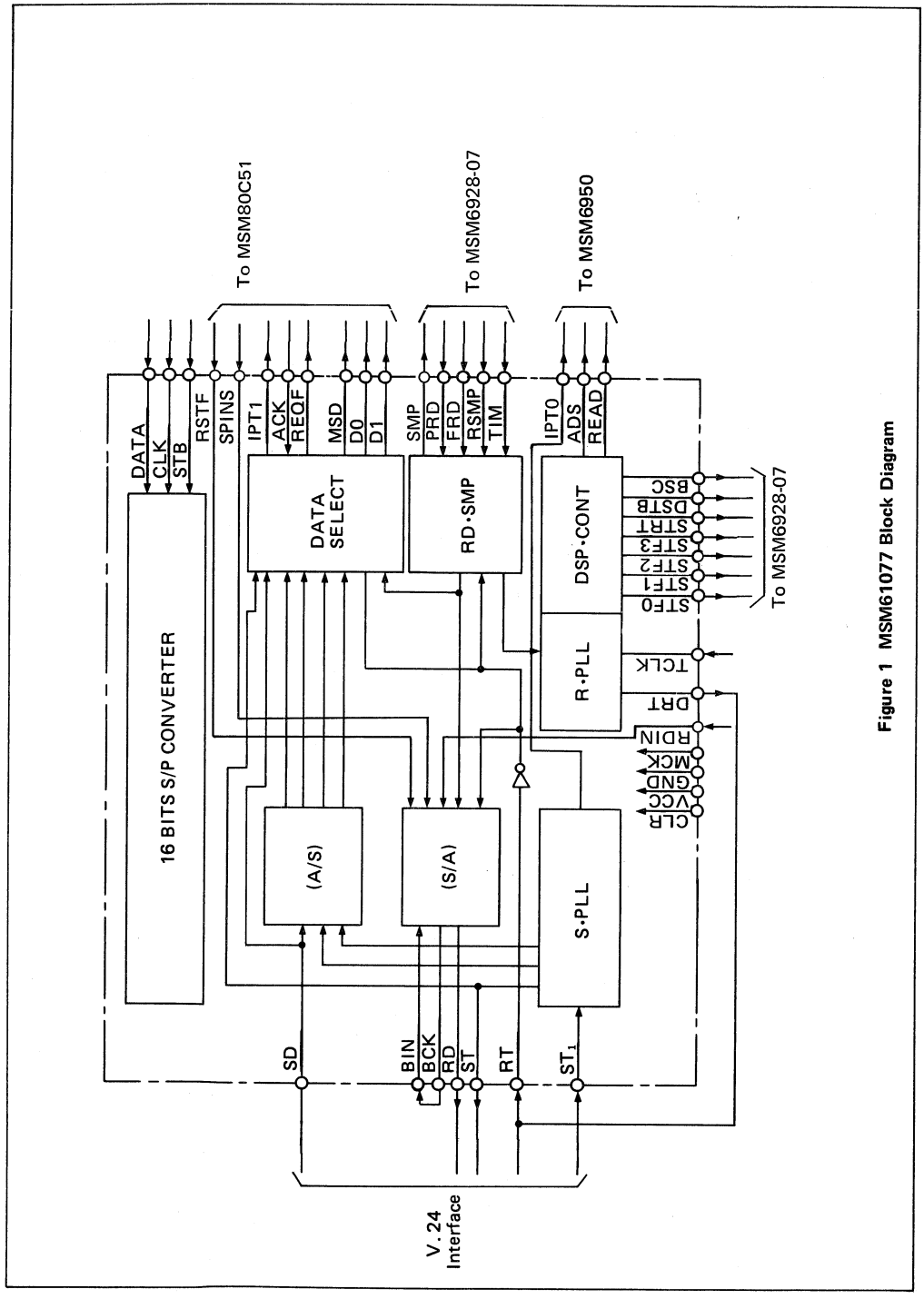
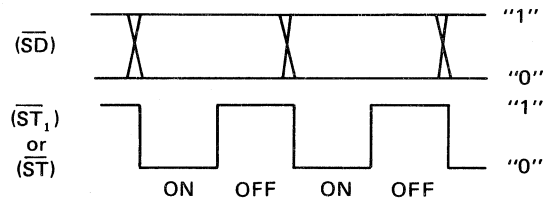
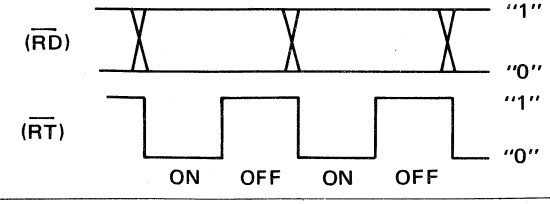


Figure 1 MSM61077 Block Diagram

ELECTRICAL CHARACTERISTICS

Please refer to that of MSM61000 series in OKI GATE ARRAY DATABOOK.

PIN DESCRIPTION

Pin Name	Pin No.	I/O	Function
MCK	1	I	Master clock input (921.6 kHz ±0.01%). The duty of this clock should be 50% ±5%.
IPTO	2	O	This signal is write clock of D/A converter in AFE. See Figure 2.
ST	3	O	2400/1200/600 Hz clock output. This clock is synchronous to INTERNAL/ST_1/RT by setting ST A/B. See Figure 2.
ST_1	4	I	External transmit timing input. (2400/1200/600 Hz ±0.01%). If ST_1 is not used, ST should be held the digital "Low".
RT	5	I	Receive-Timing signal input.
RSTF	6	I	Control flag for SYN/ASYN converter.
SPINS	7	I	Control flag for SYN/ASYN converter.
SD	8	I	Transmit-Data ($\overline{SD}$) signal input. 
RD	9	O	Receive-Data ($\overline{RD}$) signal output. 
RSMP	10	I	Latch clock input of demodulated receive data from DSP. The invert signal of SMP must be given to RSMP.

III

Pin Name	Pin No.	I/O	Function
PRD	11	I	Demodulated Receive-Data input (PSK, QAM). PRD is given from I/O port of DSP.
FRD	12	I	Demodulated Receive-Data input (FSK). FRD is given from I/O port of DSP.
DRT	13	O	Data Rate Receive-Timing (RT) signal output. This pin should be tied to the RT.
RDIN	14	I	Receive-Data input from descrambler output in MCU.
TCLK	15	I	Master clock for RPLL (1.8432 MHz).
TIM	16	I	This is the input pin for the Receive-Timing signal which is recovered in DSP.
STF0	17	O	Vector signal outputs for DSP.
STF1	18	O	
STF2	19	O	
VCC	23		Voltage supply (+5V).
STF3	21	O	Vector signal output for DSP.
STRT	22	O	Start signal output for DSP. See Figure 4.
DSTB	20	O	Write clock of I/O port for DSP. See Figure 4.
BSC	24	O	Read clock of I/O port for DSP. See Figure 4.
SMP	25	O	Latch clock of read data from I/O port.
ADS	26	O	A/D convertor start timing signal. See Figure 4.
READ	27	O	A/D convertor read timing signal. See Figure 4.
BCK	28	O	These pins may be used for device tests only. In normal operation, BCK should be tied to BIN.
BIN	29	I	
IPT1	30	O	Interrupt signal to MCU.

Pin Name	Pin No.	I/O	Function
ACK	31	I	The timing diagram of these signals is shown in Figure 3.
REQF	32	O	
D0	33	O	
D1	34	O	
MSD	35	O	
DATA	36	I	Serial status control data input. See Table 1.
CLK	37	I	Shift clock of status control data.
STB	38	I	Strobe clock of status control data.
CLR	39	I	During the CLR is active "High", all blocks can be initialized. In normal operation, this pin should be set "Low"
GND	53		Ground (0 V)

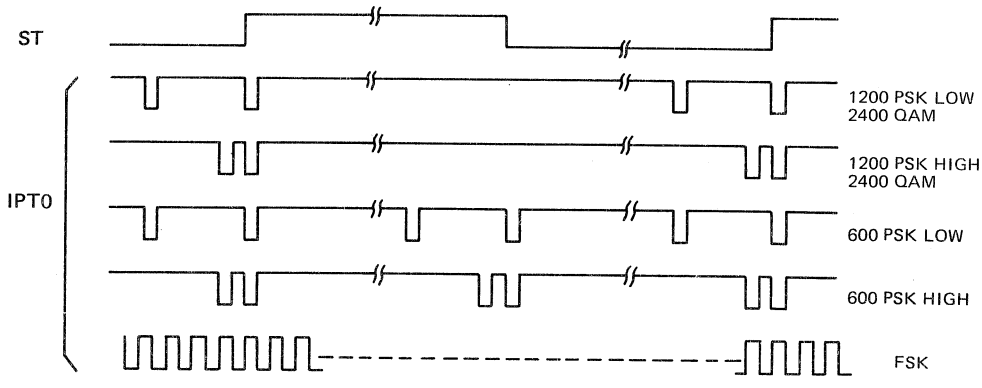


Figure 2 Timing Chart (1)

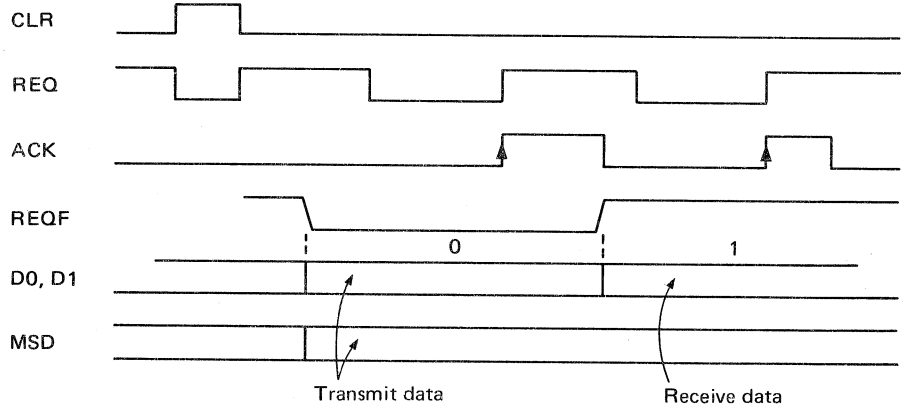
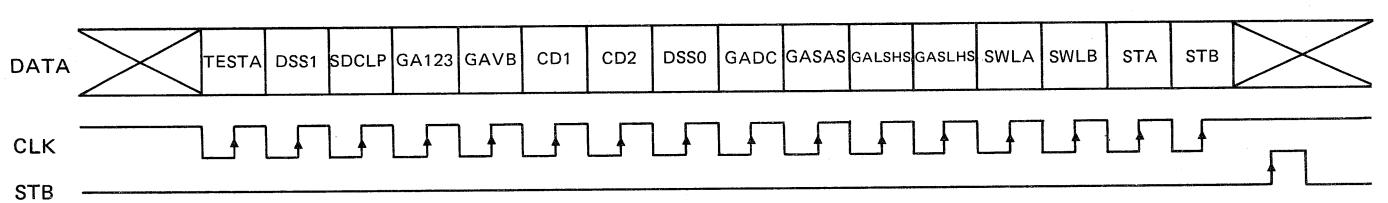


Figure 3 Timing Chart (2)

Table 1 GA Mode Definition Table

Mode				TESTA	DSS 1	SDCLP	GA123	GAVB	CD1	CD2	DSS0	GADC	GASAS	GALSHS	GASLSH	SWLA	SWLB	STA	STB
2400 bps	Asynchronous	Speed Conversion Tolerance	+1.0%	0	0	1	0	0	Timing PLL Control		X	0	0	0	0/1	Character Bit length Definition (8~11 bit)		Transmitter signal Element Timing Definition (ST_1, ST_2, RT)	
			+2.3%	0	0	1	1	0			X	0	0	0	0/1				
	Synchronous	2400±0.01%		0	0	1	X	X			X	1	1	0	0/1				
1200 bps	Asynchronous	CCITT	Speed Conversion Tolerance +1.0%	0	1	1	0	0			0	0	0	0	0/1				
			Speed Conversion Tolerance +2.3%	0	1	1	1	0			0	0	0	0	0/1				
		BELL (1200+1.0~-2.5%)		0	1	1	0	1			0	0	0	0	0/1				
	Synchronous	1200±0.01%		0	1	1	X	X			0	1	1	0	0/1				
600 bps	Asynchronous	Speed Conversion Tolerance	+1.0%	0	1	1	0	0			1	0	0	0	0/1				
			+2.3%	0	1	1	1	0			1	0	0	0	0/1				
	Synchronous	600±0.01%		0	1	1	X	X			1	1	1	0	0/1				
300 bps				0	X	X	X	X	X	X	X	1	1	1	0/1	X	X	X	X



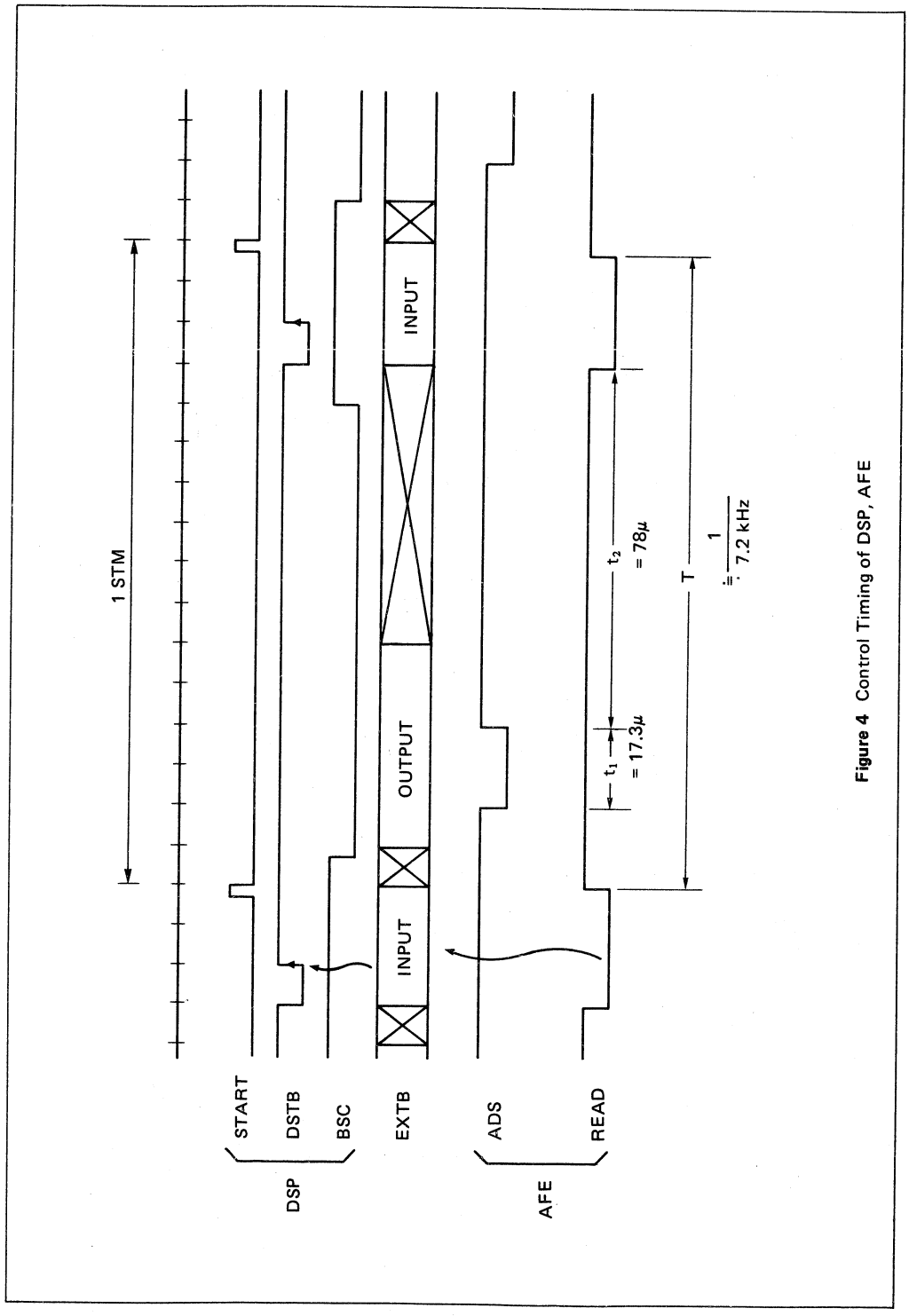


Figure 4 Control Timing of DSP, AFE

MSM6950

ANALOG FRONT END LSI

GENERAL DESCRIPTION

The MSM6950 is a analog front-end LSI which is fabricated by OKI's low power consumption CMOS silicon gate technology for modem chip set based on Bell 212A. CCITT V. 22 and CCITT V. 22 bis standard. The MSM6950 consists of two BPFs, for low band and high band, an A/D converter with 8-bit parallel output, a D/A converter with 8-bit parallel input, an AGC circuit controlled by external digital signals, a guard tone generator (550 Hz/1800 Hz selectable) and some analogue signal control switches for various applications.

The MSM6950 communicates with a modulator and a demodulator via each 8 bits parallel digital line.
This chip does not contain a carrier detect function but it will be performed with a digital signal processor dedicated to implement a demodulator by using digital signals from the A/D converter.

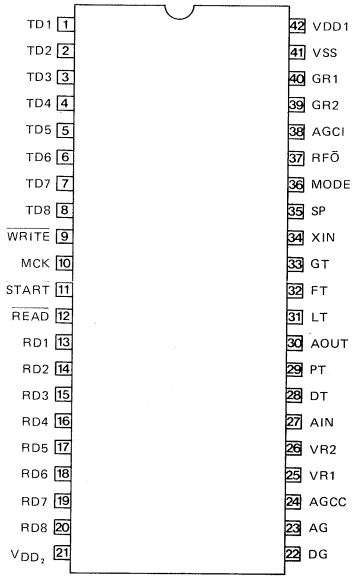
This device provides an analog signal input, an analog signal output and some signal-loop control inputs, and requires a 3.6864 MHz clock input to generate the operating time-base.

FEATURES

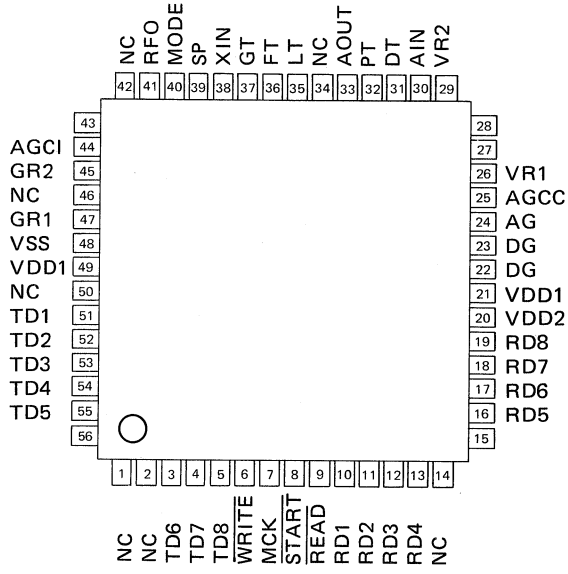
- Conforms to Bell 212A, 224 and CCITT V. 22 and V. 22 bis.
- 8-bit parallel output A/D converter and 8-bit parallel input D/A converter on chip.
- On-chip voltage reference.
- On-chip AGC circuit controlled by 8-bit external digital signal, over the received signal level range of 48 dB with 0.19 dB step.
- Dynamic range, 70 dB.
- Guard tone mixing function, 550 Hz or 1800 Hz.
- Selectable cut off frequency of transmitting for the guard tone, the DTMF tone and another, 725 Hz or 2900 Hz.
- Provides AC loop test function, a transmitting analog signal can be looped back as a receive analog signal within the chip.
- Supply voltage, ±5V.
- Low power dissipation, 80 mW.
- 3.6864 MHz external clock for operation.
- 42-pin plastic DIP package or 56-pin plastic flat package.

PIN CONFIGURATION (Top view)

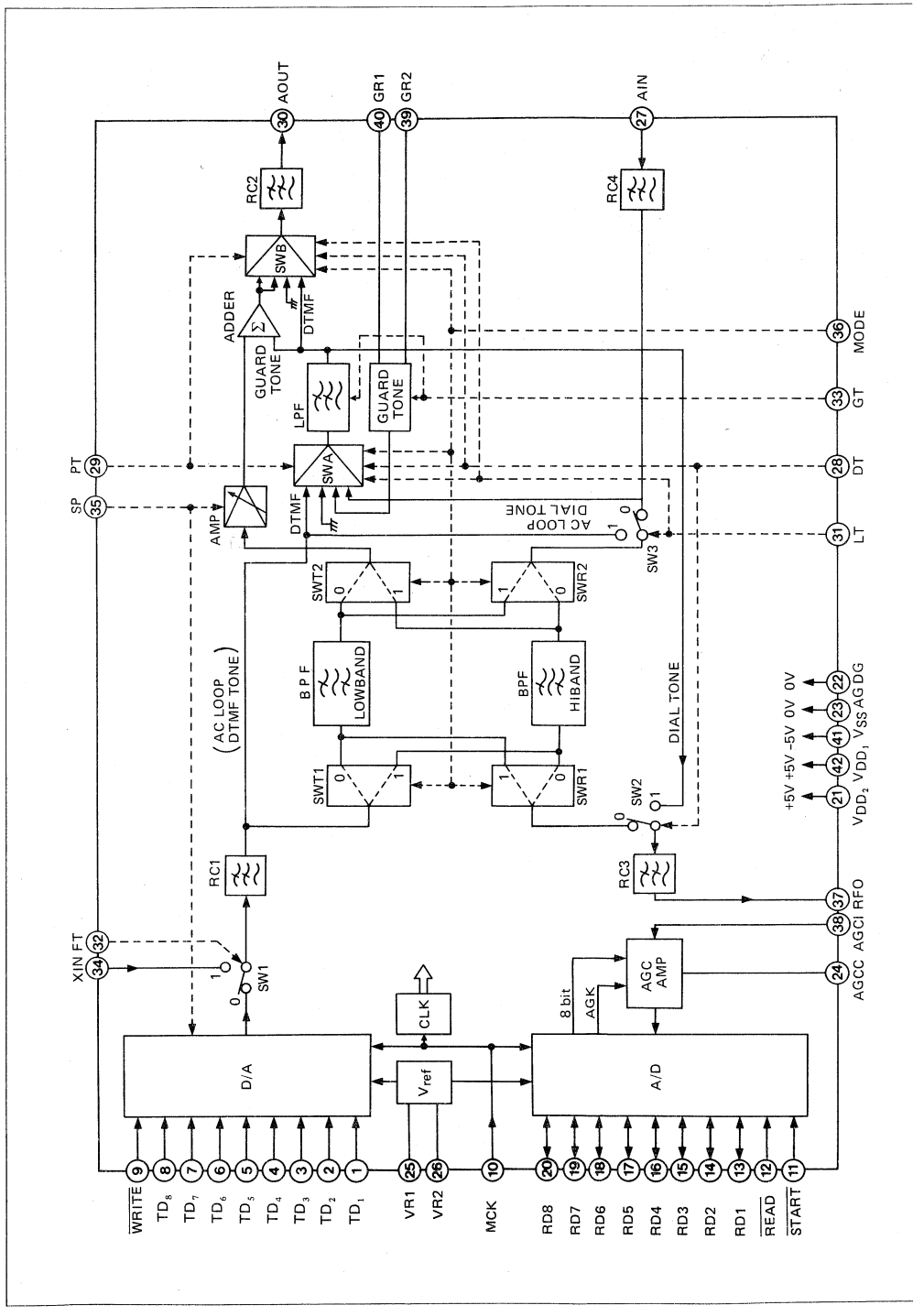
42 pin DIP (MSM6950RS)



56 pin FLAT (MSM6950GS)



BLOCK DIAGRAM



Pin Assignment

Pin Name	Pin No.		In/Out	Function	
	RS	GS			
TD1	1	51	Input	Transmit signal digital data input to DA (LSB)	
TD2	2	52	Input	Transmit signal digital data input to DA	
TD3	3	53	Input	Transmit signal digital data input to DA	
TD4	4	54	Input	Transmit signal digital data input to DA	
TD5	5	55	Input	Transmit signal digital data input to DA	
TD6	6	3	Input	Transmit signal digital data input to DA	
TD7	7	4	Input	Transmit signal digital data input to DA	
TD8	8	5	Input	Transmit signal digital data input to DA (MSB)	
$\overline{\text{WRITE}}$	9	6	Input	TD writing control signal for DA	
MCK	10	7	Input	Master clock input 3.6864 MHz	
$\overline{\text{START}}$	11	8	Input	Control signal for starting of AD conversion	
$\overline{\text{READ}}$	12	9	Input	RD reading control signal for AD	
RD1	13	10	In/Out	Receive signal digital data output from AD (LSB)	
RD2	14	11	In/Out	Receive signal digital data output from AD	
RD3	15	12	In/Out	Receive signal digital data output from AD	
RD4	16	13	In/Out	Receive signal digital data output from AD	
RD5	17	16	In/Out	Receive signal digital data output from AD	
RD6	18	17	In/Out	Receive signal digital data output from AD	
RD7	19	18	In/Out	Receive signal digital data output from AD	
RD8	20	19	In/Out	Receive signal sigital data output from AD (MSB)	
VDD2	21	20		Positive power supply (+5 V)	
DG	22	22,23		Digital ground (0 V)	
AG	23	24		Analog ground (0 V)	
AGCC	24	25		External capacitor terminal for AGC (0.1 μF)	
VR1	25	26	Input	External resistor terminal for reference voltage	
VR2	26	29	Output	External resistor terminal for reference voltage	
AIN	27	30	Input	Receive analog signal input	
DT	28	31	Input	Dial tone detecting loop	H
PT	29	32	Input	DTMF signal transmitting loop	H
AOUT	30	33	Output	Transmit analog signal output	
LT	31	35	Input	AC loop test	H
FT	32	36	Input	XIN enable (Filter test or External input)	H
GT	33	37	Input	Guard tone select (1800/550 Hz)	H/L
XIN	34	38	Input	External transmit analog signal input	
SP	35	39	Input	DA output PAM width select	
MODE	36	40	Input	Originate/Answer mode select	L/H
RFO	37	41	Output	Receive filter output	
AGCI	38	44	Input	AGC circuit input	
GR2	39	45	Output	External resistor terminal for Guard tone level	
GR1	40	47	Input	External resistor terminal for Guard tone level	
VSS	41	48		Negative power supply (−5 V)	
VDD1	42	21,49		Positive power supply (+5 V)	

ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	VDD		-0.3 ~ +7	V
	VSS		+0.3 ~ -7	
Analog input voltage	VIA		VSS - 0.3 ~ VDD + 0.3	
Digital input voltage	VID		-0.3 ~ VDD + 0.3	
Operating temperature	T_{OP}	—	-40 ~ + 85	°C
Storage temperature	T_{STG}	—	-55 ~ +150	

2. Recommended Operating Conditions

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Power Supply Voltage	V_{DD}	With Respect to AG or DG	4.75	5.00	5.25	V
	V_{SS}		-5.25	-5.00	-4.75	
	AG, DG	–	–	0	–	
Operating temperature	T_{OP}	–	0	–	70	°C
R_1	–	Transformer Impedance (Hybrid) $\left[\frac{600\ \Omega}{600\ \Omega}\right]$: 600 Ω	–	600	–	Ω
R_2	–		–	600	–	
R_3	–		–	300	–	
R_4	–	–	–	51	–	KΩ
R_5	–		–	51	–	
R_6	–		–	51	–	
R_7	–		–	51	–	
R_8	–		10	33	–	
R_9	–		–	36	–	
R_{10}	–		–	100	–	
R_{11}	–		–	51	–	
R_{12}	–		–	51	–	
C_1	–	–	–	2.2	–	μF
C_2	–		–	1	–	
C_3	–		–	0.1	–	
C_4	–		–	1	–	
C_5, C_7, C_9	–		–	10	–	
C_6, C_8	–		–	1	–	
$R_{13} \sim R_{20}$	–	–	–	20	–	KΩ
Reference Voltage	V_R	Adjusted by External Resistors	–	+2.50	–	V
Master Clock Frequency	F_{MCK}	–	3.6860	3.6864	3.6867	MHz
MCK Duty Cycle	D_{MCK}	50% to 50%	30	50	70	%
Digital Input Rise Time	T_R	$T_{D_1} \sim T_{D_8}$, $\overline{WRITE}$, $\overline{START}$, $\overline{READ}$, $R_{D_1} \sim R_{D_8}$, See Figure 1	0	–	50	nS
Digital Input Fall Time	T_F		0	–	50	nS

Parameter	Symbol	Condition	Min	Typ	Max	Unit
$\overline{\text{WRITE}}$ Period *1	T_{PW}	See Figure 2, 3	115	1/ 0.0072	143	μS
$\overline{\text{WRITE}}$ Width	T_{WW}		0.55	–	100	μS
$\overline{\text{START}}$ Period	T_{PS}		90	1/ 0.0072	143	μS
$\overline{\text{START}}$ Width	T_{WS}		1.1	–	79	μS
$\overline{\text{READ}}$ Width	T_{WR}		2.2	–	*2	μS
$\overline{\text{START}} \rightarrow \overline{\text{READ}}$ Timing	T_{SR}		80	–	*2	μS
$\overline{\text{READ}} \rightarrow \overline{\text{START}}$ Timing	T_{RS}		15	–	*2	μS
Allowable XIN Input DC Offset Voltage	V_{OSXIN}	–	-100	–	+100	mV
Allowable AIN Input DC Offset Voltage	V_{OSAIN}	–	-100	–	+100	mV

*1 Except for OKI's Special DPSK modulating mode (See APPLICATIONS INFORMATION 1-2)

*2 $T_{WR\ MAX} = T_{PS} - T_{SR} - T_{RS}$

$T_{SR\ MAX} = T_{PS} - T_{WR} - T_{RS}$

$T_{RS\ MAX} = T_{PS} - T_{WR} - T_{SR}$

Refer to Figure 9.

III

3. Power Dissipation

(V_{DD} = +5 V ±5%, V_{SS} = -5 V ±5%, T_a = 0 ~ 70°C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Positive Power Supply Current	I_{DD}	–	–	12	20	mA
Negative Power Supply Current	I_{SS}	–	–	11	20	mA

Note: V_{DD} means both of V_{DD1} and V_{DD2}.

4. Digital Interface

(V_{DD} = +5 V ±5%, V_{SS} = -5 V ±5%, T_a = 0 ~ 70°C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input Low Voltage	V_{IL}	—	0	—	0.6	V
Input High Voltage	V_{IH}	—	2.2	—	V_{DD}	V
Output Low Voltage	V_{OL}	I_{OL} = 0.36 mA	0	—	0.4	V
Output High Voltage	V_{OH}	I_{OH} = 20 μA	2.4	—	V_{DD}	V
Input Low Current	I_{IL}	$DG \leq V_{IN} \leq V_{IL}$	-10	—	10	μA
Input High Current	I_{IH}	$V_{IH} \leq V_{IN} \leq V_{DD}$	-10	—	10	μA
DA Data Set-up Time	T_{SD}	See Figure 3	0	—	—	μS
DA Data Hold Time	T_{HD}		1.1	—	—	μS
AGC Data Set-up Time	T_{SA}	See Figure 2	0	—	—	μS
AGC Data Hold Time	T_{HA}		2.2	—	—	μS
AD Data Output Delay Time	T_{D1}	Pull-up Resistor = 20 KΩ See Figure 2	0.4	—	3	μS
	T_{D2}		0.5	—	3	μS

III

5. Analog Interface

(V_{DD} = +5 V ±5%, V_{SS} = -5 V ±5%, T_a = 0 ~ 70°C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Reference Voltage						
Reference Voltage	V_R	Without Adjustment R8 = ∞	1.03	1.16	1.3	V
Transmit Analog Signal Characteristics (XIN, AOUT)						
Input Resistance	R_{XIN}	XIN	200	350	—	KΩ
Input Voltage	V_{XIN}	XIN	—	—	5	V_{PP}
Output Voltage	V_{AOUT}	$R_{AOUT} \geq$ 10 KΩ, $C_{AOUT} \leq$ 100 pF	5	—	—	V_{PP}
Load Resistance	R_{AOUT}	—	10	—	—	KΩ
Load Capacitance	C_{AOUT}	—	—	—	100	pF
DC Offset Voltage	V_{OST}	AOUT, XIN = 0 V	-1000	—	+1000	mV
Absolute Voltage Gain * — OKI's Special DPSK Mode	G_{T_1}	1,200 Hz, Originate	7.5	—	9.5	dB
	G_{T_2}	2,400 Hz, Answer	12.5	—	14.5	dB
	G_{T_3}	2,400 Hz, Answer with Guard Tone	11.5	—	13.5	dB
Absolute Voltage Gain * — FSK or Normal DPSK	G_{T_4}	1,200 Hz, Originate	1.0	—	3.0	dB
	G_{T_5}	2,400 Hz, Answer	0	—	2.0	dB
Absolute Voltage Gain * — Tone Transmit Mode	G_{T_6}	1,020 Hz	1.0	—	3.0	dB
Total Harmonic Distortion	T_{HDT}	—	—	-50	-40	dB
Idel Channel Noise	N_{IDLT}	Using a 0.3 ~ 3.4 KHz flat weighted filter	—	-44	—	dBm
Guard Tone — Frequency	F_{GT_1}	GT = V_{IL}	530	553.7	570	Hz
	F_{GT_2}	GT = V_{IH}	1,780	1,799.7	1,820	Hz
Guard Tone — Signal Level	V_{GT_1}	550 Hz, Without adjustment R_{11} = ∞	-13	-11	-9	dBm
	V_{GT_2}	1,800 Hz, Without adjustment R_{11} = ∞	-12	-10	-8	dBm
Guard Tone — Total Harmonic Distortion	T_{HDGT}	—	—	-50	-40	dB

*G_T = 20 log (V_{AOUT}/V_{XIN})
Note: 0 dBm = 0.775 Vrms

III

Receive Analog Signal Characteristics (A_{IN}, R_{FO})

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input Resistance	R_{AIN}	A_{IN}	200	350	–	KΩ
Input Voltage	V_{AIN}	A_{IN}	–	–	5	V_{PP}
Absolute Voltage Gain	G_R	1,200 Hz Answer 2,400 Hz Originate	-1	–	+1	dB
Output Voltage	V_{RFO}	$R_{RFO} \geq 10$ KΩ $C_{RFO} \leq 100$ pF	5	–	–	V_{PP}
Load Resistance	R_{RFO}	–	10	–	–	KΩ
Load Capacitance	C_{RFO}	–	–	–	100	pF
DC Offset Voltage	V_{OSR}	R_{FO}, A_{IN} = 0V	-500	–	+500	mV
Idle Channel Noise	N_{IDLR}	Using a 0.3 ~ 3.4 KHz flat weighted filter	–	-59	–	dBm
Total Harmonic Distortion	T_{HDR}	–	–	-50	-40	dB

6. Filter Transfer Characteristics

Low-band BPF

(V_{DD} = +5 V ±5%, V_{SS} = -5 V ±5%, T_a = 0 ~ 70°C)

Relative Voltage Gain to G_{FL_4}	G_{FL_1}	50 ~ 500 Hz	–	-44	-40	dB
	G_{FL_2}	555 Hz	–	-60	-48	dB
	G_{FL_3}	900Hz	-1	–	+1	dB
	G_{FL_4}	1,000 Hz	Referred Gain 0			dB
	G_{FL_5}	1,150 Hz	-1	–	+1	dB
	G_{FL_6}	1,350 Hz	-1	–	+1	dB
	G_{FL_7}	1,500 Hz	-1	–	+1	dB
	G_{FL_8}	1,800 Hz	–	-65	-45	dB
	G_{FL_9}	2400 Hz	–	-55	-50	dB
Group Delay Distortion	G_{DL}	900 ~ 1,500 Hz	–	–	100	μS

High-band BPF

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Relative Voltage Gain to G_{FH_4}	G_{FH_1}	≤ 1,500 Hz	—	-55	-50	dB
	G_{FH_2}	1,640 Hz	—	-55	-50	dB
	G_{FH_3}	2,050 Hz	-0.5	—	+1.5	dB
	G_{FH_4}	2,200 Hz	Referred Gain 0			dB
	G_{FH_5}	2,400 Hz	-1	—	+1	dB
	G_{FH_6}	2,600 Hz	-1	—	+1	dB
	G_{FH_7}	2,750 Hz	-0.2	—	+1.8	dB
	G_{FH_8}	3,210 Hz	—	-43	-40	dB
	G_{FH_9}	≥ 3,400 Hz	—	-35	-30	dB
Group Delay Distortion	G_{DH}	2,100 ~ 2,700 Hz	—	—	200	μS

Multip-purpose LPF

Parameter	Symbol	Condition		Min	Typ	Max	Unit
Absolute Voltage Gain	G_{LPF_1}	300 Hz	$G_T = V_{IL}$	-1.5	-0.5	+0.5	dB
	G_{LPF_2}	1,020 Hz	$G_T = V_{IL}$	-1	0	+1	dB
Relative Voltage Gain to G_{LPF_1}	G_{FLF_1}	0 ~ 200 Hz	$G_T = V_{IL}$	-1	—	+1	dB
	G_{FLF_2}	300 Hz		Referred Gain 0			dB
	G_{FLF_3}	750 Hz		-4	-3	-2	dB
	G_{FLF_4}	1,500 Hz		—	—	-30	dB
Relative Voltage Gain to G_{LPF_2}	G_{FHF_1}	0 ~ 80 Hz	$G_T = V_{IH}$	-1	—	+1	dB
	G_{FHF_2}	1,020 Hz		Referred Gain 0			dB
	G_{FHF_3}	3,000 Hz		-4	-3	-2	dB
	G_{FHF_4}	3,900 Hz		—	—	-10	dB

III

7. AGC Circuit and DA, AD Converters

(V_{DD} = +5 V ±5%, V_{SS} = -5 V ±5%, T_a = 0 ~ 70°C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
AGC Amplifier						
Input Resistance	R_{AGCI}	–	–	1	–	MΩ
Variable Voltage Gain Range	G_{AGC}	–	-4	–	+43.8	dB
Voltage Gain Accuracy	G_E		-0.4	+0.03 ~ -0.17	+0.4	dB
Output DC Offset Voltage	V_{OSAGC}		-60 (-3)	–	+60 (+3)	mV (LSB)
Transmit Digital to Analog Converter						
Bits of Resolution	B_{REST}	–	–	8	–	bit
End-point Linearity	NL_{DA}	–	–	0.36	0.5	%
Differential Non-linearity	DNL_{DA}	–	–	1/5	1/2	LSB
Full Scale – Plus Full Scale	PFV_{DA}	–	–	+2,481	–	mV
Full Scale – Minus Full Scale	NFV_{DA}	–	–	-2,500	–	mV
DC Offset Voltage	V_{OSDA}	–	-10	-1.5	+10	mV
Receive Analog to Digital Converter						
Bits of Resolution	B_{RESR}	–	–	8	–	bit
End-point Linearity	NL_{AD}	–	–	0.24	0.5	%
Differential Non-linearity	DNL_{AD}	–	–	1/5	1/2	LSB
Full Scale – Plus Full Scale	PFV_{AD}	–	–	+2,471	–	mV
Full Scale – Minus Full Scale	NFV_{DA}	–	–	-2,490	–	mV
DC Offset Voltage*	V_{OSAD}	–	-1/2	–	+1/2	LSB

* Only of AD converter. In practice, Output DC Offset is determined by V_{OSAGC} and the gain of AGC circuit.

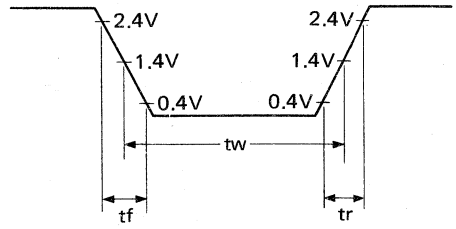


Figure 1 Definition of Rise/Fall Time

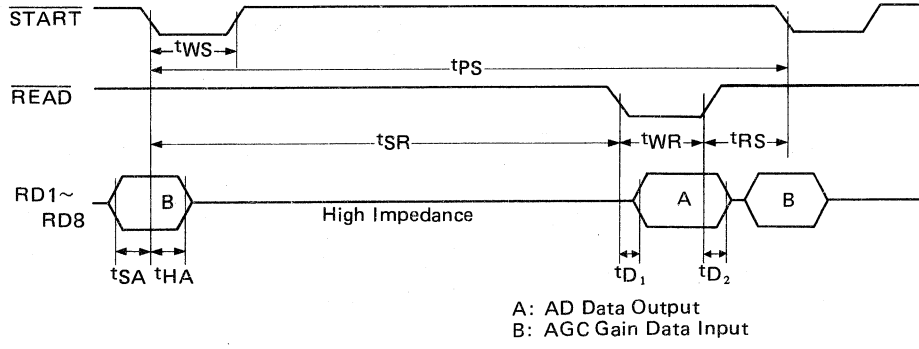


Figure 2 Receive Data Timing Chart

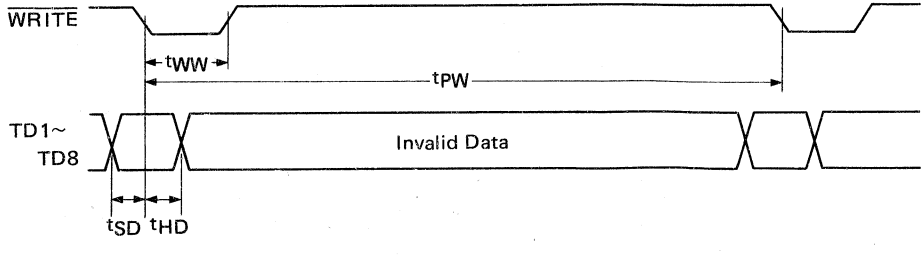


Figure 3 Transmit Data Timing Chart

III

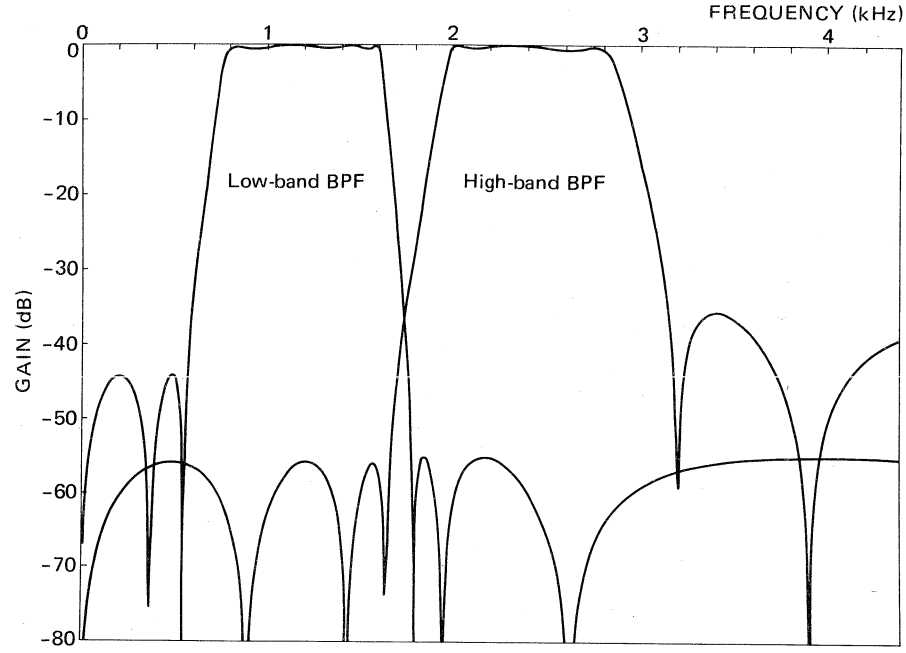


Figure 4 Low/High – band BPF FREQUENCY CHARACTERISTICS

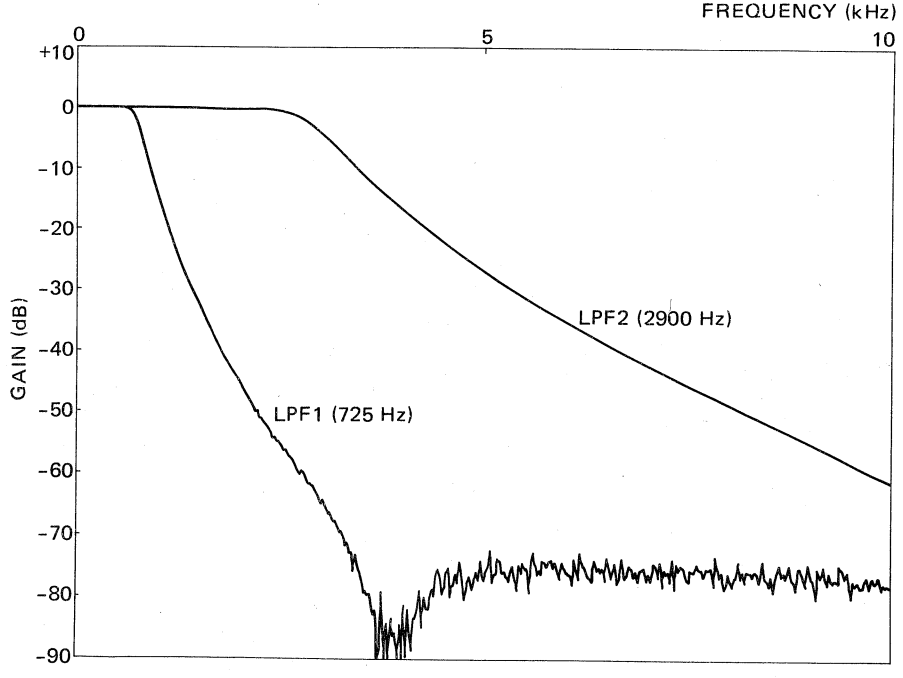
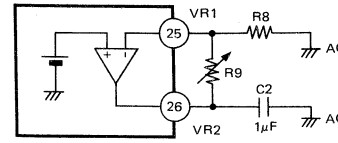


Figure 5 MULTI-PURPOSE LPF FREQUENCY CHARACTERISTICS

PIN DESCRIPTION

<table>
<tr><th rowspan="2">Pin Name</th><th colspan="2">Pin No.</th><th rowspan="2">Function</th></tr>
<tr><th>RS</th><th>GS</th></tr>
<tr><td>TD1 ~ TD8</td><td>1 ~ 8</td><td>3~5,
51~55</td><td>Transmit signal digital data input for DA conversion. These pins are 8 bit parallel two's complement data input pins. The data is loaded to the DA converter at the falling edge of $\overline{\text{WRITE}}$. TD1 is the LSB and TD8 is the MSB. Refer to Table 1 below.
<table>
<tr><th>TD</th><th>8</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>Total Value</th><th>Nominal Output Voltage*</th></tr>
<tr><td>Plus Full Scale</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>+127</td><td>+2,172.1 mV</td></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td>+126
~ 1</td><td></td></tr>
<tr><td>Plus 0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>Minus 0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>-1</td><td>-17.1 mV</td></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td>-2
~ 127</td><td></td></tr>
<tr><td>Minus Full Scale</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>-128</td><td>-2,189.2 mV</td></tr>
</table>
Table 1 *The reference voltage for AD conversion is +2.5 V. This output voltage is defined at A_{OUT}.</td></tr>
<tr><td>$\overline{\text{WRITE}}$</td><td>9</td><td>6</td><td>This signal enables TD1 ~ TD8 pins to write data into DA converter.
The digital input from TD1 ~ TD8 is latched to the DA converter at the falling edge of $\overline{\text{WRITE}}$ signal, and then converted to analog signal.
The analog output signal is renewed about 9 μsec after the falling edge of $\overline{\text{WRITE}}$ signal. The cycle of this signal can be chosen out of 115 μsec ~ 143 μsec.</td></tr>
<tr><td>MCK</td><td>10</td><td>7</td><td>A 3.6864 MHz clock signal should be applied to this pin. This is the time base for the operation of the MSM6950.</td></tr>
<tr><td>$\overline{\text{START}}$</td><td>11</td><td>8</td><td>This signal enables MSM6950 to start the AD conversion. This signal is also used to latch the input data used for setting the amplitude of the AGC circuit. The input data is supplied from a demodulating chip, the general performance of which is digital signal processing.
These two operations are performed at the falling edge of $\overline{\text{START}}$.
The cycle of this signal can be chosen out of 90 μsec ~ 143 μsec.</td></tr>
<tr><td>$\overline{\text{READ}}$</td><td>12</td><td>9</td><td>This is a control signal for 3-state output data bus line, RD1 ~ RD8. While this pin is at digital 0 state, the output bus is activated and the result of the AD conversion is output from RD1 ~ RD8 terminals.
While this pin is at digital 1 state, the output bus is inactivated and RD1 ~ RD8 become input terminals.</td></tr>
</table>

<table>
<tr><th rowspan="2">Pin Name</th><th colspan="2">Pin No.</th><th rowspan="2">Function</th></tr>
<tr><th>RS</th><th>GS</th></tr>
<tr><td>RD1 ~ RD8</td><td>13~20</td><td>10~13,
16~19</td><td>These are I/O terminals controlled by $\overline{START}$ and $\overline{READ}$ terminals.
When $\overline{READ}$ is set at digital 0 state, RD1 ~ RD8 become output terminals and the AD conversion result is output from these pins with 8 bit parallel two's compliment format. Refer to Table 2.
When $\overline{READ}$ is set at digital 1 state, RD1 ~ RD8 become input terminals. The data input to these pins is loaded into the registers at the falling edge of $\overline{START}$ signal. In this case, this data is used at the gain setting data for AGC circuit.
Nominal absolute voltage gain of AGC circuit is described in Table 3. The dynamic range of the AGC circuit is about 48 dB as shown in Table 3.
$\overline{READ}$ = Digital 0
<table>
<tr><th>RD_8</th><th>RD_7</th><th>RD_6</th><th>RD_5</th><th>RD_4</th><th>RD_3</th><th>RD_2</th><th>RD_1</th><th>Nominal Corresponding Voltage on the Input of AGC Circuit (AGCI)</th></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>+2,480.5 mV</td></tr>
<tr><td>⋮</td><td colspan="6">⟆</td><td></td><td>~ 19.5 mV Step</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>+19.5 mV</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>-19.5 mV</td></tr>
<tr><td>⋮</td><td colspan="6">⟆</td><td></td><td>~ 19.5 mV Step</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>-2,500 mV</td></tr>
</table>
Table 2
$\overline{READ}$ = Digital 1
<table>
<tr><th>RD_8</th><th>RD_7</th><th>RD_6</th><th>RD_5</th><th>RD_4</th><th>RD_3</th><th>RD_2</th><th>RD_1</th><th>Nominal Absolute Voltage Gain of AGC Circuit (dB)</th></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>+43.8</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>+43.6</td></tr>
<tr><td colspan="7">⟆</td><td>0.1875 dB Step</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>-3.63</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>-3.81</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>-4.00</td></tr>
</table>
Table 3</td></tr>
<tr><td>V_{DD_2}</td><td>21</td><td>20</td><td>Positive power supply, +5 V.
This power supply is internally connected to the digital output logical circuitry RD1 ~ RD8 to avoid the deterioration to the noise performance. Same power supply as to V_{DD_1} should be used.</td></tr>
<tr><td>DG</td><td>22</td><td>22,23</td><td>Digital ground level, 0 V.</td></tr>
<tr><td>AG</td><td>23</td><td>24</td><td>Analog ground level, 0 V.</td></tr>
<tr><td>AGCC</td><td>24</td><td>25</td><td>An external capacitor of more than 1 μF should be connected between AGCC and AG. This capacitor is necessary to compensate the DC offset voltage generated in the AGC circuit.</td></tr>
</table>

Pin Name	Pin No. RS	Pin No. GS	Function
VR1, VR2	25, 26	26, 29	The MSM6950 provides the voltage reference which is used for AD and DA convertions. The electrical potential is stabilized to variations of temperature or supply voltages, but tends to be different from chip to chip. Therefore, a external adjustment is necessary. The resistors used to adjust the reference voltage are connected to these pins as shown in Figure 6.  **Figure 6** (MSM6950RS) A bypass capacitor is required to keep this reference electrical in the silent condition. A capacitor with the value of more than 1 μF is recommended. The reference voltage on VR2 is determined by the following equation and the typical value is +2.5 V. $V_{REF} = 1.2 \times \frac{R_8 + R_9}{R_8}$ [volts]
AIN	27	30	Receive analog signal input pin. The maximum input level is about +7.2 dBm (5 Vp-p).
DT, PT	28, 29	31, 32	These pins control the transmit and receive analog signal paths for AC loop test, DTMF tone, guard tone and call progress tone. For details, refer to Table 9.
AOUT	30	33	This is the transmit analog signal output terminal. The output resistance is about 10 Ω and the load resistance should be more than 10 kΩ. The higher the road resistor is, the lower the power dissipation of MSM6950 becomes. When the full scale digital data is input to DA, the output voltage on AOUT becomes as follows. Input Data to DA / Reference Voltage / Output Voltage (AOUT) Plus Full Scale / +2.5 V / +2.17 V Minus Full Scale / +2.5 V / -2.19 V **Table 4**

<table>
<tr><th rowspan="2">Pin Name</th><th colspan="2">Pin No.</th><th rowspan="2">Function</th></tr>
<tr><th>RS</th><th>GS</th></tr>
<tr><td>LT</td><td>31</td><td>35</td><td>LT is used to provide the local AC loop test function.
When digital 1 is input to LT, the transmit analog signal bypasses the transmit bandpass filter and is directly routed to the receive bandpass filter. At this time, the transmit analog signal must be of the same channel with the receiver. The passband of the receive bandpass filter is selected by LT and MODE as shown in Table 5.
<table>
<tr><th>LT</th><th>MODE</th><th>Receive BPF's Passband</th><th>AIN</th><th>AOUT</th></tr>
<tr><td rowspan="2">1</td><td>0</td><td>2,000 ~ 2,800 Hz</td><td rowspan="2">Open</td><td rowspan="2">Shorted to AG (0V)</td></tr>
<tr><td>1</td><td>800 ~ 1,600 Hz</td></tr>
<tr><td>0</td><td>*</td><td colspan="3">Normal Operating State</td></tr>
</table>
Table 5</td></tr>
<tr><td>FT</td><td>32</td><td>36</td><td>FT controls the external transmit signal to be input to the MSM6950 and to send it over telephone line through the AOUT terminal. When FT is in digital 1 state, XIN is connected to the transmit filter input and external analog tones, such as DTMF tone, can be input to the MSM6950 through the XIN terminal.
When digital 0 is applied to FT, the output signal from DA converter is routed to the transmit filter input. This is the normal application for the MSM6950.</td></tr>
<tr><td>GT</td><td>33</td><td>37</td><td>GT controls the signal to select the frequency of the guard tone and this is a necessary function to be used internationally.
At the same time, the passband width of LPF is decided according to the frequency.
<table>
<tr><th>GT</th><th>Guard Tone Frequency</th><th>LPF's Passband</th></tr>
<tr><td>0</td><td>550 Hz</td><td>0 ~ 725 Hz</td></tr>
<tr><td>1</td><td>1,800 Hz</td><td>0 ~ 2,900 Hz</td></tr>
</table>
Table 6
LPF plays a role of rejecting harmonic components from the originated guard tone. In addition to it, this LPF can be also used in the receiver as the band limiting filter during call progress tone detection.</td></tr>
<tr><td>XIN</td><td>34</td><td>38</td><td>XIN is an external analog signal input. As described in the paragraph for FT, XIN is activated when FT is in digital 1 state. The maximum input level is about +7.2 dBm (5 Vp-p).</td></tr>
</table>

Pin Name	Pin No. RS	Pin No. GS	Function
SP	35	39	SP is a control signal input that determines the width of PAM signal output from DA and the voltage gain of the transmit amplifier. As the fundamental signal level changes according to the width of PAM signal, the compensation for the voltage gain is required to keep the transmit analog signal at a level. The advantage of the variable PAM width is effective in the special PSK modulating method devised by OKI. (Refer to APPLICATIONS INFORMATIONS 1-2 about this method) The width of PAM signal is determined by SP, LT and MODE as shown in Table 7.
MODE	36	40	MODE determines the role of each BPF by controlling SWT and SWR as shown in the circuit configuration. When digital 0 is applied to this pin, the low channel BPF is assigned to the transmitter and the high channel BPF is assigned to the receiver. This condition is called as "Originate mode". When digital 1 is input to MODE, the positions of BPFs are reversed and this is called as "Answer mode". During the AC loop back test, the frequency band used for this test becomes the receivers channel determined by MODE.
RFO	37	41	RFO is the analog signal output of the receive filter. This signal is to be connected to the AGC circuit through an external capacitor of more than 0.1 μF. The load resistance should be more than 10 kΩ. The maximum voltage swing is about 5 Vp-p.

SP	LT	Mode	PAM Signal Width	Operating Mode	
0	*	*	104 μS	Other Than Below Cases	
1	0	0	104 μS	OKI Original PSK Modulating Method	Data Transmission
1	0	1	52 μS		
1	1	0	52 μS		AC Loop-back Test
1	1	1	104 μS		

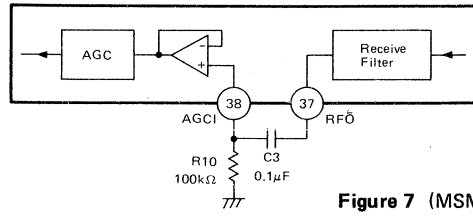
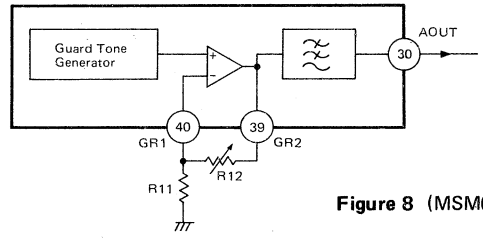
Table 7

The width could be 52 μs only when OKI's original PSK modulating method is applied in the higher frequency channel. In the FSK mode and in the normal PSK mode, SP should be in digital 0 state.

MODE	Mode	Transmit Filter	Receive Filter
0	Originate	L · BPF (800 ~ 1,600 Hz)	H · BPF (2,000 ~ 2,800 Hz)
1	Answer	H · BPF (2,000 ~ 2,800 Hz)	L · BPF (800 ~ 1,600 Hz)

Table 8

III

Pin Name	Pin No. RS	Pin No. GS	Function
AGCI	38	44	AGCI is the input pin of the AGC circuit and is connected to RFO through an external capacitor as shown in Figure 7. The role of the capacitor is to avoid a bad influence for the DC offset voltage generated in the receive filter. The input resistance is high and the maximum input voltage swing is about 5 Vp-p.  **Figure 7** (MSM6950RS)
GR2, GR1	39, 40	45, 47	The output guard tone level can be adjusted by using external resistors as shown in Figure 8.  **Figure 8** (MSM6950RS) The approximate output tone level is determined by the following equation. $$V_{AOUT} = 20 \cdot \log \frac{R_{11} + R_{12}}{R_{11}} - 14 \text{ [dBm]}$$ In Bell's standard sets, as the guard tone function is not applied, GR1 should be connected to GR2 directly.
VSS	41	48	Negative power supply pin. -5 V.
V_{DD1}	42	21, 49	Positive power supply pin. +5 V.

MSM6950RS CIRCUIT WIRING ILLUSTRATION (MSM6950RS)

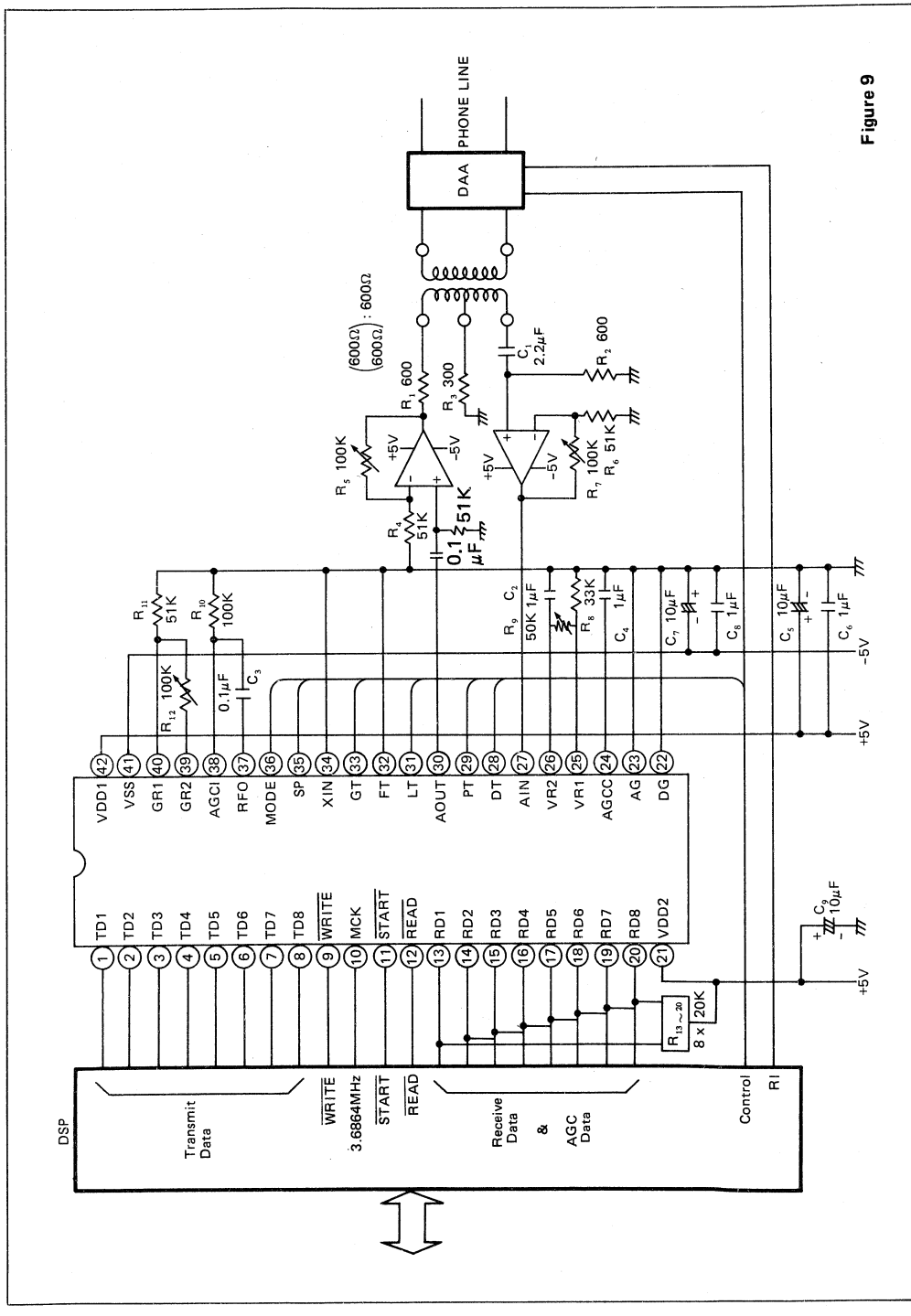


Figure 9

APPLICATIONS INFORMATION

1. Operating Modes

MSM6950 provides a variety of operating modes. By utilizing these operating modes of MSM6950, a superior modem system can be realized easily. The operating modes determined by some control pins are summarized in Table 9.

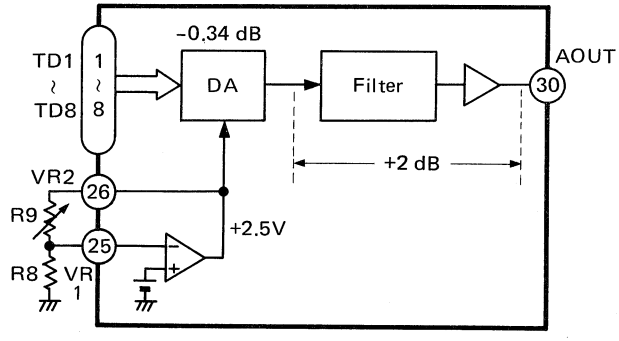
1-1 FSK and Normal PSK Mode

This mode is useful not only for normal applications that utilize DSP as modulator and demodulator, but also for the special application that uses only filtering functions of the MSM6950.

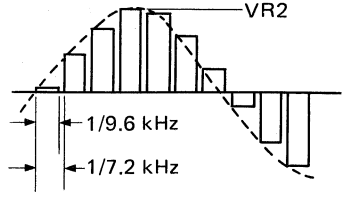
The sampling rate for DA and AD conversions — the same length as $\overline{\text{WRITE}}$ and $\overline{\text{START}}$ signal respectively — should be between 7 kHz and 9 kHz. Timing chart is shown in Figure 2 and Figure 3. In this mode, the wide of PAM signal derived from DA is to be set at 1/9.6 kHz. Therefore, when the sampling rate is 7.2 kHz, the amplitude of the fundamental component on DA's output is less than 2.5 dB compared with the PAM signal of 100% hold.

The signal level of a sine wave of 2.5 Vp-p is +7.2 dBm equivalent. Therefore, if the transmit filter has a voltage gain of +2.0 dB, and DA has a voltage gain of -0.34 dB, the transmit output signal level on AOUT becomes as follows.

$$V_{AOUT} = +7.2\ \text{dBm} - 2.5\ \text{dB} + 2.0\ \text{dB} - 0.34 = +6.36\ \text{dBm}$$



Output Wave Form of DA



$$20 \log \frac{7.2}{9.6} = -2.5\ [\text{dB}]$$

Figure 10 (MSM6950RS)

1-2 OKI's Special DPSK Mode

This is the special mode that can save the ROM size and number of processing step in the modulating processor. Normal DPSK and the special modulating method are shown in Figure 11 and 12, respectively.

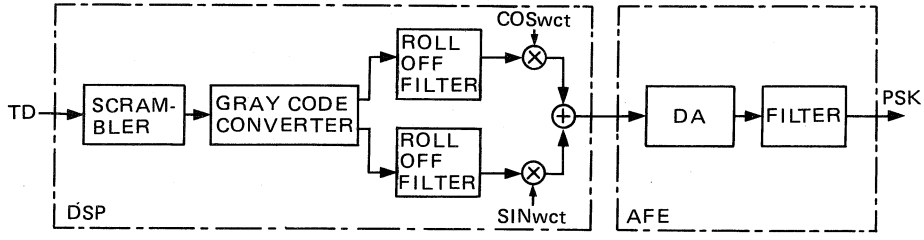


Figure 11

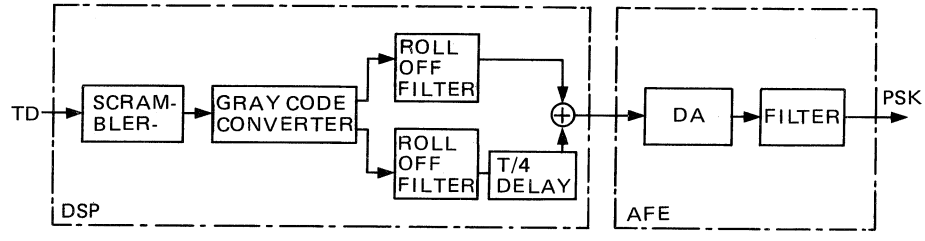


Figure 12

In the OKI's special DPSK mode, DSP is not required to perform multiplying of real part by COS wct and imaginary part by SIN wct. At the same time, as the coefficient table for multiplying is not required, the required ROM capacity of the DSP can be small. The special mode requires the special interface timing for handling the data of real and imaginary part from DSP to AFE to execute the equivalent processing in AFE. The data input timing for DA is as follows.

〈Originate Mode〉

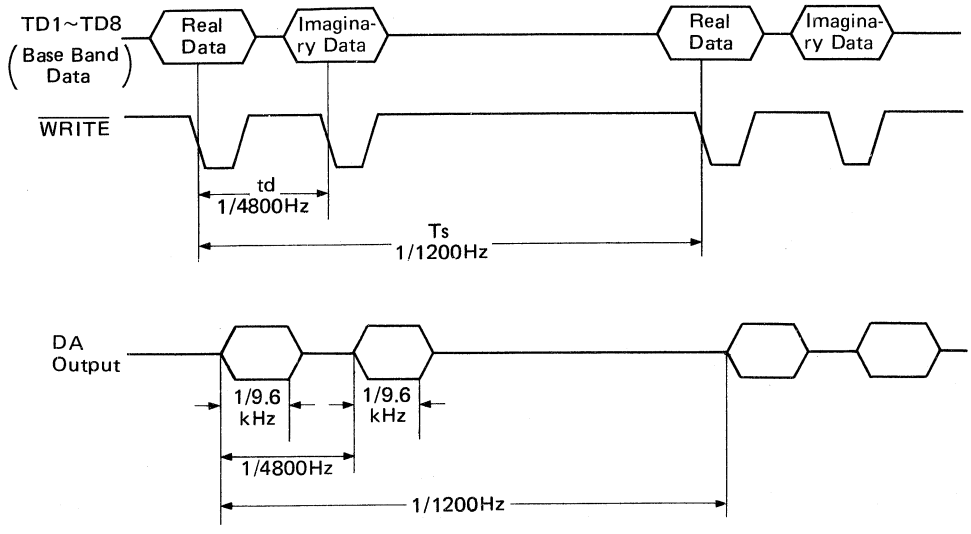


Figure 13

In the originate mode, the transmit carrier frequency is 1200 Hz. The interval between the real part data and the imaginary part data should be set at 1/4·fc (1/4·1200 Hz = 1/4800 Hz) to generate the carrier of SIN wct.

Using this method, the modulated signal, the carrier frequency of which is 1200 Hz, is obtained after filtering through the low channel BPF. The transmit output signal level on AOUT becomes as follows.

$$V_{AOUT} = +7.2\ \text{dBm} + \underbrace{20 \cdot \log 1/8}_{A} + \underbrace{20 \cdot \log \sqrt{2}}_{B} + \underbrace{6.0\ \text{dB}}_{C} + \underbrace{9\ \text{dB}}_{D} - \underbrace{0.34\ \text{dB}}_{E} = +6.81\ \text{dBm}$$

A: 1/8 PAM
B: Vector sum of real and imaginary part
C: Lower side band component after modulating
D: Voltage gain of the transmit filter (See Table 9)

The width of the PAM signal and the voltage gain are set automatically so as to satisfy the above equation.

〈Answer Mode〉

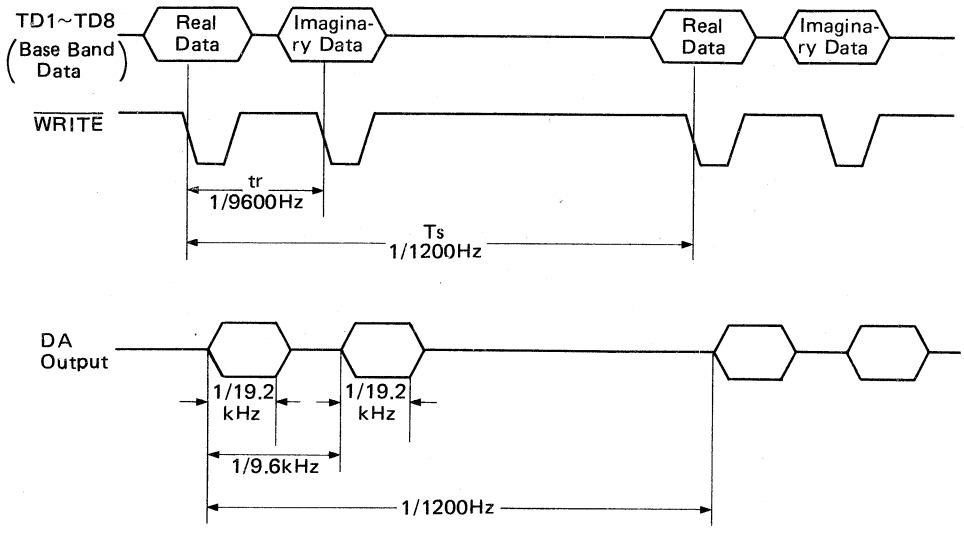


Figure 14

III

In the answer mode, the transmit carriver frequency is 2400 Hz.

Same as in the originate mode, the interval time should be set at 1/4·fc (1/4·2400 Hz = 1/9600 Hz). The modulated signal, the carrier frequency of which is 2400 Hz, is obtained after filtering through the high channel BPF.

The transmit output signal level on AOUT becomes as follows.

$$V_{AOUT} = +7.2\ dBm + 20 \cdot \log 1/16 + 20 \cdot \log \sqrt{2} + 6\ dB + 14.5\ dB - 0.34 = +6.26\ dBm$$

The width of the PAM signal and the voltage gain are set automatically internally.

When OKI's special modulating method is applied, there are some limitations about the transmit data on TD1 ~ TD8 and the timing of WRITE. But there are also many advantages about the modulator chip as described before.

1-3 Originate Transmission Mode

The low band signal must be transmitted and the high band signal must be received. MODE determines the positions of two BPFs by controlling SWT1, SWT2, SWR1 and SWR2. When MODE is in digital 0 state, the low channel BPF is assigned to the transmitter and the high channel BPF is assigned to the receiver. Both DT and PT should be in digital 1 state so that the guard tone function should be disabled.

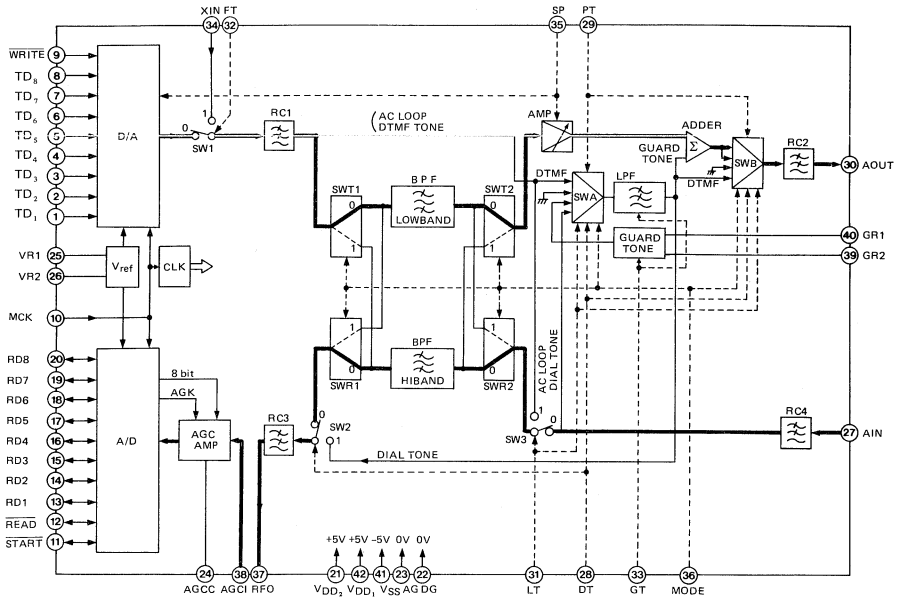


Figure 15 (MSM6950RS)

1-4 Answer Transmission Mode

The high band signal must be transmitted and the low band signal must be received. When MODE is in digital 1 state, the high channel BPF is assigned to the transmitter and the low channel BPF is assigned to the receiver. In some applications, it is required to mix a guard tone to the high channel transmit signal in the answer mode. The control signals on DT, PT and GT determine the guard tone function. When DT and PT are in digital 1 state, the guard tone function is disabled and only the high channel transmitter is enabled. When DT, PT and GT are in digital 0 state, the guard tone, the frequency of which is 550 Hz, is mixed to the transmit signal.

When GT is changed to digital 1 keeping DT and PT in digital 0 state, another guard tone, the frequency of which is 1800 Hz, is mixed to the transmit signal.

The original guard tone is filtered through LPF and only its fundamental component is extracted and mixed to the transmit signal. The cut-off frequency of LPF is about 725 Hz while GT is in digital 0 state and becomes about 2900 Hz while GT is in digital 1 state.

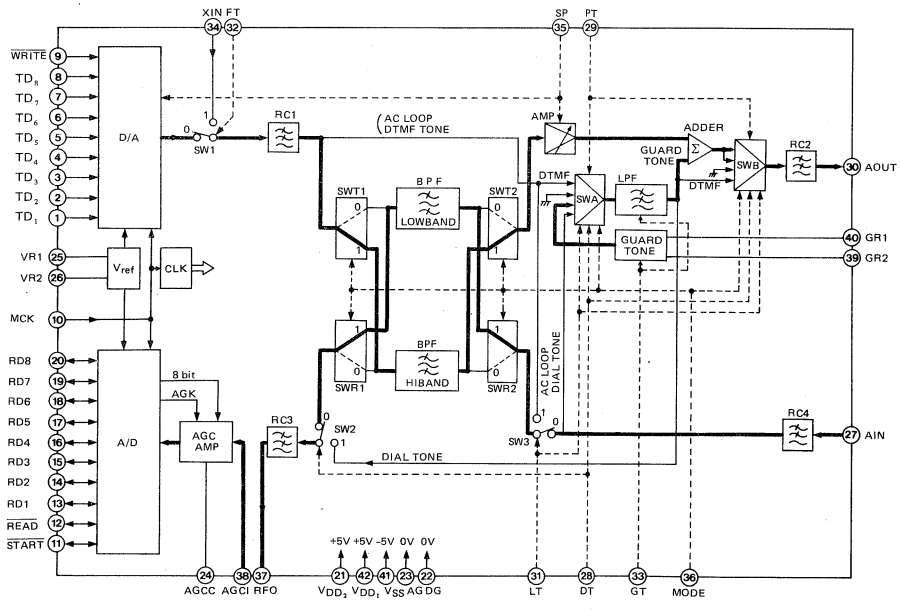


Figure 16 (MSM6950RS)

1-5 Tone Transmit Mode

The signal path in this mode is shown in Figure 17.

LPF put in this route has two kinds of its cut-off frequency (725 Hz/2900 Hz). So, this mode is effective in DTMF signaling and so forth. Refer to Table 9.

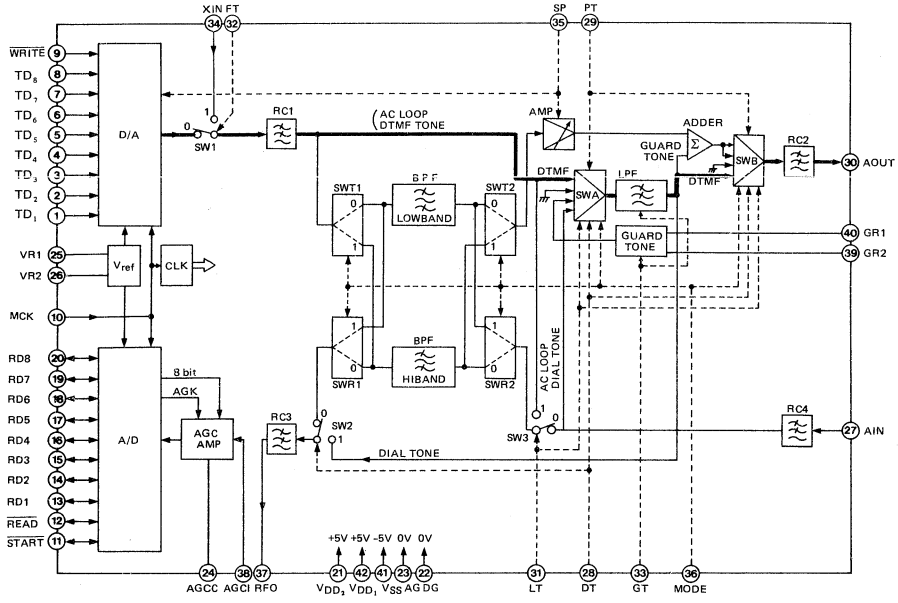


Figure 17 (MSM6950RS)

1-6 Tone Receive Mode

The signal path in this mode is shown in Figure 18.

As LPF put in this route has two kinds of cut-off frequency – 725 Hz and 2900 Hz, this mode is effective for call progress tone monitoring, such as for tone dialing. Refer to Table 9. In this mode, AOUT is connected to AG (0V) internally.

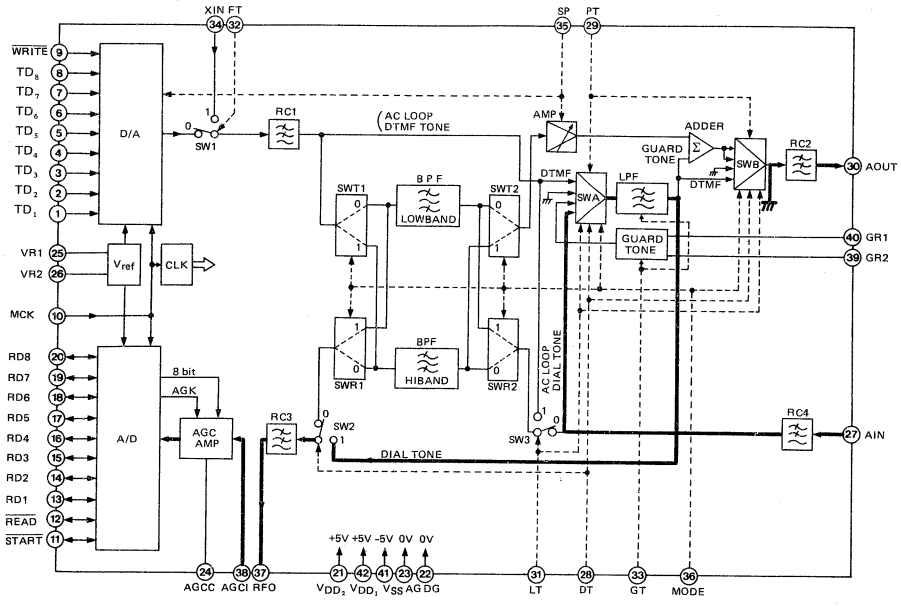


Figure 18 (MSM6950RS)

1-7 AC Loop-back Test Mode

The signal path in this mode is shown in Figure 19.

The modem system has to receive its own transmit signal to check the modem operation.

In this mode, the transmit BPF is skipped from the signal route and the channel used for AC Loop-back test determined by the receiver's channel determined by MODE. Refer to Table 9.

AOUT is connected to AG (0V) internally.

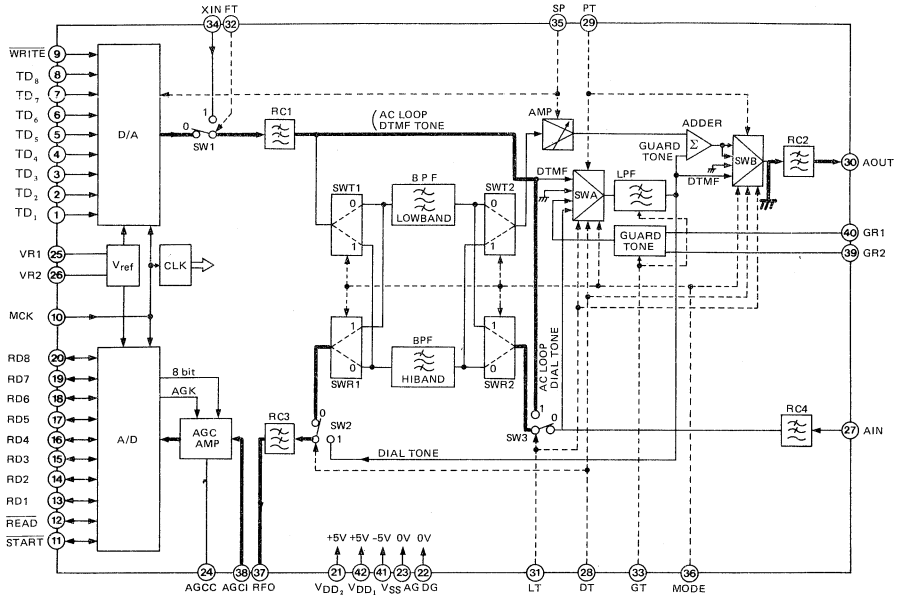


Figure 19 (MSM6950RS)

Control Signal						Transmitter				Receiver		Note	
DT	PT	MODE	GT	SP	LT	Pass Band*1	Gain*1	Guard Tone	DA-PAM Width	Pass Band*2	Gain*2		
1	1	0	X	0	0	800~1600Hz	+2.0dB		104μs	2000~2800Hz	0dB	Originate	FSK DPSK
1	1	1	X	0	0	2000~2800Hz	+2.0dB			800~1600Hz	0dB	Answer	
0	0	1	0	0	0	2000~2800Hz	+2.0dB	550Hz		800~1600Hz	0dB		
0	0	1	1	0	0	2000~2800Hz	+2.0dB	1800Hz		800~1600Hz	0dB		
1	1	0	X	1	0	800~1600Hz	+9dB		104μs	2000~2800Hz	0dB	Originate	OKI's Special DPSK
1	1	1	X	1	0	2000~2800Hz	+14.5dB		52μs	800~1600Hz	0dB	Answer	
0	0	1	0	1	0	2000~2800Hz	+13.5dB	550Hz		800~1600Hz	0dB		
0	0	1	1	1	0	2000~2800Hz	+13.5dB	1800Hz		800~1600Hz	0dB		
0	1	0	0	0	0	0~ 725Hz	-0.5dB		104μs	2000~2800Hz	0dB	Guard Tone/DTMF Tone Transmitting	
0	1	1	0	0	0	0~ 725Hz	-0.5dB			800~1600Hz	0dB		
0	1	0	1	0	0	0~2900Hz	0dB			2000~2800Hz	0dB		
0	1	1	1	0	0	0~2900Hz	0dB			800~1600Hz	0dB		
1	0	X	0	X	0					0~ 725Hz	0dB	Filtering for Call Progress Tone	
1	0	X	1	X	0					0~2900Hz	0dB		
X	X	0	X	0	1	*3 (0~10KHz)	(0dB)		104μs	2000~2800Hz	0dB	AC Loop-back Test	FSK DPSK
X	X	1	X	0	1	*3 (0~10KHz)	(0dB)			800~1600Hz	0dB		
X	X	0	X	1	1	*3 (0~10KHz)	(0dB)		52μs	2000~2800Hz	0dB		OKI's Special DPSK
X	X	1	X	1	1	*3 (0~10KHz)	(0dB)		104μs	800~1600Hz	0dB		

*1 XIN → AOUT
*2 AIN → RFO
*3 AOUT is connected to Ground.

Table 9. Various Operating Modes

2. Considerations for duplexer (Line Hybrid Using Op. Amps)

In case of full-duplex systems, a duplexer plays a important role. Its purpose is to help reject transmit signal energy from the receive signal.

Theoretically, a duplexer can be adjusted to achieve infinite rejection (no existence of cross-talk) — where the phase and amplitude of the inverting and non-inverting signals cancel through the duplexer OP-Amps. In practice however, telephone line impedances vary enough such that only about 10 ~ 15 dB of rejection can be expected. To attain this rejection, it is recommended that the duplexer components (R_1, R_2, R_3 and C_1 in Figure 20) be tuned for the impedance and loss characteristics of the particular type of transformer being used. This will minimize the impedance variation of the line.

Once these component values have been determined for a particular transformer type, further trimming is usally unnecessary on a board-to-board basis. A recommended procedure for balancing the duplexer, which was used in finding the values in Figure 20, is as follows.

a) A recommended procedure for balancing the duplexer

① First, set the chip into the transmit squelch mode. Next, connect a 600 ohm signal source to points A and B (the signal source; -12 dBm and 1200 Hz). Tweak R_1 until the loss at point A and B is exactly 6 dB. This allows maximum power transfer through the transformer.

② With R_1 at this new value, replace the signal source with a 600 ohm resistor at point A and B. Now output the transmit signal from AOUT via OPA1 at the frequency of 1200 Hz.

③ Now tune R_3 until the signal out of AOUT reaches a minimum at OPA2 output terminal (V_2'). Then tune C_1 until a new, lower minimum is reached which should be around 30 dB.

The phase and amplitude of the two signal components have now been matched for the best rejection over the spread of telephone lines.

A crosstalk characteristic of the duplexer adjusted in steps ① through ③ is shown in Figure 21. It was obtained by measuring the V_0-to-V_2 transfer characteristic with the modem chip and the duplexer disconnected from each other.

The duplexer has the attenuation pole at about 1420 Hz when a line impedance is ideal 600 ohm.

b) Characteristics on an practical line

Figure 21 also shows the practical characteristics of the duplexer connected to existing telephone lines.

These are represented by V_0-to-V_2 transfer characteristics; it should be noticed that the receive signal level at AIN terminal (V_3) will be lower than V_2 by about 6 dB typically because of the existence of R_6 and R_7.

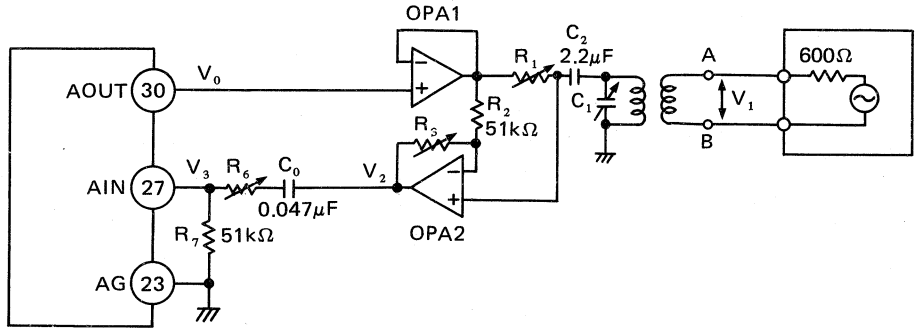
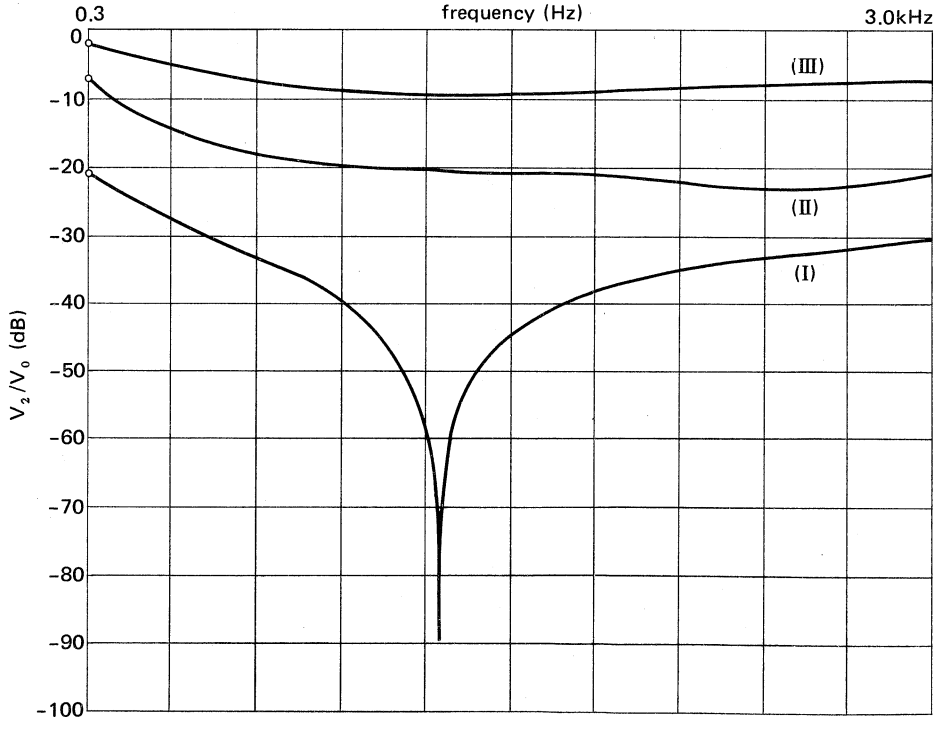


Figure 20 Duplexer (Line Hybrid Circuit) Considerations (MSM6950RS)



(I) Terminal by 600Ω pure resistor
(II) Connected to a private phone line
(III) Connected to a public switched network

Figure 21 Experimental Cross-Talk Characteristics

III

Preliminary

OKI semiconductor

MSM6949

ANALOG FRONT END LSI

GENERAL DESCRIPTION

The MSM6949 is an analog front end LSI which is fabricated by OKI's low power consumption CMOS silicon gate technology. The MSM6949 is used to implement an analog front end function required in the modem set based on CCITT V. 26, V. 27 and V. 29 recommendations.

The MSM6949 performs all basic analog signal processing functions such as transmit and receive filters, selectable amplitude equalizers, transmit signal level attenuator, fast carrier detector, AD and DA converter with 8-bit parallel input/output.

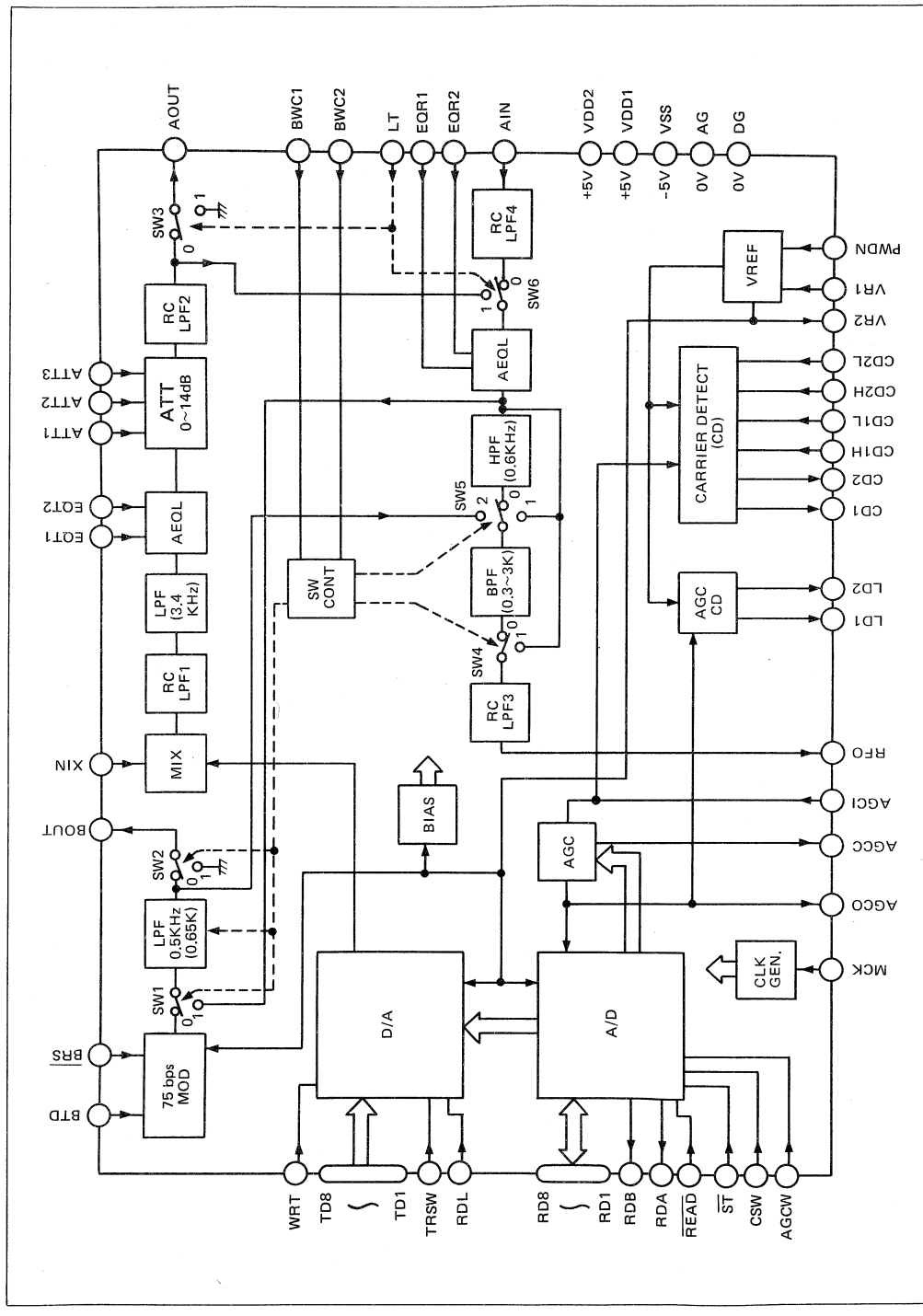
In addition to it, the MSM6949 performs analog loop test, the detection of call progress tones, 75 bps backward channel transmitter and automatic gain control (AGC). AGC circuit is digitally controlled by the digital signal processor which performs the demodulating function.

By utilizing the MSM6949 together with OKI's digital signal processors, a cost effective modem can be designed easily.

FEATURES

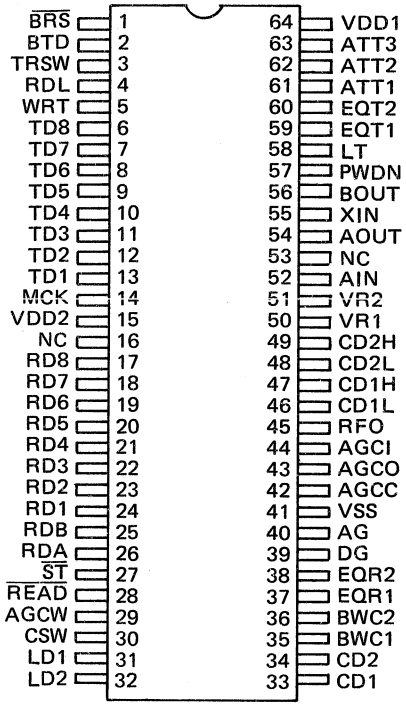
- Performs all analog signal processing functions required for CCITT V. 26, V. 27 and V. 29.
- 75 bps backward channel FSK transmitter.
- Interfaces to digital signal processors with receive and transmit parallel data bus.
- Call progress tone monitoring.
- An chip AGC circuit controlled by external digital signals, over the received signal level range of 51 dB with 0.2 dB step.
- Analog loop test: A transmitting analog signal can be looped back as a receive analog signal within the chip.
- A set of carrier detection circuits, the on/off levels of which, are fixed at each of the compromised values within the chip, and also can be adjusted by external resistors.
- Two CD circuits are useful for Fall-Back operation and so forth.
- 3.456 MHz external clock for operation.
- On-chip voltage reference.
- Few external components required.
- Supply voltage, ±5V.
- Low power dissipation: 140 mW typical.
- Power stand by mode available.
- 64 pin mini-size DIP, 68 pin PLCC will be available by 1Q '87.

BLOCK DIAGRAM



PIN CONFIGURATION (Top View)

64 pin mini DIP (MSM6949SS)



68 pin PLCC (MSM6949JS): Available by 1Q '87.

PIN ASSIGNMENTS (SS --- 64 pin mini-size DIP, JS --- 68 pin PLCC)

Pin Name	Pin No.		Function	
	SS	JS		
$\overline{BRS}$	1		Request to Send for backward channel (V.23)	
BTD	2		Transmit Data for backward channel (V.23)	
TRSW	3		Control signal for connection of DA input bus	
RDL	4		Latch clock for RD to input to DA within chip	
WRT	5		Control signal for writing TD to DA	
TD8	6		Transmit signal digital data bus input to DA	MSB
TD7	7			—
TD6	8			—
TD5	9			—
TD4	10			—
TD3	11			—
TD2	12			—
TD1	13			LSB
MCK	14		Master clock input 3.456 MHz	
VDD2	15		+5V power supply	
N.C.	16			
RD8	17		Receive signal digital data bus output from AD (3-state I/O)	MSB
RD7	18			—
RD6	19			—
RD5	20			—
RD4	21			—
RD3	22			—
RD2	23			—
RD1	24			LSB
RDB	25		Additional digit for RD bit shifting (3-state output)	
RDA	26			
$\overline{ST}$	27		Control signal for starting of AD conversion	
$\overline{READ}$	28		Control signal for reading RD from AD	
AGCW	29		Writing clock for setting data to AGC circuit	
CSW	30		RD bit shifting enable	
LD1	31		Outputs of level comparators put to AGC circuit's output. These are used to set AGC at typical gain when detecting urgent changes.	
LD2	32			
CD1	33		Carrier detect for QAM/PSK signal	
CD2	34		Carrier detect for FSK signal (T.30)	

III

Pin Name	Pin No.		Function
	SS	JS	
BWC1	35		Receive filter bandwidth select
BWC2	36		
EQR1	37		Fixed compromise cable amplitude equalization select for receiving
EQR2	38		
DG	39		Digital ground (0V)
AG	40		Analog ground (0V)
VSS	41		–5V power supply
AGCC	42		External capacitor terminal for AGC circuit
AGCO	43		AGC circuit output
AGCI	44		AGC circuit input connected for RFO through external capacitor
RFO	45		Receive filter output connected to AGCI through external capacitor
CD1L	46		Carrier detect level select for CD1
CD1H	47		
CD2L	48		Carrier detect level select for CD2
CD2H	49		
VR1	50		On-chip reference voltage adjust using external resistors
VR2	51		
AIN	52		Receive analog signal input
N.C.	53		
AOUT	54		Transmit analog signal output
XIN	55		External analog signal input
BOUT	56		75 bps FSK transmit signal output
PWDN	57		Power down mode select
LT	58		Analog loop test
EQT1	59		Fixed compromise cable amplitude equalization select for transmitting
EQT2	60		
ATT1	61		8 steps attenuator select for transmit signal level
ATT2	62		
ATT3	63		
VDD1	64		+5V power supply

ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Parameter	Symbol	Condition	Ratings	Unit
Power supply voltage	V_{DD}	T_a = 25°C With respect to AG or DG	-0.3 ~ +7	V
	V_{SS}		-7 ~ +0.3	
Analog input voltage	V_{IA}		V_{SS}-0.3 ~ V_{DD}+0.3	
Digital input voltage	V_{ID}		-0.3 ~ V_{DD}+0.3	
Operating temperature	T_{OP}	–	-40 ~ 85	°C
Storage temperature	T_{STG}	–	-55 ~ 150	

2. Recommended Operating Conditions

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Power Supply Voltage	V_{DD}	With respect to AG or DG	4.75	5.00	5.25	V
	V_{SS}		-5.25	-5.00	-4.75	
	AG, DG	–	–	0	–	
Operating Temperature	T_{OP}	–	0	–	70	°C
R1	–	Transformer impedance (Hybrid) $\frac{600\Omega}{600\Omega}$: 600Ω	–	600	–	Ω
R2	–		–	600	–	
R3	–		–	300	–	
R4	–	–	–	51	–	kΩ
R5	–		–	51	–	
R6	–		–	51	–	
R7	–		–	51	–	
R8	–		10	33	–	
R9	–		–	36	–	
C1	–	–	–	2.2	–	μF
C2	–		–	1	–	
C3	–		–	0.1	–	
C4	–		–	1	–	
C5, C7, C9	–		–	10	–	
C6, C8	–		–	1	–	
R10 ~ R17	–	–	–	10	–	kΩ
Reference Voltage	V_{REF}	Ajusted by External Resistors	–	+2.50	–	V
Master Clock Frequency	f_{MCK}		3.4557	3.456	3.4563	MHz
MCK Duty Cycle	D_{MCK}	50% to 50%	30	50	70	%
Digital Input Rise Time	t_r	$\overline{RDL}$, WRT, MCK, $\overline{ST}$, $\overline{READ}$, AGCW See Figure 1	0	–	50	ns
Digital Input Fall Time	t_f		0	–	50	ns
$\overline{ST}$ Period	t_{PS}	See Figure 2, 3	51	–	143	μs
$\overline{ST}$ Width	t_{WS}		0.3	–	t_{PS}-0.3	μs
$\overline{READ}$ Width	t_{WRE}		0.3	–	–	μs

Parameter	Symbol	Condition	Min	Typ	Max	Unit
$\overline{ST} \rightarrow \overline{READ}$ Timing	t_{SR}	See Figure 2, 3	51	–	$t_{PS}+50$	μs
$\overline{ST} \rightarrow$ AGCW Timing	t_{SA}		5	–	$t_{PS}-10$	μs
AGCW Width	t_{WA}		0.3	–	$t_{PS}-0.3$	μs
WRT Period	t_{PW}		20	–	143	μs
WRT Width	t_{WW}		0.3	–	$t_{PW}-0.3$	μs
RDL Period	t_{PRD}	See Figure 3	20	–	143	μs
RDL Width	t_{WRD}		0.3	–	$t_{PRD}-0.3$	μs
RDL → WRT Timing	t_{RDW}		0	–	$t_{PRD}-0.6$	μs
Allowable XIN Input DC Offset Voltage	V_{OSXIN}	–	-100	–	+100	mV
Allowable AIN Input DC Offset Voltage	V_{OSAIN}	–	-100	–	+100	mV

Refer to Figure 16.

III

3. Power Dissipation

(V_{DD} = +5V ±5%, V_{SS} = -5V ±5%, T_a = 0 ~ 70°C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Power-Down Current	I_{DDS}	PDWN = 1	–	0.2	0.5	mA
	I_{SSS}		–	0.2	0.5	mA
Active Current	I_{DD}	PDWN = 0	–	14	25	mA
	I_{SS}		–	13	25	mA

NOTE) V_{DD} means both of V_{DD1} and V_{DD2}.

4. Digital Interface

(V_{DD} = +5V ±5%, V_{SS} = -5V ±5%, T_a = 0 ~ 70°C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input Low Voltage	V_{IL}	–	0	–	0.6	V
Input High Voltage	V_{IH}	–	2.2	–	V_{DD}	V
Output Low Voltage	V_{OL}	I_{OL} = 0.4 mA	0	–	0.4	V
Output High Voltage	V_{OH}	I_{OH} = 20 μA	2.4	–	V_{DD}	V
Input Low Current	I_{IL}	DG ≤ V_{IN} ≤ V_{IL}	-10	–	10	μA
Input High Current	I_{IH}	V_{IH} ≤ V_{IN} ≤ V_{DD}	-10	–	10	μA
TD Data Set-up Time	t_{STD}	See Figure 2, 3	100	–	–	ns
TD Data Hold Time	t_{HTD}		100	–	–	ns
AGC Data Set-up Time	t_{SAG}		100	–	–	ns
AGC Data Hold Time	t_{HAG}		100	–	–	ns
RD Data Set-up Time	t_{SRD}	See Figure 3	100	–	–	ns
RD Data Hold Time	t_{HRD}		100	–	–	ns
AD Data Output Delay Time	t_{D1}	See Figure 2, 3	–	–	300	ns
	t_{D2}		–	–	300	ns

5. Analog Interface

(V_{DD} = +5V ±5%, V_{SS} = -5V ±5%, T_a = 0 ~ 70°C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Reference Voltage						
Reference Voltage	VR	Without adjustment $R_s = \infty$	+1.02	+1.20	+1.38	V
Backward Channel Transmit Signal Output (BOUT), External Signal Input (XIN)						
Output Resistance	R_{OB}	BOUT —	—	10	20	Ω
Load Resistance	R_{BOUT}	BOUT —	10	—	—	kΩ
Load Capacitance	C_{BOUT}	BOUT —	—	—	100	PF
DC Offset Voltage	V_{OSB}	BOUT —	-200	—	+200	mV
Output Carrier Level	V_{BOUT}	BOUT $R_{BOUT} \geq 10$ kΩ, V_{REF} = +2.50 V	1.74 -2	2.19 0	2.76 2	Vpp dBm
BWC Transmit Signal Level Ratio	L_{RBWC}	$\frac{V_{AOUT}\ (450\ Hz)}{V_{AOUT}\ (390\ Hz)}$	-1	0	1	dB
BWC Transmit Carrier Frequency — Mark "1"	f_{OBM}	BTD = 0	389	390	391	Hz
BWC Transmit Carrier Frequency — Space "0"	f_{OBS}	BTD = 1	449	450	451	Hz
Input Resistance	R_{XIN}	XIN —	25	50	—	kΩ
Input Signal Level	V_{XIN}	XIN —	—	—	4.38 +6	Vpp dBm

NOTE) 0 dBm = 0.775 Vrms = 2.19 Vpp

Transmit Analog Signal Ouput (AOUT)

Output Resistance		R_{OT}	—	—	10	20	Ω
Load Resistance		R_{AOUT}	—	10	—	—	kΩ
Load Capacitance		C_{AOUT}	—	—	—	100	PF
DC Offset Voltage		V_{OST}	XIN = AG	-200	—	+200	mV
Transmit Level (Single Tone)	Forward* Channel	V_{AOUT}	EQT1 = 1, EQT2 = 1, ATT1 = 1, ATT2 = 1, ATT3 = 1, V_{REF} = +2.50 V; f_{IN} 1.8 kHz Full scale	3.48 +4	4.38 +6	5.52 +8	Vpp dBm
Idle Channel Noise		N_{IDLT}	Using a 0.3 ~ 3.4 kHz flat weighted filter	—	-80	—	dBm
Total Harmonic Distortion		T_{HDT}	—	—	-65	-50	dB

III

* Transmit data (TD1~TD8) determine this level essentially. If the DA converter sends a single sine wave signal of which amplitude is ±2.5 Vop (Full scale of DA converter, equivalent +7 dBm) to the transmit filter, the transmit signal level at AOUT becomes +6 dBm (4.37 Vpp). But, generally in PSK or QAM modulation, maximum peak factor of about 3 dB or 7 dB should be considered in the design. Therefore, for instance, the transmit signal in the QAM forward channel is designed to be -1 dBm. This value shows one example of designs.

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Receive Analog Signal Input (AIN)						
Input Resistance	R_{AIN}	–	100	–	–	kΩ
Receive Signal Level Range (Single Tone)	V_{AIN}	Single Tone	4.36		1095	mVo-p
		Allows the level increase by PSK or QAM modulation.	-48	–	0	dBm
Receive Filter Output (RFO)						
Output Resistance	R_{OR}	–	–	10	20	Ω
Load Resistance	R_{RFO}	–	50	–	–	kΩ
Load Capacitance	C_{RFO}	–	–	–	100	PF
DC Offset Voltage	V_{OSR}	AIN = AG	-200	–	+200	mV
Output Signal Level	V_{RFO}	EQR1 = 1, EQR2 = V1 f_{IN} = 1800 Hz	V_{AIN} -2	V_{AIN}	V_{AIN} +2	dBm
Idle Channel Noise	N_{IDLR}	Using a 0.3 ~ 3.4 kHz flat weighted filter	–	-80	–	dBm
Total Harmonic Distortion	T_{HDR}	–	–	–	-50	dB

III

Parameter	Symbol		Condition	Min	Typ	Max	Unit
AGC Circuit Input (AGCI), Output (AGCO)							
Input Resistance	R_{AGCI}	AGCI	–	50	100	–	kΩ
Allowable Input DC Offset Voltage	V_{OSAGCI}		–	-0.5	–	+0.5	mV
Input Signal Level Range*	V_{AGCI}		–	-45.4	–	+5.6	dBm
Output Resitance	R_{OA}	AGCO	–	–	10	20	Ω
Load Resistance	R_{AGCO}		V_{AGCO} = -6 dBm	10	–	–	kΩ
Load Capacitance	C_{AGCO}		–	–	–	100	PF
DC Offset Voltage	V_{OSA}		–	-50	–	+50	mV
Output Signal Level*	V_{AGCO}		Controlled by Demodulator	–	-6	–	dBm

* When V_{AGCI} is within this range, the signal level output from AGC circuit should be about -6 dBm with digitally controlling by the demodulating DSP.

6. Attenuator, Amplitude Equalizers and Filters Characteristics

(V_{DD} = +5V ±5%, V_{SS} = -5V ±5%, T_a = 0 ~ 70°C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Attenuator						
Attenuation Accuracy (0 ~ 14 dB, 2 dB step)	A_{TT}	To the Designed Values	-1	0	+1	dB
Amplitude Equalizer (Transmit and Receive Paths)						
Frequency Characteristics (Relative gain to the gain at 1800 Hz) See Figure 4	EQ0 (Through)	EQT(R)1 = 1 EQT(R)2 = 1	f_{IN}	600 Hz	-1	0	+1	dB
				1200 Hz	-0.5	0	+0.5	
				2400 Hz	-0.5	0	+0.5	
				3000 Hz	-1	0	+1	
	EQ1 (I)	EQT(R)1 = 1 EQT(R)2 = 0		600 Hz	-2.1	-1.1	-0.1	
				1200 Hz	-1.2	-0.7	-0.2	
				2400 Hz	+0.2	+0.7	+1.2	
				3000 Hz	+0.4	+1.4	+2.4	
	EQ2 (II)	EQT(R)1 = 0 EQT(R)2 = 1		600 Hz	-4.8	-3.3	-1.8	
				1200 Hz	-2.8	-1.8	-0.8	
				2400 Hz	+0.4	+1.4	+2.4	
				3000 Hz	+1.2	+2.7	+4.2	
	EQ3 (III)	EQT(R)1 = 0 EQT(R)2 = 0		600 Hz	-6.8	-5.3	-3.8	
				1200 Hz	-3.7	-2.7	-1.7	
				2400 Hz	+1.0	+2.0	+3.0	
				3000 Hz	+2.3	+3.8	+5.3	
Gain Tolerance (Relative gain to the gain of EQ0 at 1800 Hz)	G_{EQ1}	EQT(R)1 = 1 EQT(R)2 = 0	f_{IN}	1800 Hz	-0.5	0	+0.5	dB
	G_{EQ2}	EQT(R)1 = 0 EQT(R)2 = 1			-0.5	0	+0.5	
	G_{EQ3}	EQT(R)1 = 0 EQT(R)2 = 0			-0.5	0	+0.5	

NOTE) This spec is applicable for only amplitude equalizers and does not include other filters' frequency characteristics.

III

Parameter	Symbol	Condition			Min	Typ	Max	Unit
BWC Transmit LPF								
2nd/3rd Harmonics Components Amplitude (Relative values to the fundamental component amplitude)	H_{BWC}	BTD = 0	$2 \cdot f_{OBM}$	780 Hz	—	-60	-55	dB
			$3 \cdot f_{OBM}$	1170 Hz	—	-60	-55	dB
		BTD = 1	$2 \cdot f_{OBS}$	900 Hz	—	-60	-55	dB
			3·fOBS	1350 Hz	—	-60	-55	dB
Transmit LPF								
Transmit LPF Voltage Gain	G_{TL}	EQT1, 2 = 1 ATT1, 2, 3 = 1 V_{XIN} = 0 dBm		390 Hz 450 Hz	-2	0	+2	dB
				1700 Hz 1800 Hz	-0.8	+1.2	+3.2	dB
Frequency — Amplitude Characteristics (Relative gain to G_{TL} at 390 Hz)	A_{TL}	EQT1, 2 = 1 ATT1, 2, 3 = 1 V_{XIN} = 0 dBm	f_{IN}	2400 Hz	+0.5	+1.5	+2.5	dB
				6000 Hz	—	-26	-23	dB
Group Delay Distortion	D_{TL}	EQT1, 2 = 1 300 Hz ≤ f_{IN} ≤ 4000 Hz			—	—	150	μs
Receive BPF								
Receive BPF Voltage Gain	G_{RB}	EQR1, 2 = 1 V_{AIN} = 0 dBm f_{IN} = 1700 Hz			-2	0	+2	dB
Frequency — Amplitude Characteristic (Relative gain to G_{RB})	A_{RB}	EQR1, 2 = 1 V_{AIN} = 0 dBm	f_{IN}	150 Hz	—	-17	-14	dB
				300 Hz	-4	-3	-1	dB
				3000 Hz	+3	+4	+6	dB
				6000 Hz	—	-19	-16	dB
Group Delay Distortion	D_{RB}	EQR1, 2 = 1 300 Hz ≤ f_{IN} ≤ 4000 Hz			—	—	1.3	ms

Parameter	Symbol	Condition			Min	Typ	Max	Unit
Receive HPF								
Receive HPF Voltage Gain *1	G_{RH}	EQR1, 2 = 1 V_{AIN} = 0 dBm f_{IN} = 620 Hz			−2	0	+2	dB
Frequency – Amplitude Characteristics (Relative gain to G_{RH}) *1	A_{RH}	EQR1, 2 = 1 V_{AIN} = 0 dBm	f_{IN}	390 Hz	—	−77	−65	dB
				450 Hz	—	−71	−65	dB
				500 Hz	—	−40	−36	dB
Group Delay Distortion *2	D_{RH}	EQR1, 2 = 1 800 Hz ≤ f_{IN} ≤ 4000 Hz			—	—	1	ms

*1: Includes Receive BPF's characteristics. *2: Only Receive HPF itself.

Receive LPF (for Call Progress Tone Detection)

Receive LPF Voltage Gain *1	G_{RL}	EQR1, 2 = 1 V_{AIN} = 0 dBm f_{IN} = 620 Hz			−2	0	+2	dB
Frequency – Amplitude Characteristics (Relative gain to G_{RL}) *1	A_{RL}	EQR1, 2 = 1 V_{AIN} = 0 dBm	f_{IN}	350 Hz	−3	−2	−1	dB
				910 Hz	—	−60	−54	dB

*1: Includes Receive BPF's characteristics.

III

NOTE) Each Spec. is measured according to the following table.

Circuits	Signal Input	Signal Output	BWC1	BWC2	ATT 1,2,3	EQT 1,2	EQR 1,2	Measured Block	Reference Figure
Attenuator	XIN	AOUT	—	—	000 ~ 111	1	—	ATT + T·LPF	5
Transmit Amplitude Equalizer	XIN	AOUT	—	—	1	00 ~ 11	—	AEQL + T·LPF	4, 5
BWC Transmit LPF	BOUT →XIN	AOUT	1	1	1	1	—	BWC·LPF + T·LPF	5, 6
Transmit LPF	XIN	AOUT	—	—	1	1	—	T·LPF	5
Receive Amplitude Equalizer	AIN	RFO	1	1	—	—	00 ~ 11	AEQL	4
Receive BPF	AIN	RFO	0	0	—	—	1	R·BPF	7
Receive HPF	AIN	RFO	0	1	—	—	1	R·HPF + R·BPF	7, 8
Receive LPF	AIN	RFO	1	0	—	—	1	R·LPF + R·BPF	6, 7

Table 1

7. DA, AD Converter and AGC Circuit

(V_{DD} = +5V ±5%, V_{SS} = -5V ±5%, T_a = 0 ~ 70°C)

Parameter		Symbol	Condition		Min	Typ	Max	Unit
Transmit Digital to Analog Converter								
Bits of Resolution		B_{REST}	–		–	8	–	bit
DA Conversion Reference Voltage		V_{REF}	–		–	+2.50	–	V
Full Scale*	Plus Full Scale	PFV_{DA}	V_{REF} = + 2.50 V	TD8 ~ TD1: 01111111	+2.16	+2.21	+2.27	V
	Minus Full Scale	NFV_{DA}		TD8 ~ TD1: 10000000	-2.29	-2.23	-2.18	V
Linearity*		N_{LDA}	–			0.36	0.5	%

* This specification is defined as the voltage at the A_{OUT} terminal, but does not include the DC offset voltage at the terminal.

Receive Analog to Digital Converter

Bits of Resolution	B_{RESR}	–	–	8	–	bit
AD Conversion Reference Voltage	V_{REF}	–	–	+2.50	–	V
Full Scale* Plus Full Scale	PFV_{AD}	V_{REF} = + 2.50 V Equivalent values to the input voltage of AD converter	+2.42	+2.48	+2.54	V
Full Scale* Minus Full Scale	NFV_{AD}		-2.56	-2.50	-2.44	V
Linearity*	NL_{AD}	–	–	0.24	0.5	%
Output DC Offset*	V_{OSAD}	–	-1/2	–	+1/2	LSB

* This specification does not include the DC offset voltage at the input of the AD converter (AGCO).

AGC Circuit

Gain Control Bits of Resolution	B_{RESA}	–	–	8	–	bit
Dynamic Range	DY_{AGC}	–	–	51	–	dB
Gain Setting Minimum Step	G_{STP}	–	–	0.2	–	dB
Gain Setting Accuracy	G_E	–	-0.2	0	+0.2	dB
Total Harmonic Distortion	THD_{AGC}	–	–	–	-50	dB
Signal to Noise Ratio	SN_{AGC}	Set Gain = Maximum Signal/Noise at AGCO	50	–	–	dB

8. Timing Characteristics

(V_{DD} = +5V ±5%, V_{SS} = -5V ±5%, T_a = 0 ~ 70°C)

Parameter		Symbol	Condition			Min	Typ	Max	Unit
Carrier Detect and Level Comparator for AGC Circuit									
CD1 See Figure 9-1	OFF → ON	T_{CDON1}	CD1H = V_{SS}	CD1L = 0 BWC1 = 0	V_{AIN} = 0 dBm	–	2.5	–	ms
	ON → OFF	T_{CDOFF1}			f_{IN} = 1700 Hz	–	9.6	–	ms
	OFF → ON	T_{CDON2}			V_{AIN} = -36 dBm	–	3.5	–	ms
	ON → OFF	T_{CDOFF2}			f_{IN} = 1700 Hz	–	6.0	–	ms
	OFF → ON	T_{CDON3}		CD1L = 1 BWC1 = 0	V_{AIN} = 0 dBm	–	1.8	–	ms
	ON → OFF	T_{CDOFF3}			f_{IN} = 1800 Hz	–	9.0	–	ms
	OFF → ON	T_{CDON4}			V_{AIN} = -39 dBm	–	3.1	–	ms
	ON → OFF	T_{CDOFF4}			f_{IN} = 1800 Hz	–	4.6	–	ms
	OFF → ON	T_{CDON5}		CD1L = 0 BWC1 = 1 BWC2 = 0	V_{AIN} = 0 dBm	0	1.8	90	ms
	ON → OFF	T_{CDOFF5}			f_{IN} = 400 Hz	0	1.8	90	ms
	OFF → ON	T_{CDON6}			V_{AIN} = -40 dBm	0	5.0	90	ms
	ON → OFF	T_{CDOFF6}			f_{IN} = 400 Hz	0	4.6	90	ms
CD2 See Figure 9-1	OFF → ON	T_{CDON7}	CD2H = V_{SS}		V_{AIN} = 0 dBm	–	1.2	–	ms
	ON → OFF	T_{CDOFF7}			f_{IN} = 1650 Hz	–	10	–	ms
	OFF → ON	T_{CDON8}			V_{AIN} = -40 dBm	–	5.6	–	ms
	ON → OFF	T_{CDOFF8}			f_{IN} = 1650 Hz	–	2.2	–	ms
LD1 See Figure 9-2	OFF → ON	T_{LD1ON}				–	2.5	–	ms
	ON → OFF	T_{LD10FF}				–	1.5	–	ms
LD2 See Figure 9-2	OFF → ON	T_{LD20N}				–	5.4	–	ms
	ON → OFF	T_{LD20FF}				–	0.6	–	ms

Power Down Control Timing

Power ON Time	T_{PWON}	PWDN: 1 → 0 See Figure 10	–	–	200	ms
Power Down Time	T_{PWOFF}	PWDN: 0 → 1 See Figure 10	–	–	10	ms

III

9. Transmission Performance

(V_{DD} = +5V ±5%, V_{SS} = -5V ±5%, T_a = 0 ~ 70°C)

Parameter	Symbol	Condition		Min	Typ	Max	Unit
Transmitter							
Out-of-Band Energy Referred to Carrier Level	E_{OT}	EQT1, 2 = 1 V_{AOUT} = 0 dBm See Figure 11	4 ~ 8 kHz	—	—	-20	dB
			8 ~ 12 kHz	—	—	-40	dB
			12 kHz ~	—	—	-60	dB

Receiver

Dynamic Range	DY_R	As a single tone				-48	—	0	dBm/600Ω
Carrier Detect Threshold*3	TH_{CDON1}	CD1H = V_{SS}	CD1L = 0 BWC1 = 0	CD1	ON	—	-39.2	—	dBm
	TH_{CDOFF1}				OFF	—	-49.3	—	dBm
	TH_{CDON2}		CD1L = 1 BWC1 = 0	CD1	ON	—	-41.8	—	dBm
	TH_{CDOFF2}				OFF	—	-46.8	—	dBm
	$TH_{CDON/OFF3}$		BWC1 = 1 BWC2 = 0	CD1	ON/OFF	—	-45*1	—	dBm
	TH_{CDON4}	CD2H = V_{SS}		CD2	ON	—	-45	—	dBm
	TH_{CDOFF4}				OFF	—	-50	—	dBm
*2 Optional Carrier Detect Threshold by External Potentials	TH_{CDON5}	CD1L: 0 ~ V_{DD}		CD1	ON	Adjustable			dBm
	TH_{CDOFF5}	CD1H: 0 ~ V_{DD}			OFF	Adjustable			dBm
	TH_{CDON6}	CD2L: 0 ~ V_{DD}		CD2	ON	Adjustable			dBm
	TH_{CDOFF6}	CD2H: 0 ~ V_{DD}			OFF	Adjustable			dBm

*1 This operating mode is used during the call progress tone monitoring and does not provide the hysteresis of the detect ON and OFF level.

*2 In this mode, CD1's ON/OFF and CD2's ON/OFF levels are determined by external adjustments. It is impossible to use the optional threshold either for CD1 or CD2.

*3 Threshold levels are defined by a single tone input on the AIN terminal. In actual applications, however, input analog signal is not a single tone but a modulated signal by FSK, PSK or QAM. Therefore, the hysteresis values (CD/OFF-CD/ON) become less than the differences of CD/ON and CD/OFF levels shown in the specification table.

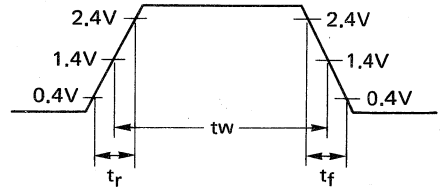


Figure 1 Definition of Rise/Fall Time

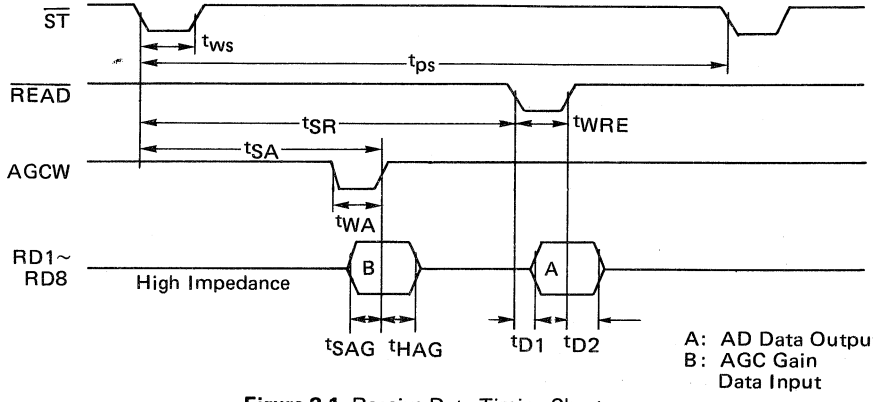


Figure 2-1 Receive Data Timing Chart

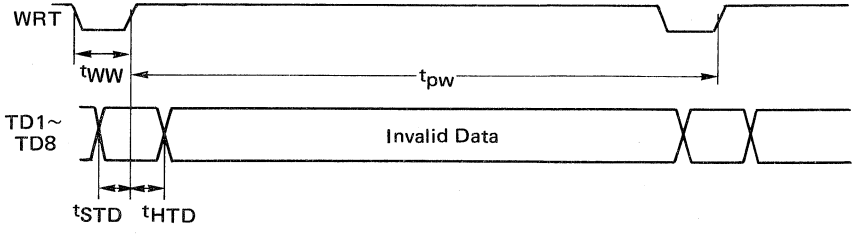


Figure 2-2 Transmit Data Timing Chart

NOTE) Figure 2-1 and Figure 2-2 show the timing when transmit data is input to the chip via TD1 through TD8.

III

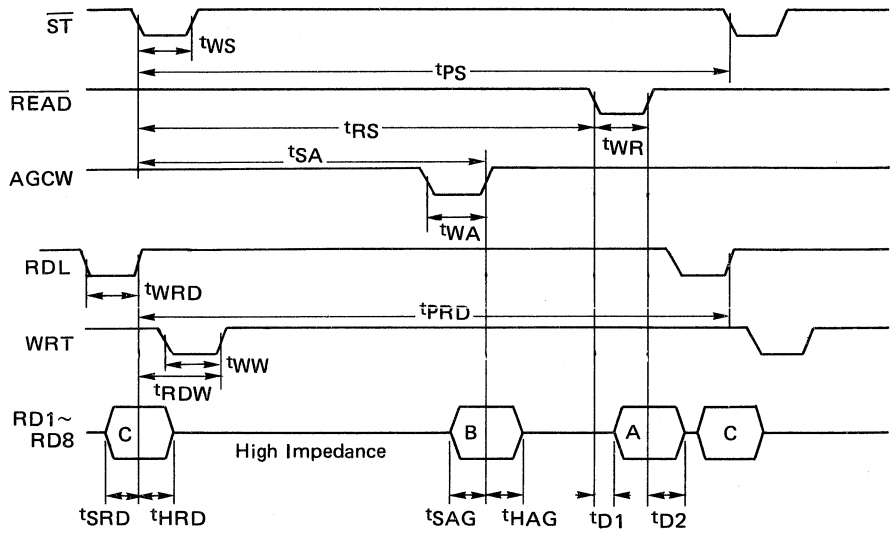


Figure 3 Transmit and Receive Data Timing Chart

NOTE) Figure 3 shows the timing when transmit, receive and AGC data are interfaced via RD1 through RD8 as a common data bus.

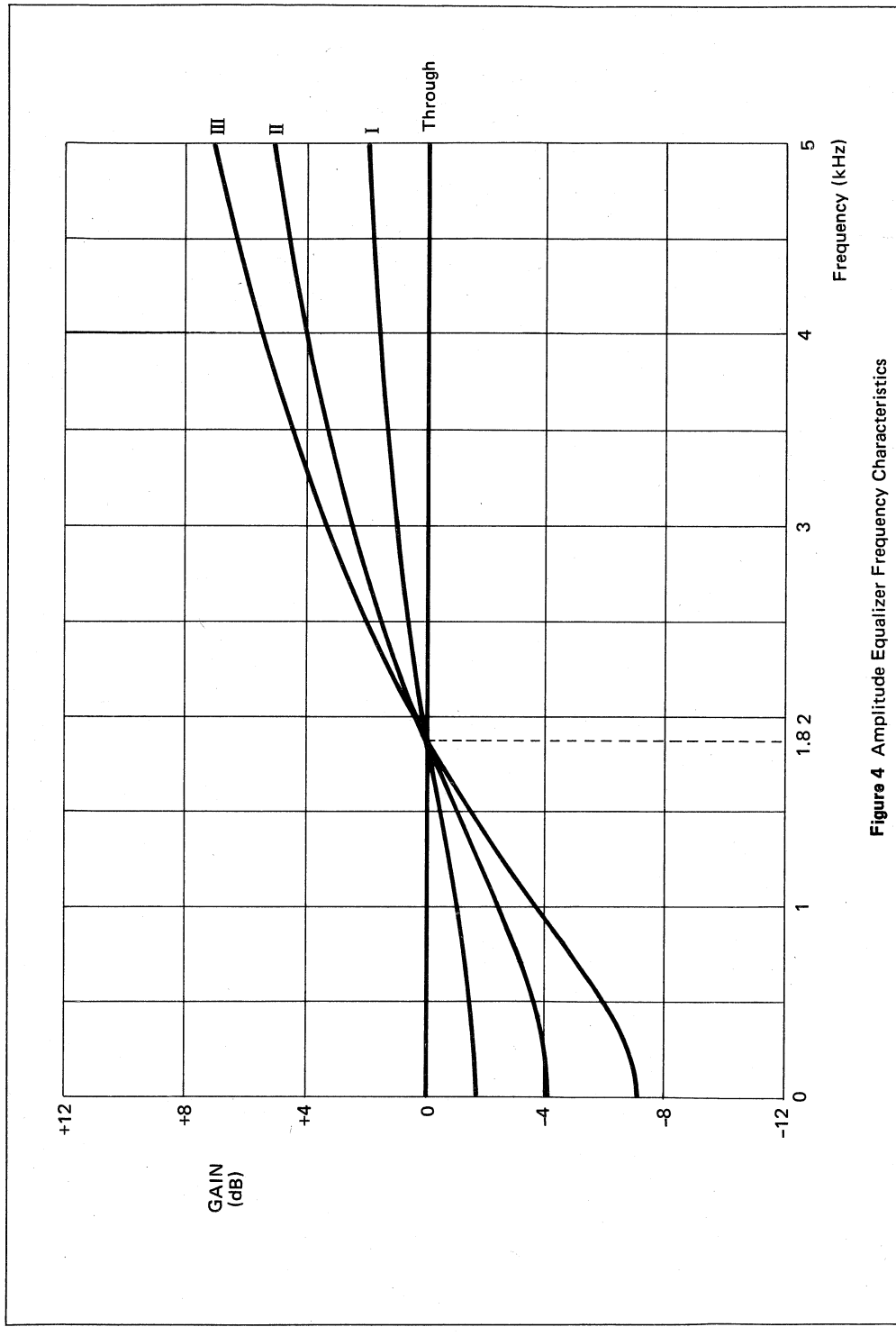


Figure 4 Amplitude Equalizer Frequency Characteristics

III

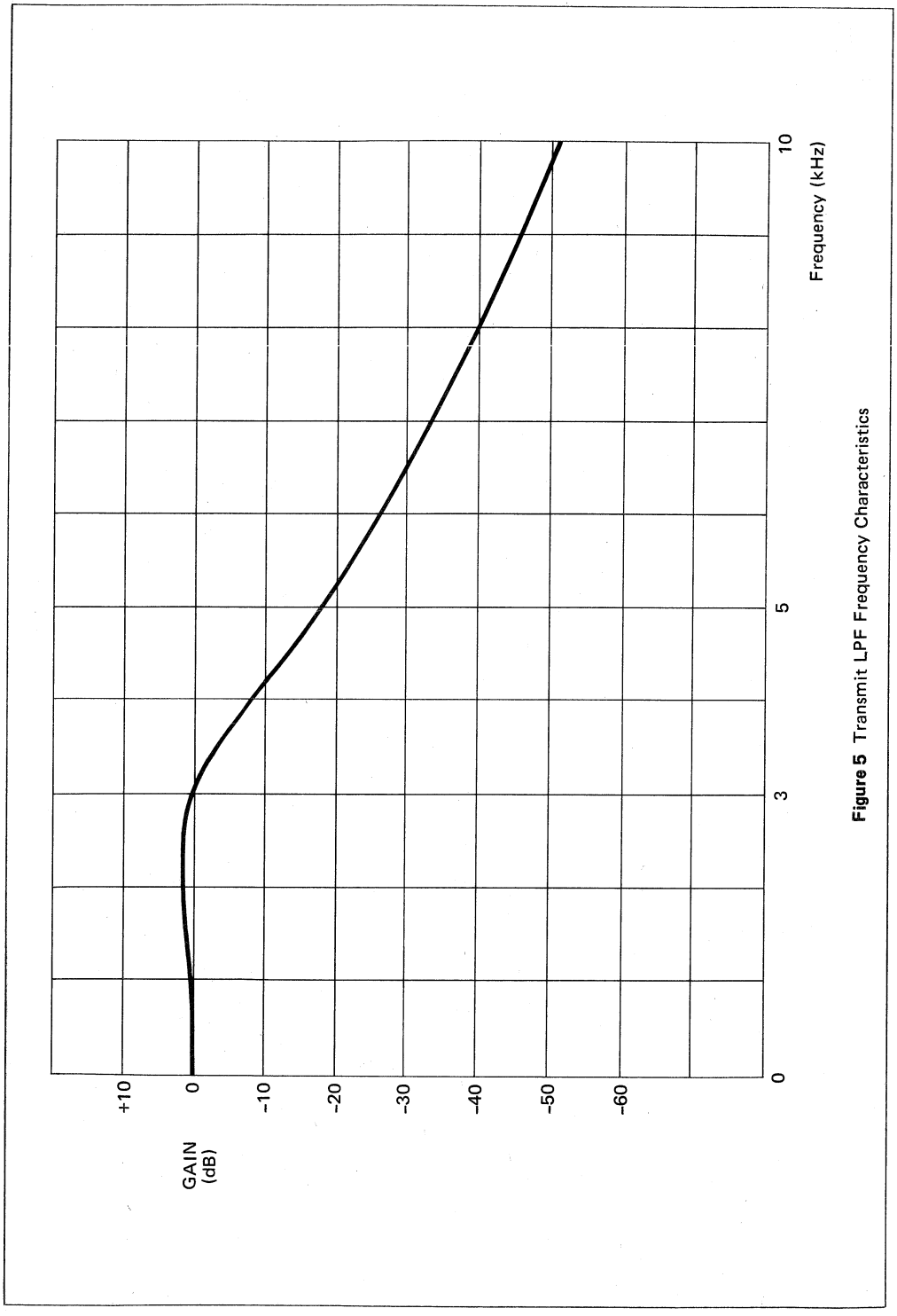


Figure 5 Transmit LPF Frequency Characteristics

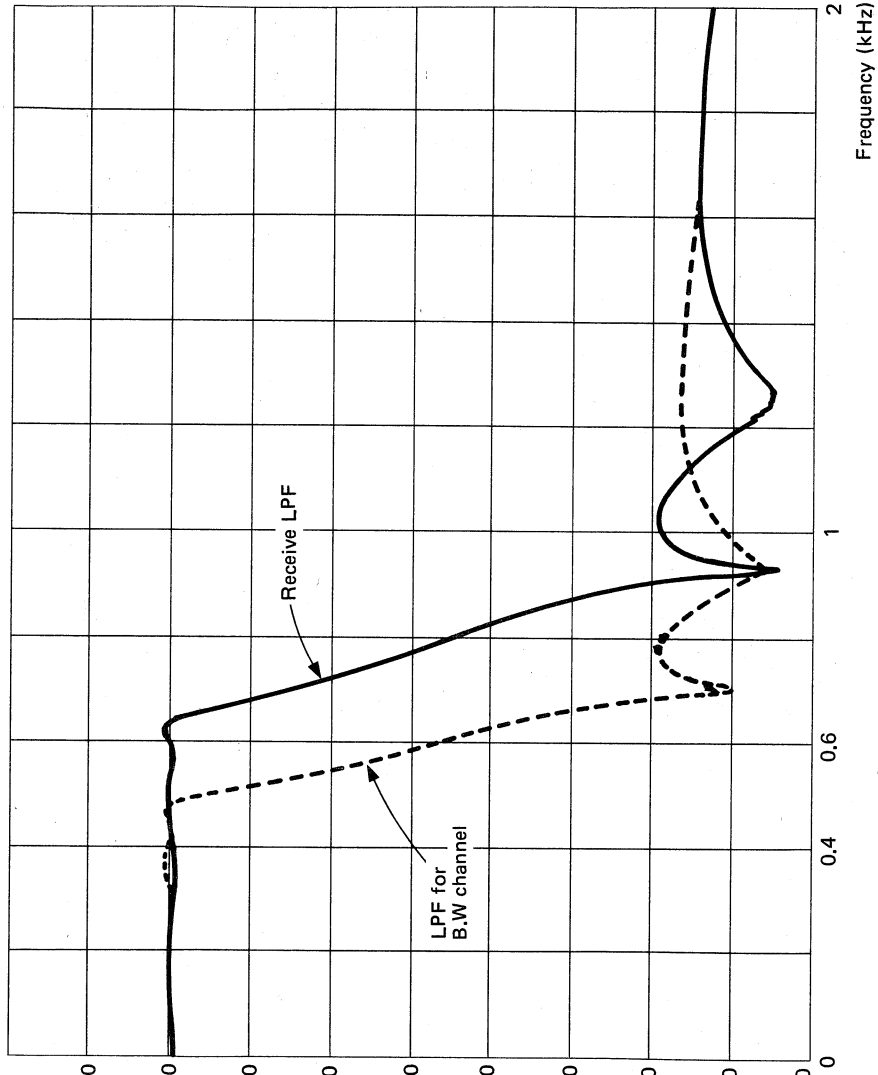


Figure 6 LPF for Backward Channel/Receive LPF Frequency Characteristics

NOTE) The LPF is used for both transmit and receive path changed its bandwidth.

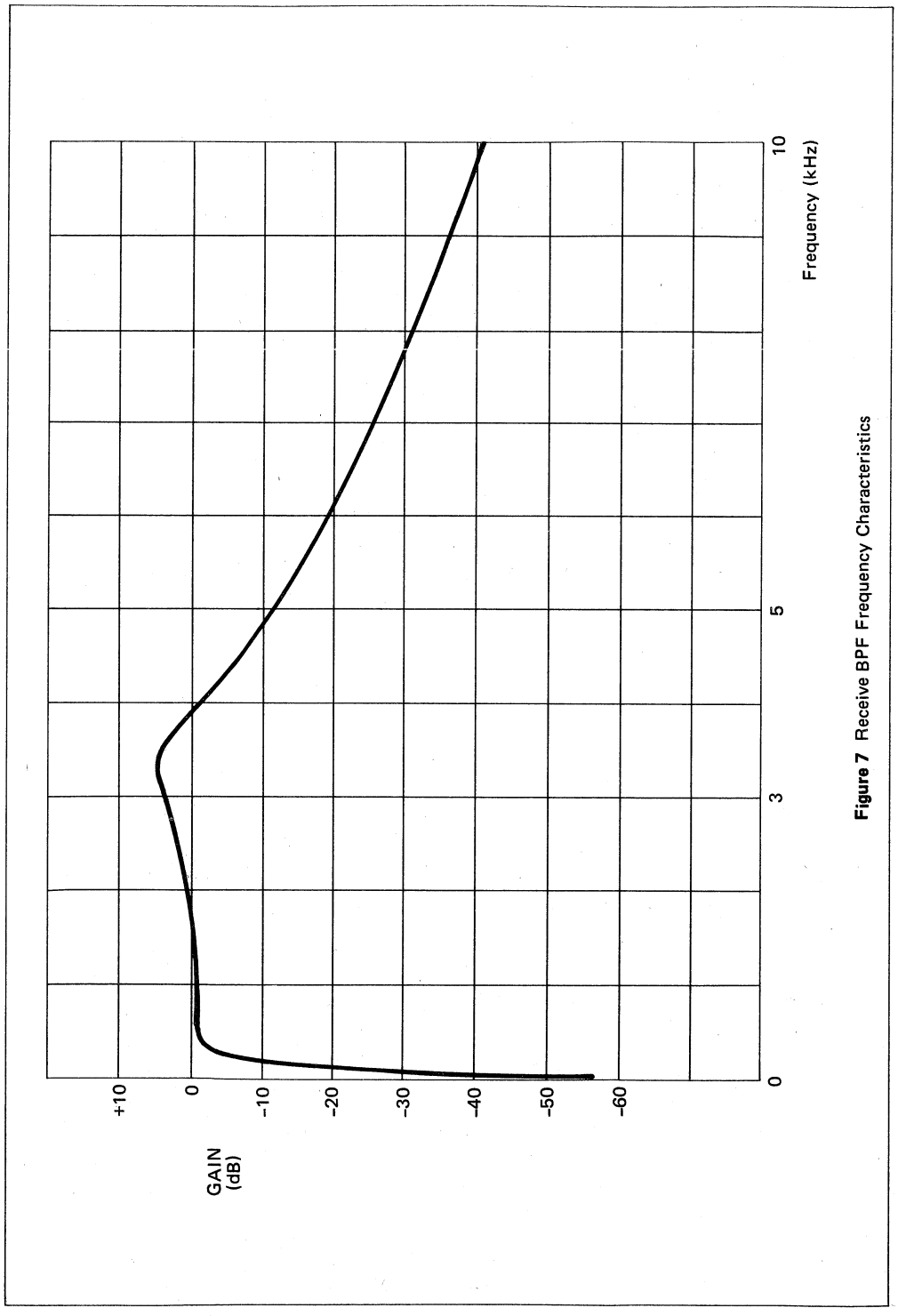


Figure 7 Receive BPF Frequency Characteristics

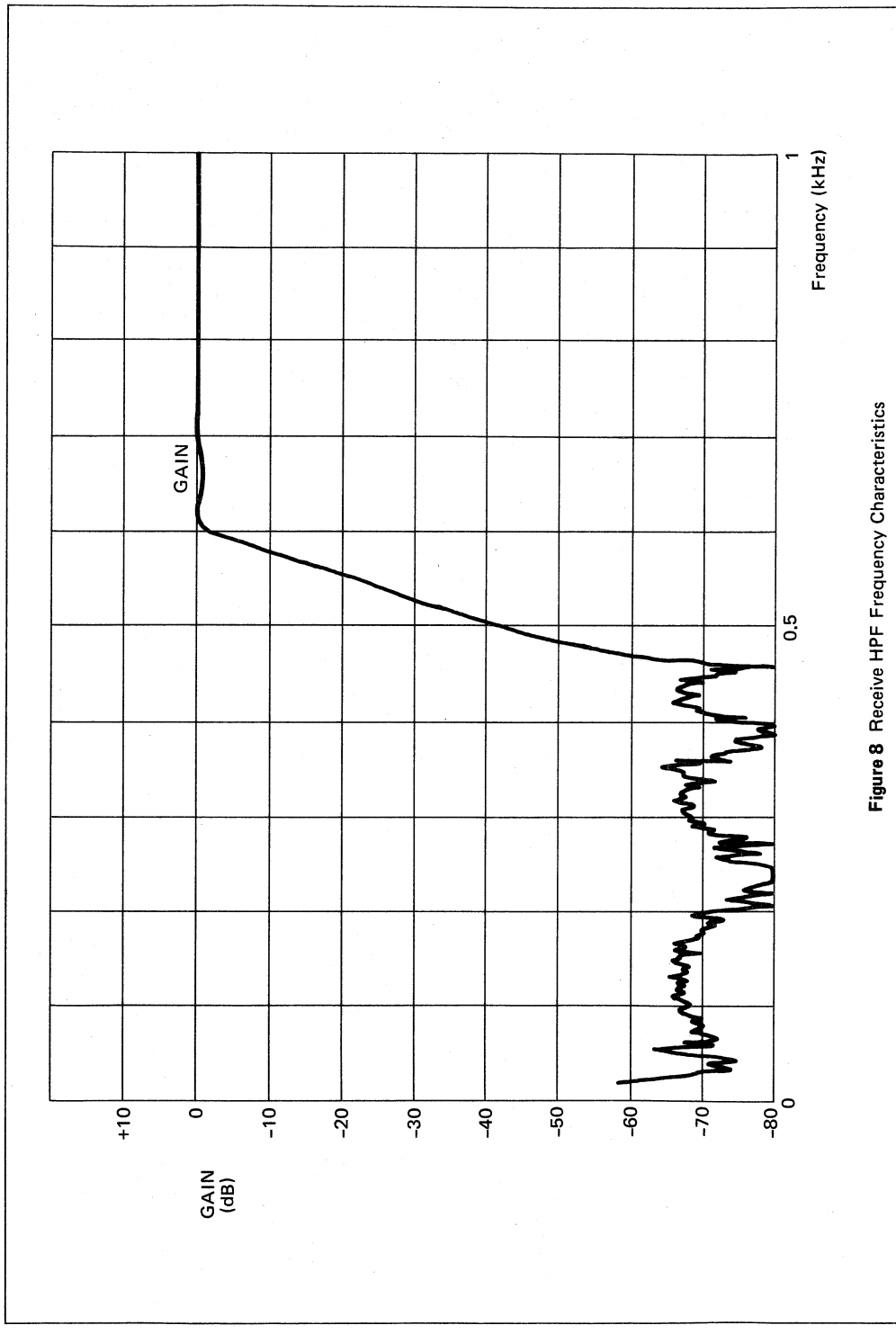


Figure 8 Receive HPF Frequency Characteristics

III

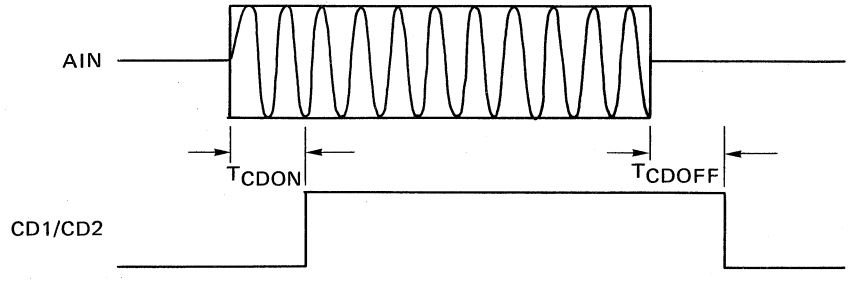


Figure 9-1

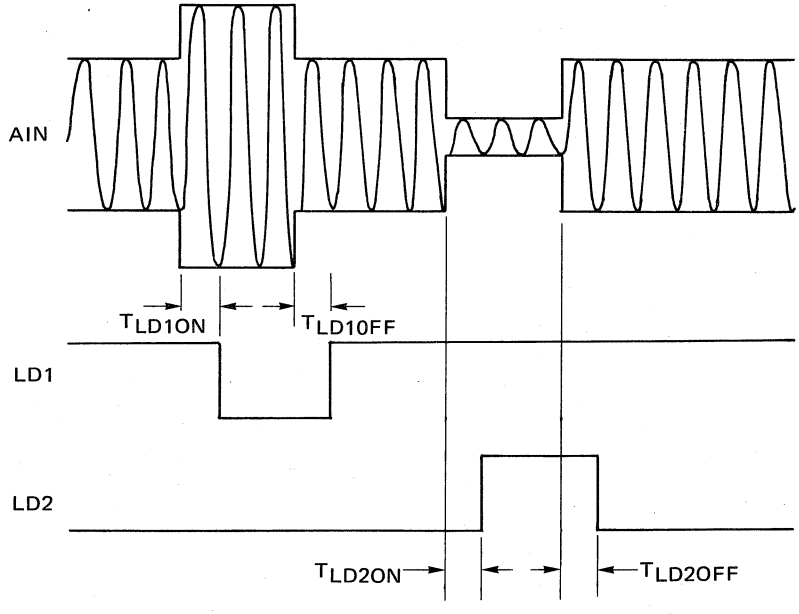


Figure 9-2

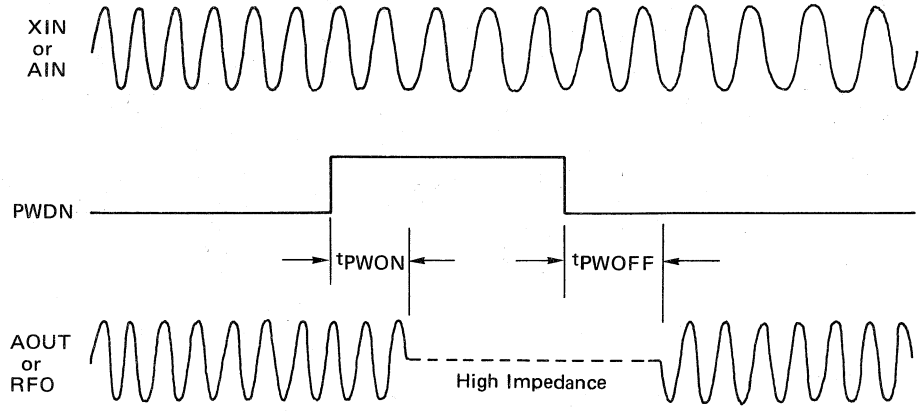


Figure 10 Power Down Mode Response

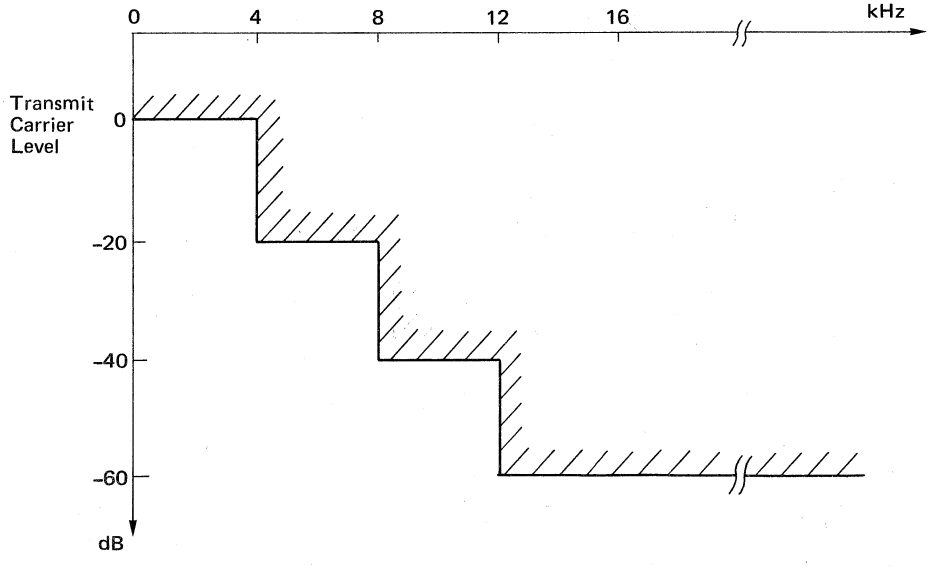


Figure 11 Maximum Level of Out-of-Band Energy Relative to the Transmit Carrier Level

III

PIN DESCRIPTION

Pin Name	Pin No. SS	Pin No. JS	Function
$\overline{BRS}$	1		The chip contains 75 bps FSK modulator (420 ± 30 Hz) that is useful for some kinds of applications, such as videotex systems. $\overline{BRS}$ controls the modulator to send FSK signal over telephone line through AOUT.
BTD	2		BTD is the transmit data that should be converted to the modulated FSK signal to be sent over telephone line.
TRSW	3		On-chip DA converter can operate according to not only TD, but also RD for its input data. This function is significant in the special application where both RD and TD are given to and taken from the same data bus line. At this case, it is required to put TRSW on digital 1 state for connecting the input of DA to RD terminals internally in place of TD terminals.
RDL	4		A clock pulse should be input to RDL to latch RD on it's positive edge. Refer to Figure 12.

$\overline{BRS}$	FSK signal transmit
Digital 0	Enable
Digital 1	Disable

Table 2

BTD	FSK signal frequency
Digital 0	"Space" 450 Hz
Digital 1	"Mark" 390 Hz

Table 3

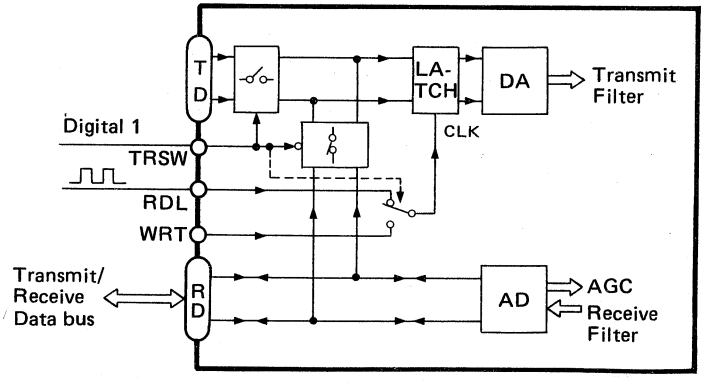


Figure 12

Pin Name	Pin No. SS	Pin No. JS	Function
WRT	5		This signal controls to write the data on TD1 ~ TD8 into the DA converter. These data are latched on the positive edge of WRT.
TD1 ⌇ TD8	13 ⌇ 6		Transmit signal digital data input for DA conversion. These pins are 8-bit parallel two's complement data input pins, and the data are loaded into the DA converter on the positive edge of WRT. TD1 is the LSB and TD8 is the MSB. Refer to Table 4.
MCK	14		A 3.456 MHz clock signal should be applied to this pin. This is the time base for the operation of MSM6949 and is divided down within the chip for variety of internal uses.
V_{DD2}	15		Positive power supply, +5V. This pin is internally connected only to the digital output logic circuitry for RD1 ~ RD8, RDA and RDB.
RD1 ⌇ RD8	24 ⌇ 17		These are I/O terminals. When $\overline{READ}$ is held on digital 0 state, these pins become output terminals and the result of the AD conversion with 8-bit (or 10-bit) parallel two's complement format appears. Refer to Table 4. When $\overline{READ}$ is held on digital 1 state, these pins become input terminals and the data input to these pins are loaded into the register storing them as the gain setting data for AGC circuit on the positive edge of AGCW.

TD/RD	8	7	6	5	4	3	2	1
Plus Full Scale	0	1	1	1	1	1	1	1
⋮								
Plus 0	0	0	0	0	0	0	0	0
Minus 0	1	1	1	1	1	1	1	1
⋮								
Minus Full Scale	1	0	0	0	0	0	0	0

Table 4 8-digit Data Table for TD and RD

<table>
<tr><th rowspan="2">Pin Name</th><th colspan="2">Pin No.</th><th rowspan="2">Function</th></tr>
<tr><th>SS</th><th>JS</th></tr>
<tr><td></td><td></td><td></td><td>
To input digital 1 to each digit of RD1 ~ RD8 means the following amplitude per digit for AGC circuit.
<table>
<tr><th>Pin</th><th>Gain</th><th>Pin</th><th>Gain</th></tr>
<tr><td>RD1</td><td>+0.2 dB</td><td>RD5</td><td>+3.2 dB</td></tr>
<tr><td>2</td><td>+0.4</td><td>6</td><td>+6.4</td></tr>
<tr><td>3</td><td>+0.8</td><td>7</td><td>+12.8</td></tr>
<tr><td>4</td><td>+1.6</td><td>8</td><td>+25.6</td></tr>
</table>
Table 5
The actual values of AGC circuit's relative and obsolute gain are as shown in Table 6.
<table>
<tr><th colspan="8">RD</th><th colspan="2">Gain (dB)</th></tr>
<tr><th>8</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>Relative</th><th>Absolute</th></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>-25.5</td><td>-11.6</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>-25.3</td><td>-11.4</td></tr>
<tr><td colspan="8">⋮</td><td>⋮</td><td>⋮</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>-0.1</td><td>+13.8</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>+0.1</td><td>+14.0</td></tr>
<tr><td colspan="8">⋮</td><td>⋮</td><td>⋮</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>+25.3</td><td>+39.2</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>+25.5</td><td>+39.4</td></tr>
</table>
Table 6
</td></tr>
<tr><td>RDB</td><td>25</td><td></td><td rowspan="2">These are 3-state output pins to extend the RD bit length when CSW is set at digital 1 state. When CSW is set at digital 1 state, each digit of RD8 ~ RD1 is shifted toward less significant bit by 2 bits and this makes RDA become LSB and MSB appears on RD6, RD7 and RD8 with the same data. This processing is useful to attenuate the received signal level for the demodulator.</td></tr>
<tr><td>RDA</td><td>26</td><td></td></tr>
<tr><td>$\overline{ST}$</td><td>27</td><td></td><td>This signal allows the MSM6949 to start the AD conversion on the negative edge of $\overline{ST}$. The conversion period should be within 51 ~ 143 μs. The latest AD converted data appear on the RD pins 44 μs after from the falling edge of $\overline{ST}$.</td></tr>
</table>

Pin Name	Pin No. SS	Pin No. JS	Function
$\overline{\text{READ}}$	28		This is a control signal for 3-state output data bus line RD8 ~ RD1, RDA and RDB. While this pin is in digital 0 state, the output bus is active and the result of the AD conversion appears on RD8 ~ RD1, While this pin is in digital 1 state, the output bus is inactive and RD8 ~ RD1, RDA and RDB become input terminals.
AGCW	29		This signal controls to load the gain setting data into the register for AGC circuit through RD8 ~ RD1 on the positive edge of AGCW. At this time, $\overline{\text{READ}}$ must be in digital 1 state.
CSW	30		As mentioned in the description of RDA and RDB, the RD bit length is extended from 8-bits to 10-bits and the position of each digit is shifted by 2-bits toward the less significant digit when CSW is set at digital 1 state.
LD1	31		These output signals are of comparators which have different threshold levels each other and the inputs are connected to the output of AGC circuitry (AGCO).
LD2	32		When AGCO shows an extraordinary signal level by the abrupt change in the received signal level, LD1 and LD2 can be a warning signal for the demodulator and the AGC circuit.

	Signal level on AGCO (dBm)				
	+2	+1		-14.5	-15.5
LD1	0		1		
LD2		0			1

Table 7

For example, the demodulator should be reset when LD1 indicates the digital 0 state.

In other case when LD2 indicates the digital 1 state, the AGC circuit should be set at the nominal gain by setting digital 0 to all of RD digits for the quick escape from the abnormal state. Refer to Table 7 and Figure 13.

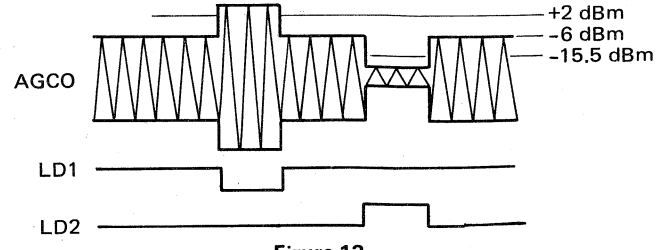


Figure 13

Pin Name	Pin No. SS	Pin No. JS	Function
CD1	33		The MSM6949 provides a pair of carrier detect circuitry and each of them has a inherent detect level which is internally fixed.
CD2	34		On the other hand, their carrier detect levels can be determined by external circuit by using CD1L, CD1H, CD2L and CD2H. Usually, CD1 is used for 2400, 4800, 7200 and 9600 bps data transmission, or for call progress tone monitoring. CD2 is used for FSK transmission, such as CCITT T. 30. The state of digital 1 means that the received signal is within the level range to be demodulated. When indicating the digital 0 state, the received data should be ignored as meaningless information. Refer to the descriptions for CD1L, CD1H, CD2L and CD2H.
BWC1	35		These control signals determine the receive filter bandwidth according to the application's requirement. Refer to Figure 6, 7 and 8.
BWC2	36		

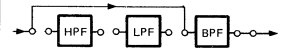
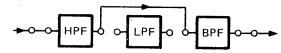
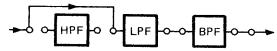
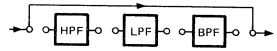
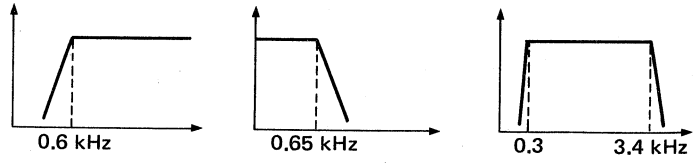
BWC1	BWC2	Receive Filter Composition	Band-width	Application
0	0		0.3 ~ 3.4 kHz	No backward channel transmitting
0	1		0.6 ~ 3.4 kHz	Backward channel transmitting
1	0		0.3 ~ 0.65 kHz	Call progress tone monitoring
1	1		Through	Special case (External Filter)

Table 8



<table>
<tr><th rowspan="2">Pin Name</th><th colspan="2">Pin No.</th><th rowspan="2">Function</th></tr>
<tr><th>SS</th><th>JS</th></tr>
<tr><td></td><td></td><td></td><td>When a modem operates without backward channel (BWC) transmiting, receive signal bandwidth should be extended to 0.3 kHz for better transmission data quality. When a modem operates with BWC transmitting, the receive filter must reject the BWC signal which leaks from own BWC transmitter through the hybrid circuit in the 2-wire facilities.

As backward channel transmitting signal's components exsist below 0.6 kHz, the received data quality would be deteriorated if HPF to eliminate them is not used.

Usually, the frequencies of call progress tones are included in the range from 0.3 kHz to 0.65 kHz. The MSM6949 have the filter for detecting those tones.</td></tr>
<tr><td>EQR1</td><td>37</td><td></td><td rowspan="2">For better transmission data quality, amplitude equalizers are provided about MSM6949 in both transmitter and receiver.

<table><tr><th>EQR1 / EQT1</th><th>EQR2 / EQT2</th><th>Equalizing Characteristics</th></tr><tr><td>0</td><td>0</td><td>III</td></tr><tr><td>0</td><td>1</td><td>II</td></tr><tr><td>1</td><td>0</td><td>I</td></tr><tr><td>1</td><td>1</td><td>Through</td></tr></table>
Table 9

Refer to Figure 4.</td></tr>
<tr><td>EQR2</td><td>38</td><td></td></tr>
<tr><td>DG</td><td>39</td><td></td><td>Digital ground, 0V.</td></tr>
<tr><td>AG</td><td>40</td><td></td><td>Analog ground, 0V.

When digital and analog circuitry are implemented in the same chip, analog functional performances are easy to be deteriorated by the digital noise. Especially, when the digital noise is asynchronous to the operating timing for analog circuitry, such as switched capacitor filter, AD and DA converter, the chip's performances become serious. The delicate chip is designed carefully so that the influence becomes less, but it is important not to mix the noise to AG as possible and design of PCB should be taken care of.</td></tr>
<tr><td>V_{SS}</td><td>41</td><td></td><td>Negative power supply, -5V.</td></tr>
</table>

III

Pin Name	Pin No. SS	Pin No. JS	Function
AGCC	42		An external capacitor of 1 μF should be connected between AGCC and AG. This capacitor is necessary to compensate the DC offset voltage generated in the AGC circuit.
AGCO	43		The output of the AGC circuit. This pin is used for the chip test, etc. The gain setting data should be loaded into the chip through RD8 ~ RD1 so that the signal level at AGCO becomes -6 dBm.
AGCI	44		AGCI is the input of the AGC circuit and RFO is the receive filter's output. These pins should be mutually connected via an external capacitor of 0.1 μF. This capacitor is required as an AC-coupling not to transfer the DC offset voltage to the AGC circuit. The input impedance of AGCI is typically 100 kΩ.
RFO	45		
CD1L	46		As described in the description of CD1 and CD2, a pair of carrier detect circuits can be used with the internally fixed inherent detect levels. On the other hand, detect levels can be externally adjusted for various kinds of applications. Internal fixed values and external adjustments are as follows.
CD1H	47		
CD2L	48		
CD2H	49		

CD1L	CD1H	CD2L	CD2H	BWC1	BWC2	CD1 ON	CD1 OFF	CD2 ON	CD2 OFF	Operating MODE
0	VSS	*	*	0	*	-39.2	-49.3	–	–	7200/9600 bps
1	VSS	*	*	0	*	-41.8	-46.8	–	–	2400/4800 bps
*	VSS	*	*	1	0	-45	–	–	–	Call Progress Tone
*	*	*	VSS	*	*	–	–	-45	-50	300 bps (T. 30)
>0V	>0V	*	*	0	*	Depend on V_{CD1L}, V_{CD1H}		–	–	External Adjustment
>0V	>0V	*	*	1	0	Depend on V_{CD1L}, V_{CD1H}		–	–	
*	*	>0V	>0V	*	*	–	–	Depend on V_{CD2L}, V_{CD2H}		

NOTE 1) Unit of CD1/2 detect level: dBm (0 dBm = 0.775 Vrms)
2) These levels are defined with a single tone.

Table 10

<table>
<tr><th rowspan="2">Pin Name</th><th colspan="2">Pin No.</th><th rowspan="2">Function</th></tr>
<tr><th>SS</th><th>JS</th></tr>
<tr><td></td><td></td><td></td><td>If an external adjustment is required, each of these terminals should be connected to the appropriate potential, which is over 0V, and this determines the carrier detect ON/OFF level. Four different kind of potentials determine the level as follows.

<table><tr><th>Terminal</th><th>Carrier Detect</th></tr><tr><td>CD1L</td><td>CD1 OFF</td></tr><tr><td>CD1H</td><td>CD1 ON</td></tr><tr><td>CD2L</td><td>CD2 OFF</td></tr><tr><td>CD2H</td><td>CD2 ON</td></tr></table>
As an aim for external adjustment, it can be forecast that the carrier detect threshold level becomes about -40 dBm when the input potential is plus 2.5 V. The relation between the potential and the level is linear.

Table 11</td></tr>
<tr><td>VR1</td><td>50</td><td></td><td rowspan="2">The MSM6949 provides the voltage reference which is used for AD and DA conversions, carrier detect, backward channel transmitter, etc.

The potential is stabilized to variations of temperature or supply voltages, but tends to be different from chip to chip. Therefore, an external adjustment is necessary.

The resistors used to adjust the reference voltage are connected to these pins as follows.

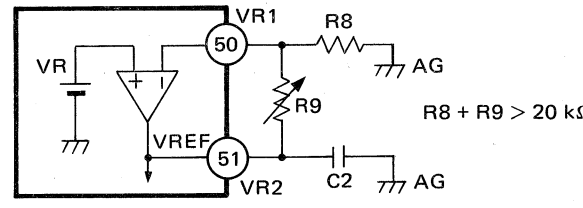
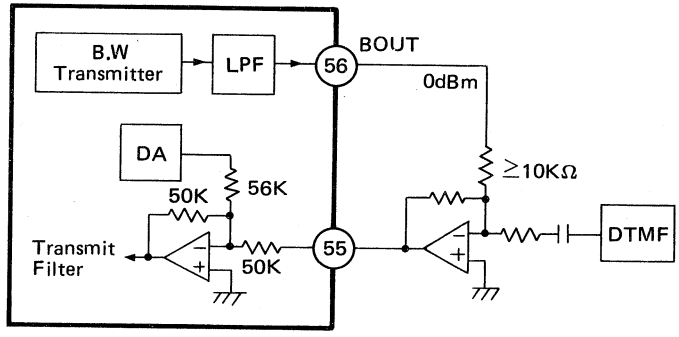
 

Figure 14

A bypass capacitor is required to keep this reference potential in the silent condition and the value of 1 μF is recommended. The reference voltage on VR2 (VREF) is approximately determined by the following equation and the typical value is +2.5V.

$$V_{REF} \simeq 1.2 \times \frac{R8 + R9}{R8} [V]$$</td></tr>
<tr><td>VR2</td><td>51</td><td></td></tr>
<tr><td>AIN</td><td>52</td><td></td><td>This pin is the receive analog signal input. The maximum input level is about 0 dBm (1.1 $V_{o\text{-}p}$).</td></tr>
</table>

Pin Name	Pin No.		Function
	SS	JS	
AOUT	54		This is the transmit analog signal output pin. The output resistance is about 10Ω and the load resistance should be more than 10 kΩ. The output signal level is set at typically +3 dBm or -1 dBm for PSK or QAM mode, respectively.
XIN	55		This is an external analog signal input. Usually, XIN is used as the input for the backward channel transmitter, and frequently for an external DTMF tone. This signal is routed to the transmit filter's input via an adder same as the signal from the DA converter.  **Figure 15** An external operational amplifier can be omitted when the DTMF tone is not input to XIN, and BOUT is connected to XIN directly.
BOUT	56		This is an output terminal of the backward channel transmitter. Refer to the description for XIN. The signal level is about 0 dBm. While call progress tone monitoring is proceeding, BOUT is internally connected to AG, because LPF is used in the receiver side.
PWDN	57		When digital 1 is input to PWDN, whole functions in the MSM6949 are disabled and the MSM6949 goes into the power standby mode. At this time, AOUT and RFO become high impedance state.
LT	58		LT is used to provide the signal path for the local analog loop (AC) test function. When digital 1 is input to LT, the transmit analog signal is routed to the input of the receive filter and AOUT is connected to AG internally.

<table>
<tr><th rowspan="2">Pin Name</th><th colspan="2">Pin No.</th><th rowspan="2">Function</th></tr>
<tr><th>SS</th><th>JS</th></tr>
<tr><td>EQT1</td><td>59</td><td></td><td rowspan="2">Refer to the description of EQR1 and EQR2.</td></tr>
<tr><td>EQT2</td><td>60</td><td></td></tr>
<tr><td>ATT1
⌇
ATT3</td><td>61
⌇
63</td><td></td><td>The MSM6949 provides attenuator for transmit signal.
<table><tr><th>ATT1</th><th>ATT2</th><th>ATT3</th><th>Signal Level Loss (dB)</th></tr><tr><td>0</td><td>0</td><td>0</td><td>14</td></tr><tr><td>0</td><td>0</td><td>1</td><td>12</td></tr><tr><td>0</td><td>1</td><td>0</td><td>10</td></tr><tr><td>0</td><td>1</td><td>1</td><td>8</td></tr><tr><td>1</td><td>0</td><td>0</td><td>6</td></tr><tr><td>1</td><td>0</td><td>1</td><td>4</td></tr><tr><td>1</td><td>1</td><td>0</td><td>2</td></tr><tr><td>1</td><td>1</td><td>1</td><td>0</td></tr></table>Table 12</td></tr>
<tr><td>V_{DD1}</td><td>64</td><td></td><td>Positive power supply, +5V.</td></tr>
</table>

CIRCUIT WIRING ILLUSTRATION

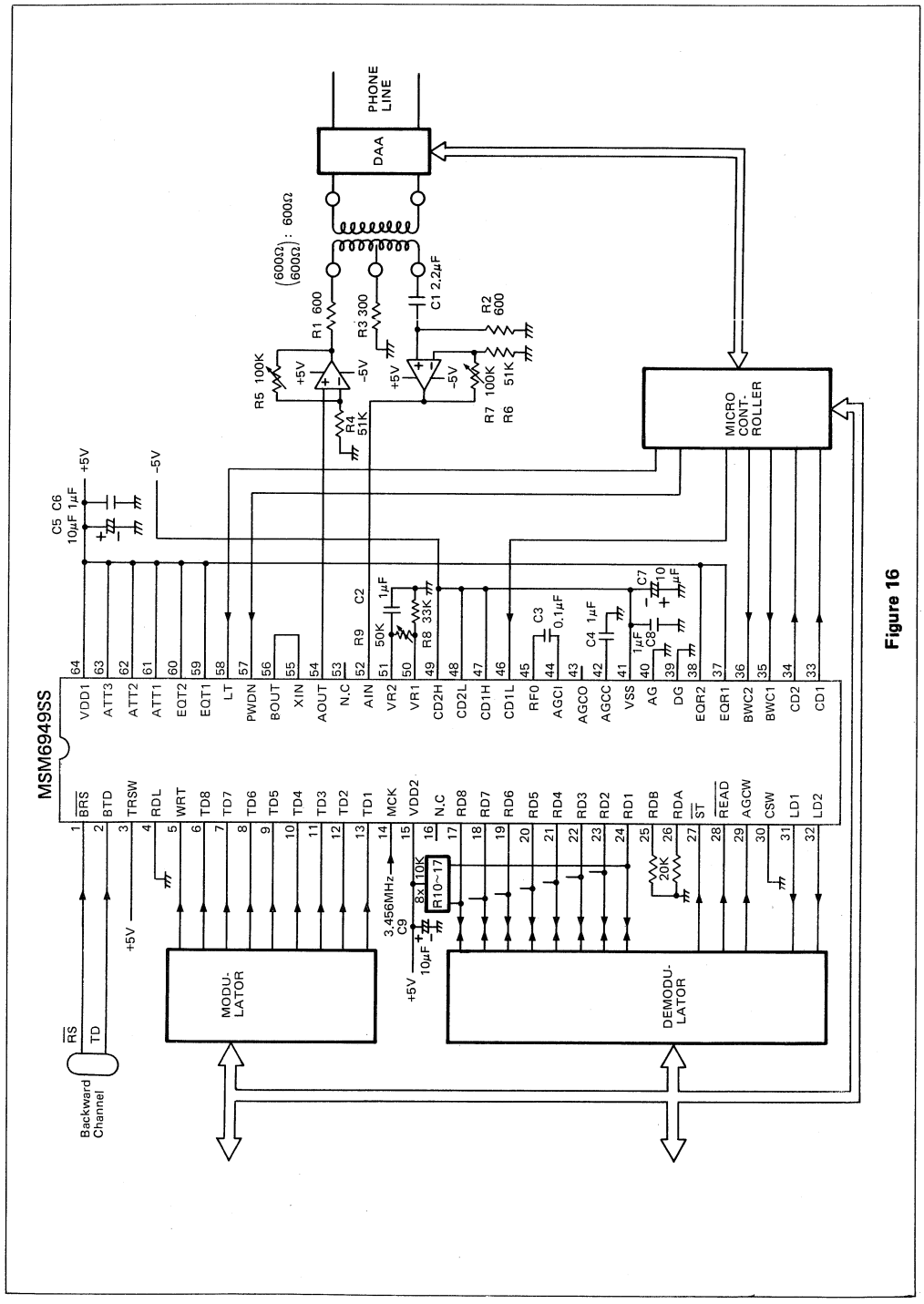


Figure 16

B. TELEPHONE APPLICATION

III

MSM6052

CMOS 4BIT SINGLE CHIP LOW POWER MICROCONTROLLER FOR TELEPHONE

GENERAL DESCRIPTION

The OKI MSM6052 is low-power and high-performance single-chip 4 bits microcontroller employing complementary Metal Oxide Semiconductor technology, especially designed for use in sophisticated telephone sets. Integrated onto a single chip are 4 bits ALU, 28 kbits of mask programmable ROM, 2560 bits of data RAM, programmable timer, oscillator, 12 bits of input port, 12 bits of output port and 4 bits of input/output port. In addition to these units, DTMF generator is provided.

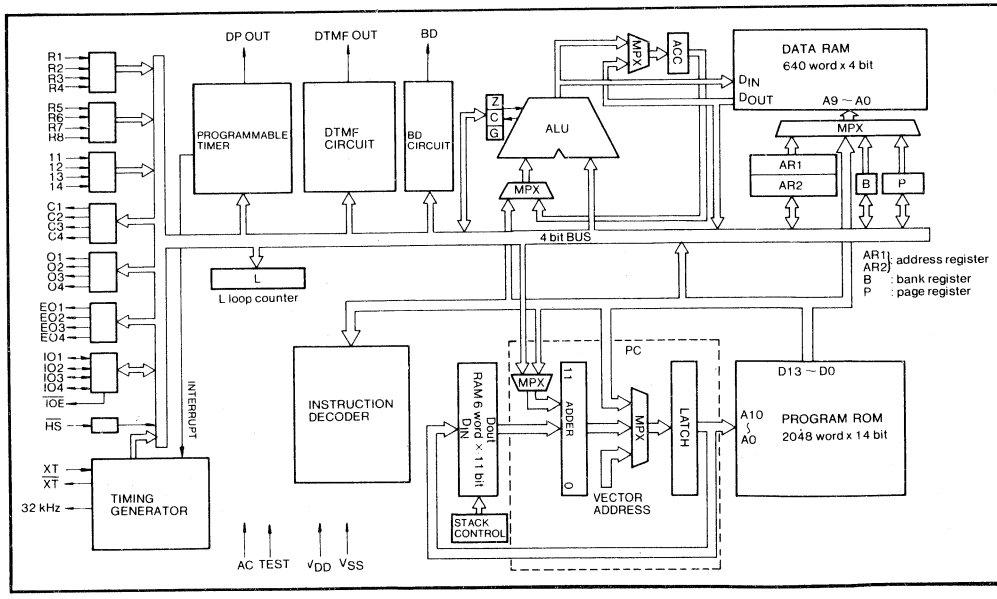
With MSM6052, sophisticated telephone sets become feasible by a single chip instead of conventional 3-chip configuration.

FEATURES

- Low Power Consumption 0.3mA Typical @3V (DTMF output off)
- 2048 × 14 Internal ROM
- 640 × 4 Internal RAM
- 3 × 4 Input Port
- 3 × 4 Output Port
- 1 × 4 Input/Output Port
- DTMF Generator
- Buzzer Sound Output
- 4 Bits Programmable Timer Applicable for Output of Dial Pulse
- Interrupt by Progammable Timer
- 5 Level Stack
- Power Down Mode
- 52 Instruction Sets
- Instructions Useful for Data Management (Data Search and Block Data Transfer)
- 2.5 to 6.0V Operating Voltage
- 3.58 MHz Oscillator
- 17.9 μS Instruction Cycle
- −20 to 75°C Operating Temperature
- 28 Pin DIP or 40 Pin DIP or 44 Pin FLAT

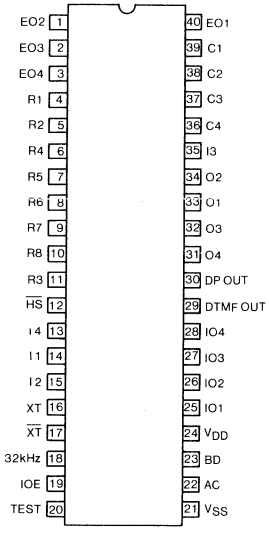
III

FUNCTIONAL BLOCK DIAGRAM

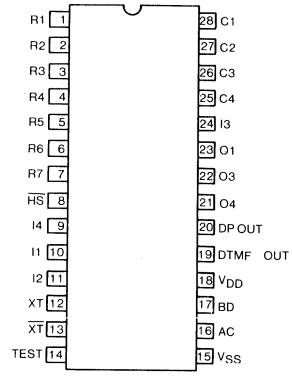


PIN CONFIGURATION

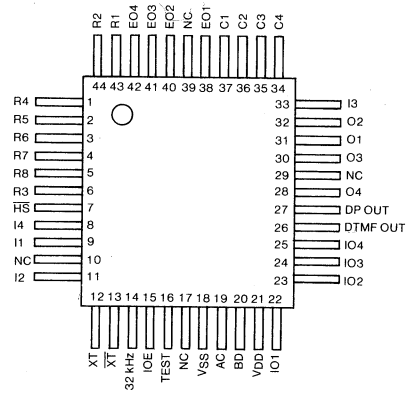
(Top View) 40 Lead Plastic DIP



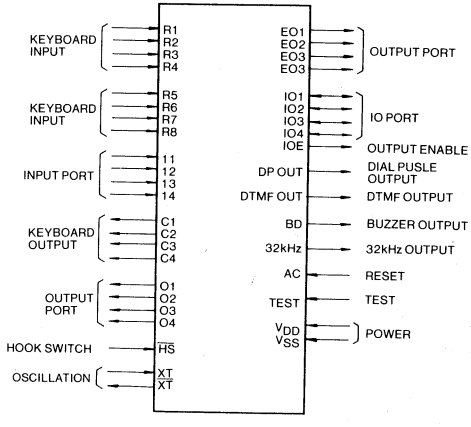
(Top View) 28 Lead Plastic DIP



(Top View) 44 Lead Plastic Flat Package



LOGIC SYMBOL



PIN DESCRIPTION

Pin Name	Function
V_{DD}	Pource source
V_{SS}	Circuit ground potential
AC	Terminal to clear internal logic, pulled down to V_{SS}. After power is turned on, the MSM6052 must be reset by this terminal.
TEST	Terminal to test internal logic, pulled down to V_{SS}. This terminal must be open in normal operation.
XT, $\overline{XT}$	Input and output terminals of oscillator inverter. 3.58 MHz ceramic resonator is connected to these terminals.
$\overline{HS}$	Input terminal connected to the hook switch, pulled up tp V_{DD}.
DP OUT	Output terminal of dial pulse. Dial pulse rate (10 pps or 20 pps) and Make Break ràtio (40% or 33 %) can be selected by software.
DTMF OUT	Output terminal of DTMF signal
BD	Output terminal of buzzer sound
32 kHz	Output terminal of 32 kHz clock
$R_1 \sim R_4$ $R_5 \sim R_8$	Input port pulled down to V_{SS}.
$I_1 \sim I_4$	Input port having clocked pull-down resistor to V_{SS}. Only when this port is accessed, pull-down resistors are connected to this port.
$C_1 \sim C_4$ $O_1 \sim O_4$	Output port
$IO_1 \sim IO_4$	Tri-state bidirectional port
IOE	Output terminal When $IO_1 \sim IO_4$ is accessed, input completion signal (when read) or load signal (when written) is output from IOE terminal.

FUNCTIONAL DESCRIPTION

A block diagram of the MSM6052 is given on page 102. Each block of logic will be briefly discussed. For more information, please refer to the MSM6052 user's manual.

Program ROM

The MSM6052 will address up to 2 k words of internal mask programmable ROM. Each word consists of 14 bits and all instructions are one word. The instructions are routed to a programmed logic array which generates the signals necessary for control of logic.

Data RAM

Data is organized in 4 bit nibbles. Internal data RAM consists of 640 nibbles.

All locations are addressed by 10 bits address registers (AR_1, AR_2), 2 bits bank register (B), 4 bits page register (P) or a part of the instruction's operand.

ALU

The ALU performs 4 bits parallel operation of RAM and ACC contents, or RAM contents and an immediate digit. It sets or resets the three flags (Z, C, G) depending on the condition.

Program Counter (PC)

The program counter is 11 bits wide counter to specify the address of program ROM.

The PC is incremented by one every execution of the instruction, and then specifies the next instruction to be executed. However, the contents of the PC are rewritten by the execution of Jump, Call or Branch instruction.

As there is no boundary in the ROM, Jump, Call or Branch instruction can be put anywhere in the ROM

Stack

The MSM6052 has 5 level stack aparting from data RAM. The contents of the PC are loaded into stack when Call instruction is executed or interrupt is generated. Nesting of subroutines within subroutines can continue up to 4 times including the interrupt.

Input Port

Port (R1 ~ R4)

4 bits input port. Each pin of the ports is pulled down to V_{SS} by internal resistor, and status of the port is fetched by input instruction.

Port (R5 ~ R8)

4 bits input port. Each pin of the port is pulled down to V_{SS} by internal resistor, and status of the port is fetched by input instruction.

Port (I1 ~ I4)

4 bits input port. Each pin of the ports is pulled down to V_{SS} by internal resistor and transistor. Only when it is desired to fetch status of the port, input current flows through these pins. Status of the port is fetched by input instruction.

Output Port

Port (C1 ~ C4)

4 bits output port. These ports consist of data latches and buffers, and the contents of data latches are rewritten by output instruction.

Port (O1 ~ O4)

4 bits output port. These ports consist of data latches and buffers, and the contents of data latches are rewritten by output instruction.

Electrical characteristics of O3 and O4 are different from those of O1 and O2. O3 and O4 of the ports are used as $\overline{\text{XMIT MUTE}}$ and $\overline{\text{MUTE}}$ normally.

Port (EO1 ~ EO4)

4 bits output port. These ports consist of data latches and buffers, and the contents of data latches are rewritten by output instruction.

- **Input/Output Port**

Port (IO1 ~ IO4)

4 bits bidirectional port. These ports consist of data latches, output buffers and input buffers. The contents of data latches are rewritten by output instruction and status of the port is fetched by input instruction.

Address Registers (AR1, AR2)

The address registers are used to specify 10 bits address of data RAM, when data search instruction (RDAR) or block data transfer instruction (MVAR) is executed.

These registers are up/down counter, and incremented or decremented by 1 with execution of the instruction.

Timing Generator

By connecting 3.58 MHz ceramic resonator to XT and $\overline{\text{XT}}$ terminal, the timing generator generates basic timing signal to control the MSM6052.

The MSM6052 can operate in 2 modes, normal operating mode and power down mode. STOP instruction is used to place the MSM6052 in the power down mode. The oscillation stops and the entire functions are stopped. However, the contents of RAM and all registers are maintained.

Programmable Timer

The programmable timer consists of 4 bits down counter and 1/100 prescaler.

Any of 7990.1 Hz clock, 1997.5 Hz clock and 998.8 Hz clock is input to 1/100 prescaler. Output of 1/100 prescaler decrements 4 bits down counter by 1.

When the contents of 4 bits down counter is decremented to 0, the programmable timer generates interrupt.

This programmable timer can be used as dial pulse generator. Dial pulse rate (10 pps, 20 pps) and Make/Break ratio (40%, 33%) of dial pulse which the programmable timer generates are selectable.

DTMF Circuit

DTMF circuit is used to generate DTMF signal. 12 kinds of DTMF signal (0 to 9, #, *) can be output by output instruction.

BD Circuit

BD circuit generates the square wave which can be used as the confirmation sound, warning sound and so on. 15 kinds of sound (4.66 to 0.82 kHz) are output by output instruction specifying the frquency.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Limits	Unit
Supply Voltage	V_{DD}	Ta = 25°C	−0.3 to 7.0	V
Input Voltage	V_I	Ta = 25°C	−0.3 to V_{DD}+0.3	V
Output Voltage	V_O	Ta = 25°C	−0.3 to V_{DD}+0.3	V
Storage Temperature	Tstg	—	−55 to 125	°C
Power Dissipation	P_D	Ta = 25°C	200	mW

OPERATING CONDITIONS

Parameter	Symbol	Limits	Unit
Operating Voltage	V_{DD}	2.5 to 6.0	V
Memory Retension Voltage	V_{DDM}	1.2 to 6.0	V
Operating Temperature	Topr	−20 to 75	°C

DC CHARACTERISTICS

(VDD = 3V, Ta = −20 to 75°C)

Parameter	Symbol	Conditions		Limits			Unit
				Min	Typ	Max	
"H" Input Voltage	V_{IH}	V_{DD}=3V		2.2	—	—	V
		V_{DD}=6V		4.4	—	—	V
"L" Input Voltage	V_{IL}	V_{DD}=3V		—	—	0.8	V
		V_{DD}=6V		—	—	1.6	V
"H" Output Current (1)	I_{OH1}	O_3, O_4 DP OUT	V_{OH}=2.6V	−200	—	—	μA
"L" Output Current (1)	I_{OL1}		V_{OL}=0.4V	500	—	—	μA
"H" Output Current (2)	I_{OH2}	$C_1 \sim C_4$	V_{OH}=2.6V	−1	—	—	mA
"L" Output Current (2)	I_{OL2}		V_{OL}=0.4V	10	—	—	μA
"H" Output Current (3)	I_{OH3}	O_1, O_2, BD	V_{OH}=2.6V	−20	—	—	μA
"L" Output Current (3)	I_{OL3}		V_{OL}=0.4V	10	—	—	μA

DC CHARACTERISTICS (CONT.)

Parameter	Symbol	Conditions		Limits Min	Limits Typ	Limits Max	Unit
"H" Output Current (4)	I_{OH4}	$IO_1 \sim IO_4$ IOE $EO_1 \sim EO_4$	V_{OH}= 2.6V	−150	–	–	μA
"L" Output Current (4)	I_{OL4}		V_{OL}= 0.4V	300	–	–	μA
"H" Output Current (5)	I_{OH5}	32 kHz	V_{OH}=2.6V	−40	–	–	μA
"L" Output Current (5)	I_{OL5}		V_{OL}=0.4V	25	–	–	μA
Pull-up Resistance	R_{UP}	$\overline{HS}$		17	–	150	kΩ
Pull down Resistance (1)	Rdwon 1	$R_1 \sim R_8$		33	–	300	kΩ
Pull down Resistance (2)	Rdwon 2	$I_1 \sim I_4$, AC, TEST		10		100	kΩ
Input Leak Current	I_{IL}	$IO_1 \sim IO_4$	$0 \leq V_{IN} \leq V_{DD}$ V_{DD}= 2.5 to 6.0V	–	–	±2	μA
Current Consumption (1)	I_{DDP}	DTMF output off	V_{DD}= 3V	–	0.3	0.6	mA
			V_{DD}= 6V	–	1.2	2.4	mA
Current Consumption (2)	I_{DDT}	DTMF output on	V_{DD}= 3V	–	1.2	2.4	mA
			V_{DD}=6V	–	3.5	7.0	mA
Memory retention Current	I_{DDM}	ON HOOK V_{DD}=2.5V	Ta=25°C	–	0.01	0.2	μA
			Ta=−20to75°C	–	–	2	μA

III

AC CHARACTERISTICS

(VDD = 3V, Ta = −20 to 75°C)

Parameter	Symbol	Conditions		Limits Min	Limits Typ	Limits Max	Unit
Key Input Time	T_{KIN}	V_{DD}=2.5 to 6.0V		33	–	–	ms
Tone Output Voltage	V_{OUT}	Row only R_L=1 kΩ	V_{DD}=2.5V	–	250	–	mV rms
			V_{DD}=4.0V	–	350	–	
			V_{DD}=6.0V	–	480	–	
High/Low Level Ratio	dB_{CR}	V_{DD}=2.5 to 6.0V		1	2	3	dB
Distortion Ratio	%DIS	R_L=1 kΩ		–	1	5	%
Rise/Fall Time (1)	t_{TLH1}	O_3, O_4, DP OUT C_L=50 pF		–	–	0.5	μS
	t_{THL1}			–	–	0.5	
Rise/Fall Time (2)	t_{TLH2}	$C_1 \sim C_4$ C_L=50 pF		–	–	0.5	μS
	t_{THL2}			–	–	10	
Rise/Fall Time (3)	t_{TLH3}	O_1, O_2, BD, 32 kHz C_L=50 pF		–	–	5	μS
	t_{THL3}			–	–	10	
Rise/Fall Time (4)	t_{TLH4}	IO_1~IO_4, IOE, $EO_1 \sim EO_4$ C_L=50 pF		–	–	1	μS
	t_{THL4}			–	–	1	

DESCRIPTION OF INSTRUCTIONS

	Mnemonic	Instruction Code														Operation
		13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Arithmetic and logic	ADD ACC, AP	0	0	0	0	0	P	0	1	0	0	A				AP ← (AP) + ACC
	ADD #D, AP	0	1	1	0	0	P	D				A				AP ← (AP) + D
	ADC AP	0	0	0	0	0	P	0	1	0	1	A				AP ← (AP) + ACC + C
	SUB ACC, AP	0	0	0	0	1	P	0	1	0	0	A				AP ← (AP) − ACC
	SUB #D, AP	0	1	1	0	1	P	D				A				AP ← (AP) − D
	SBC AP	0	0	0	0	1	P	0	1	0	1	A				AP ← (AP) − ACC − C
	CMP ACC, AP	0	0	0	0	1	P	1	1	1	0	A				(AP) − ACC
	CMP #D, AP	0	1	0	1	1	P	D				A				(AP) − D
	XOR ACC, AP	0	0	0	0	0	P	0	1	1	1	A				AP ← (AP) ∀ ACC
	XOR #D, AP	0	1	1	1	1	P	D				A				AP ← (AP) ∀ D
Bit operation	BIT ACC, AP	0	0	0	0	0	P	1	1	1	0	A				(AP) V $\overline{ACC}$
	BIT #D, AP	0	1	0	1	0	P	D				A				(AP) V $\overline{D}$
	BIS ACC, AP	0	0	0	0	0	P	0	1	1	0	A				AP ← (AP) V ACC
	BIS #D, AP	0	1	0	0	0	P	D				A				AP ← (AP) V D
	BIC ACC, AP	0	0	0	0	1	P	0	1	1	0	A				AP ← (AP) Λ $\overline{ACC}$
	BIC #D, AP	0	1	0	0	1	P	D				A				AP ← (AP) Λ $\overline{D}$
Rotate	ROR AP	0	0	0	0	0	P	0	0	1	0	A				⌊(AP) → C⌋
	ROL AP	0	0	0	0	1	P	0	0	1	0	A				⌊(AP) ← C⌋
	ASR AP	0	0	0	0	0	P	0	0	1	1	A				0 → (AP) → C
	ASL AP	0	0	0	0	1	P	0	0	1	1	A				C ← (AP) ← 0
Flag operation	SEZ	0	0	0	0	1	0	1	0	1	0	0	0	0	0	Z ← 1
	CLZ	0	0	0	0	0	0	1	0	1	0	0	0	0	0	Z ← 0
	SEC	0	0	0	0	1	0	1	0	0	1	0	0	0	0	C ← 1
	CLC	0	0	0	0	0	0	1	0	0	1	0	0	0	0	C ← 0
	SEG	0	0	0	0	1	0	1	0	0	0	0	0	0	0	G ← 1
	CLG	0	0	0	0	0	0	1	0	0	0	0	0	0	0	G ← 0
	SEA	0	0	0	0	1	0	1	0	1	1	0	0	0	0	Z ← 1, C ← 1, G ← 1
	CLA	0	0	0	0	0	0	1	0	1	1	0	0	0	0	Z ← 0, C ← 0, G ← 0
Data transfer	MOV ACC, AP	1	1	1	1	0	1	0	0	0	0	A				AP ← ACC
	MOV ACC, AX	1	1	1	1	0	0	X				A				AX ← ACC
	MOV #D, AP	0	1	1	1	0	P	D				A				AP ← D
	MOV AP, ACC	1	1	1	1	1	1	0	0	0	0	A				ACC ← (AP)
	MOV AX, ACC	1	1	1	1	1	0	X				A				ACC ← (AX)
	CHG AP	1	1	1	0	0	1	0	0	0	0	A				(AP) ⟷ ACC

DESCRIPTION OF INSTRUCTIONS (CONT.)

	Mnemonic	Instruction Code												Operation
		13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Data transfer	CHG AX	1	1	1	0	0	0	X				A				(AX) ⟷ ACC
	RDAR	1	1	0	0	0	0	0	0	0	0	0	0	0	0	ACC ← (AR_1)
	RDAR + (−)	1	1	0	0	0	0	0	0	1	D/I	0	0	0	0	ACC ← (AR_1), AR_1 ← $AR_1 \pm 1$
	RDAR + (−), Z	1	1	0	0	0	0	0	1	0	D/I	0	0	0	0	ACC ← (AR_1) if (AR_1)=0 then PC ← PC + 1 else AR_1 ← $AR_1 \pm 1$, repeat
	RDAR + (−), N	1	1	0	0	0	0	1	0	0	D/I	0	0	0	0	ACC ← (AR_1) if (AR_1)≠0 then PC ← PC + 1 else AR_1 ← $AR_1 \pm 1$, repeat
	RDAR + (−), Z, L	1	1	0	0	1	0	0	1	0	D/I	0	0	0	0	ACC ← (AR_1), L ← L − 1 if (AR_1)=0 or L=0 then PC← PC+1 else AR_1 ← $AR_1 \pm 1$, repeat
	RDAR + (−), N, L	1	1	0	0	1	0	1	0	0	D/I	0	0	0	0	ACC ← (AR_1), L ← L − 1 if (AR_1)≠0 or L=0 then PC ← PC + 1 else AR_1 ← $AR_1 \pm 1$, repeat
	MVAR	1	1	0	1	0	0	0	0	0	0	0	0	0	0	AR_2 ← (AR_1)
	MVAR + (−)	1	1	0	1	0	0	0	0	1	D/I	0	0	0	0	AR_2 ← (AR_1), AR_1 ← $AR_1 \pm 1$, AR_2 ← $AR_2 \pm 1$
	MVAR + (−), Z	1	1	0	1	0	0	0	1	0	D/I	0	0	0	0	AR_2 ← (AR_1), if (AR_1)=0 then PC ← PC +1 else AR_1 ← $AR_1 \pm 1$, AR_2 ← $AR_2 \pm 1$, repeat
	MVAR + (−), N	1	1	0	1	0	0	1	0	0	D/I	0	0	0	0	AR_2 ← (AR_1) if (AR_1)≠0 then PC ← PC +1 else AR_1 ← $AR_1 \pm 1$, AR_2 ← $AR_2 \pm 1$, repeat
	MVAR + (−), L	1	1	0	1	1	0	0	0	0	D/I	0	0	0	0	AR_2 ← (AR_1), L ← L − 1 if L=0 then PC ← PC +1 else AR_1 ← $AR_1 \pm 1$, AR_2 ← $AR_2 \pm 1$, repeat
	MVAR + (−), Z, L	1	1	0	1	1	0	0	1	0	D/I	0	0	0	0	AR_2 ← (AR_1), L ← L −1 if (AR_1)=0 or L=0 then PC ← PC +1 else AR_1 ← $AR_1 \pm 1$, AR_2 ← $AR_2 \pm 1$, repeat
	MVAR + (−), N, L	1	1	0	1	1	0	1	0	0	D/I	0	0	0	0	AR_2 ← (AR_1), L ← L −1 if (AR_1)≠0 or L=0 then PC ← PC +1 else AR_1 ← $AR_1 \pm 1$, AR_2 ← $AR_2 \pm 1$, repeat
Sub routine	CALL adrs	1	0	1	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0	STACK ← (PC), PC ← adrs
	RET	0	0	0	0	0	0	1	1	0	0	0	0	0	0	PC ← (STACK) + 1
	RTI	0	0	0	0	1	0	1	1	0	0	0	0	0	0	PC ← (STACK) or PC ← (STACK) +1

DESCRIPTION OF INSTRUCTIONS (CONT.)

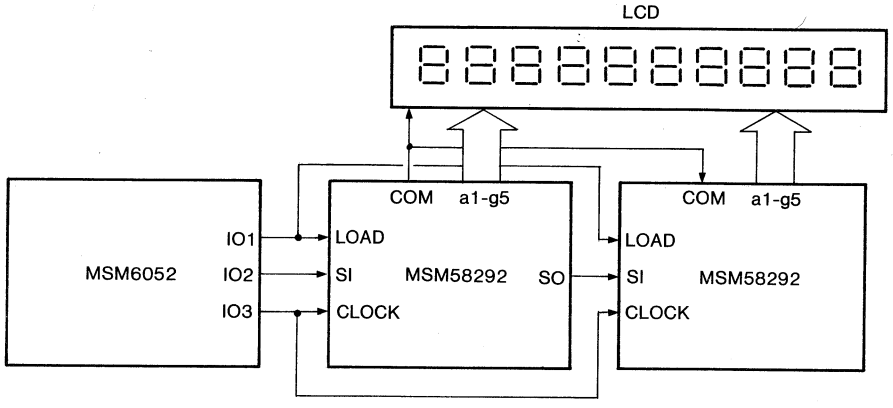
	Mnemonic	Instruction Code 13 12	11 10 9 8	7 6 5 4	3 2 1 0	Operation
Jump	JMP adrs	1 0	0 a_{10} a_9 a_8	a_7 a_6 a_5 a_4	a_3 a_2 a_1 a_0	PC ← adrs
	JMP @AP	0 0	0 0 0 P	1 1 0 1	A	PC ← (PC) + (AP) + 1
	JMPIO @AP	0 0	0 0 1 P	1 1 0 1	A	PC ← (PC) + {(AP) ∧ 7H} +1
Branch	BEQ n (BZE n)	1 1	1 0 1 P	0 1 0 n_4	n_3 n_2 n_1 n_0	if Z=1 then PC←PC − n or PC ← PC + n +1 else ← PC ← PC + 1
	BNE n (BNZ n)	1 1	1 0 1 P	1 1 0 n_4	n_3 n_2 n_1 n_0	if Z=0 then PC←PC − n or PC ← PC + n + 1 else PC ← PC +1
	BCS n	1 1	1 0 1 P	0 0 0 n_4	n_3 n_2 n_1 n_0	if C=1 then PC ← PC −n or PC ← PC + n + 1 else PC ← PC +1
	BCC n	1 1	1 0 1 P	1 0 0 n_4	n_3 n_2 n_1 n_0	if C=0 then PC ← PC − n or PC ←-PC+n+1 else PC ← PC +1
	BGT n	1 1	1 0 1 P	0 0 1 n_4	n_3 n_2 n_1 n_0	if G=1 then PC ← PC − n or PC ← PC + n + 1 else PC ← PC +1
	BLE n	1 1	1 0 1 P	1 0 1 n_4	n_3 n_2 n_1 n_0	if G=0 then PC ← PC − n or PC ← PC +n+1 else PC ← PC +1
	BGE n	1 1	1 0 1 P	0 1 1 n_4	n_3 n_2 n_1 n_0	if G=1 or Z=1 then PC ← PC − n or PC ← PC+n+1, else PC ← PC +1
	BLT n	1 1	1 0 1 P	1 1 1 n_4	n_3 n_2 n_1 n_0	if G=0 and Z=0 then PC ← PC −n or PC ← PC+n+1 else PC ← PC+1
Input/ Output	IN PORT, AP	0 0	0 1 0 P	P_L	A	AP ← (PORT)
	OUT AP, PORT	0 0	1 0 P_H P	P_L	A	PORT ← (AP)
	OUT #D, PORT	0 0	1 1 P_H 0	P_L	D	PORT ← D
CPU control and others	STOP	0 0	1 1 1 0	0 0 0 0	0 0 0 0	Stop system clock
	HALT	0 0	1 1 1 0	0 0 0 1	0 0 0 0	Halt CPU
	ACT	0 0	1 1 1 0	0 0 1 0	0 0 0 0	Activate CPU
	EI	0 0	1 1 1 0	0 1 1 0	1 0 0 0	Enable timer interrupt
	DI	0 0	1 1 1 0	0 1 1 0	0 1 0 0	Disable timer interrupt
	ET	0 0	1 1 1 0	0 1 1 0	0 0 1 0	Enable timer activate
	DT	0 0	1 1 1 0	0 1 1 0	0 0 0 1	Disable timer activate
	EC	0 0	1 1 1 0	0 1 1 1	1 0 0 0	Enable output port (C_1~C_4)
	DC	0 0	1 1 1 0	0 1 1 1	0 1 0 0	Disable output port (C_1~C_4)

DESCRIPTION OF INSTRUCTIONS (CONT.)

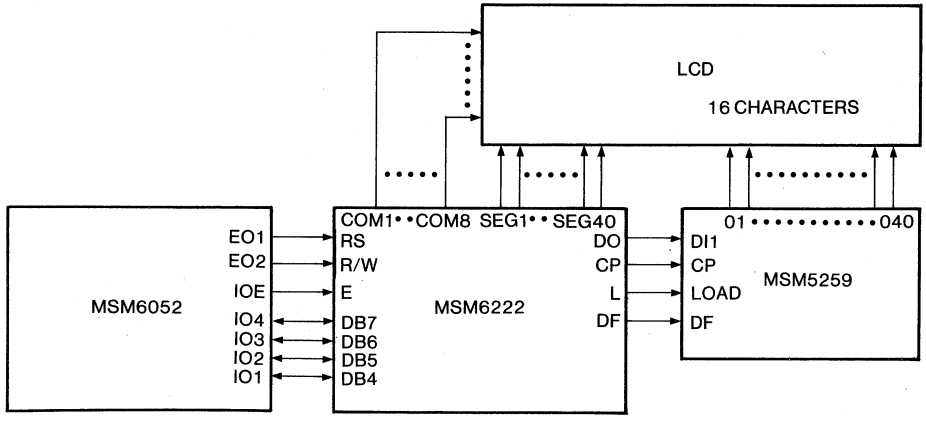
	Mnemonic	Instruction Code 13 12	11 10 9 8	7 6 5 4	3 2 1 0	Operation
CPU control and others	OM	0 0	1 1 1 0	0 1 1 1	0 0 1 0	Set I/O port (IO_1~IO_4) to output mode
	IM	0 0	1 1 1 0	0 1 1 1	0 0 0 1	Set I/O port (IO_1~IO_4) to input mode
	RST	0 0	1 1 1 0	1 0 0 1	0 0 0 0	Reset divider
	NOP	0 0	0 0 0 0	0 0 0 0	0 0 0 0	No operation

APPLICATION FOR DISPLAY TELEPHONE

INTERFACING WITH LCD SEGMENT DRIVER

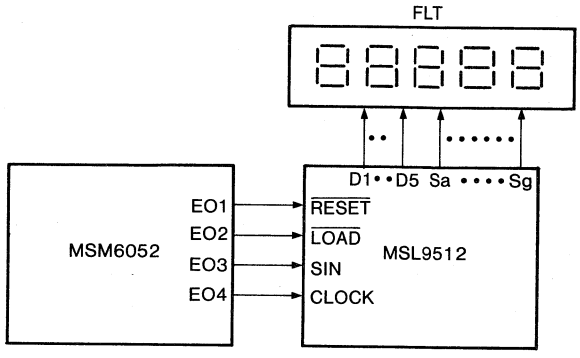


INTERFACING WITH A DCT MATRIX LCD DRIVER/CONTROLLER



APPLICATION FOR DISPLAY TELEPHONE (CONT.)

INTERFACING WITH FLT SEGMENT DRIVER



MSM6052-01RS/20RS

TONE/PULSE SWITCHABLE REPERTORY DIALER

GENERAL DESCRIPTION

The MSM6052-01RS and MSM6052-20RS are repertory tone/pulse switchable dialer which are fabricated by OKI's low power consumption CMOS silicon gate technology. These LSIs can generate either DTMF (Dual Tone Multi Frequency) signal or DP (Dial Pulse) signal.

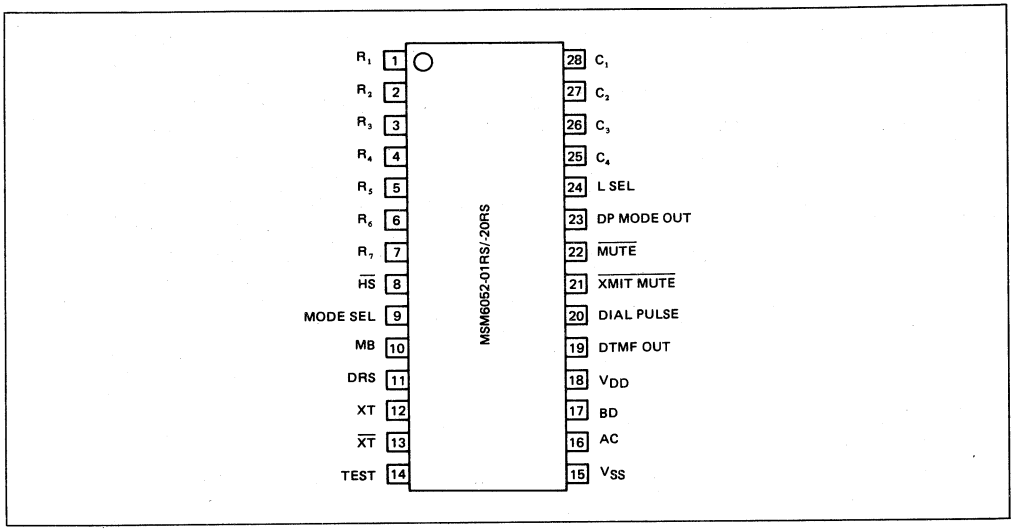
The repertory memory has a capacity of 500 digits. Maximum 54 telephone numbers of 32 digits maximum/number can be stored in it, so far as total number of stored digits does not exceed 500.

It operates on 2.5 V ~ 6 V single supply. Standby current is 0.2 μA maximum and memory retention voltage is 1.2 V.

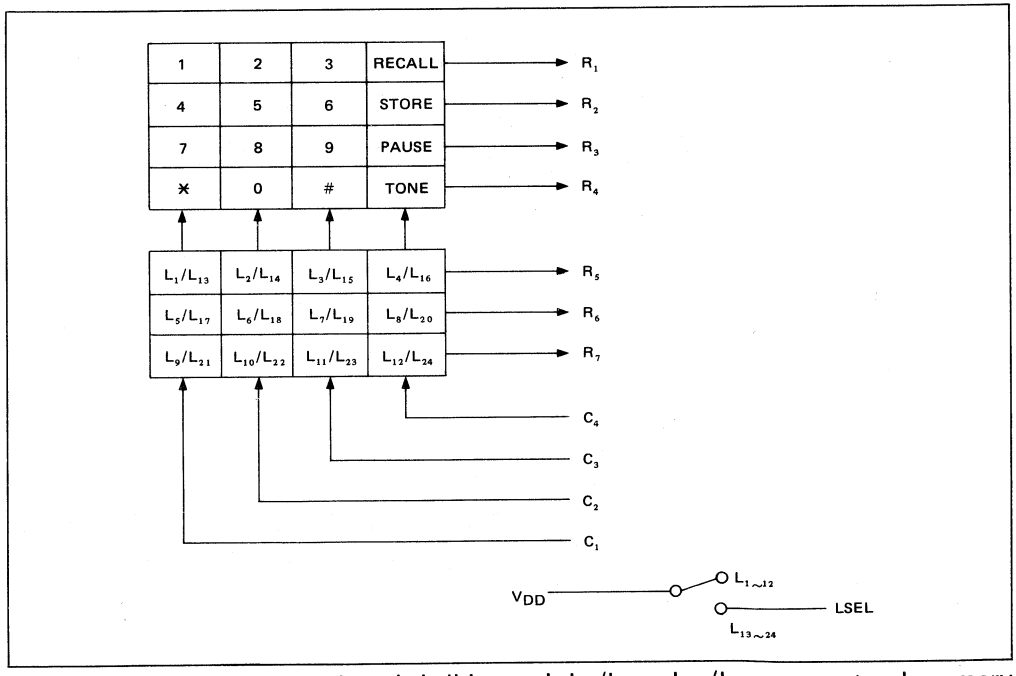
FEATURES

- Either DTMF signal or DP signal generation.
- DP/TONE output starts 100 msec after keying in normal dialing (-20RS).
- DP/TONE output starts 300 msec after keying in normal dialing (-01RS).
- 500 digits repertory memory. (54 numbers maximum, 32 digits maximum/number).
- 24 numbers repertory dialing by single key dialing plus maximum 30 numbers repertory dialing by 2-digit abbreviated code dialing.
- Last number redial (32 digits maximum).
- Mixed dialing/storing.
- Auto insersion of 4 seconds access pause.
- Pulse rate 10/20 pps pin selectable.
- Make/Break ratio 34/66 or 40/60 pin selectable.
- Tone output for valid key input (2 kHz, 32 msec).
- Alarm tone for wrong operations.
- Single contact matrix keyboard to be used.
- 3.58 MHz oscillation circuit on chip for ceramic resonator.
- Supply voltage range 2.5 V ~ 6 V.
- Low standby current 0.2 μA maximum.
- 28-pin plastic DIP Package.

PIN CONFIGURATION



KEYBOARD INTERFACE



A 7 x 4 single contact keyboard shall be used. $L_1/L_{13} \sim L_{12}/L_{24}$ are one touch memory recall keys. By connecting or disconnecting LSEL to/from V_{DD}, two telephone numbers can be assigned for each key. So, the 24 numbers in total can be recalled by single key operation.

In addition to it, maximum 30 numbers can be abbreviated into 2-digit address code (00 ~ 29).

PIN DESCRIPTION

Pin Name	Pin No.	Function
$R_1 \sim R_7$ $C_1 \sim C_4$	1 ~ 7 25 ~ 28	Key input pins. $C_1 \sim C_4$ are set to low level in on-hook mode, while they are set to high level in off-hook standby mode. When the key input is off, key scanning and oscillation stop. Single contact keyboard shall be connected.
$\overline{HS}$	8	Hook switch input pin. $\overline{HS}$ = High: On-hook $\overline{HS}$ = Low: Off-hook
LSEL	24	Selection pin for $L_1 \sim L_{12}$ or $L_{13} \sim L_{24}$ for single-key dialing LSEL = Low: $L_1 \sim L_{12}$ LSEL = High: $L_{13} \sim L_{24}$
MB	10	Make/Break ratio selection pin. MB = Low: 40/60 MB = High: 34/66 This input is sensed during the transition stage from On-hook to Off-hook.
DRS	11	Dial rate selection pin. DRS = Low: 10 pps DRS = High: 20 pps This input is sensed during the transition stage from On-hook to Off-hook.
MODE SEL	9	DP/DTMF mode selection pin. MODE SEL = Low: DP mode MODE SEL = High: DTMF mode The status at off-hook is maintained. If [TONE] key is pressed when this pin is being set to low level, the DTMF mode is established.
XT, $\overline{XT}$	12, 13	Ceramic resonator connection pins. Since this LSI is provided with oscillation inverter and feed-back resistor, 3.58 MHz ceramic resonator and capacitors are connected to XT and $\overline{XT}$ pin.
V_{DD}, V_{SS}	18, 15	V_{DD}: Positive power supply pin. 2.5 V ~ 6 V. V_{SS}: Negative power supply pin (Ground).
AC	16	IC initial pin. When IC is powered on, "H" level reset signal has to be applied to this pin.
TEST	14	Test pin.

Pin Name	Pin No.	Function
BD	17	Buzzer output pin. It outputs key tone for valid key input. It also outputs various alarm/confirming tone. Refer to "Sound output waveforms" for details.
DTMF OUT	19	DTMF output pin. In case of double keying or pressing some key without releasing a previous key, DTMF output is disabled.
DIAL PULSE	20	Dial pulse output pin. Make: High Break: Low $\overline{HS}$ = High (On hook): Low
$\overline{XMIT\ MUTE}$	21	Transmit mute output pin. When $\overline{HS}$ = High (On-hook): Low When $\overline{HS}$ = Low (Off-hook) ① While DP signal or DTMF signal is being sent out: Low ② All other times: High
$\overline{MUTE}$	22	Mute output pin. When $\overline{HS}$ = High (On-hook): Low When $\overline{HS}$ = Low (Off-hook) ① While DP is being sent out: Low ② All other times: High
DP MODE OUT	23	Dial Pulse Mode output pin. MODE SEL = High: Low MODE SEL = Low: High When mode is changed to DTMF mode by TONE key input: Low

III

FUNCTIONAL DESCRIPTION

Dialing Function

(1) Normal Dialing

Off-Hook [D_1].....[D_N]

Maximum 32 digits can be sent out at a time. Further key inputs are effective only after the first 32 digits have been sent out to the line. If more than 32 digits are dialed, redialing of that number is disabled. Pressing [PAUSE] key causes 4 seconds access pause. The access pause is released automatically 4 seconds later or manually by pressing [PAUSE], [RECALL], [STORE] or [TONE] key again.

Switching from DP dialing to DTMF dialing can be done during the course of dialing. By pressing [TONE] key during DP mode, the mode is changed to DTMF mode. When [TONE] key is pressed, if DP signal is being sent out, the mode will be changed after sending out all DP signal and an access pause of 4 seconds is automatically inserted. An access pause can be released earlier by pressing [PAUSE], [RECALL], [STORE] or [TONE] key, if so desired.

(2) Redialing

Off-Hook [R] [R]

The last dialed number can be redialed by pressing [RECALL] key twice. The functions of [TONE] and [PAUSE] signals included in the redialed number are same as in the repertory dialing. When the redialing is being prohibited, an alarm sound is generated at the second [RECALL] key input. The normal dialing can follow after that leaving the telephone off hook.

III

(3) Repertory Dialing

Off-Hook [R] [A_1] [A_2]

Off-Hook [L_n]

The telephone numbers abbreviated to [L_n] code can be dialed by single key operation ([L_1] ~ [L_{24}]), while those abbreviated to 2-digit can be dialed by pressing [RECALL] key followed by 2-digit code.

If a wrong address code is input, an alarm sound is generated.

If a stored number has an access pause, dialing halts for 4 seconds or until [PAUSE], [RECALL], [STORE] or [TONE] key is pressed. If a stored number has a [TONE] signal, the dialing mode is changed from DP mode to DTMF mode, and dialing halts for 4 seconds or until [PAUSE], [RECALL], [STORE] or [TONE] key is pressed.

(4) Mixed Dialing

Off-Hook [R] [R] [D_1] ..... [D_n] [R] [A_1] [A_2] [L_n]

- [R] [R]: Redial
- [D_1] ..... [D_n]: Normal dialing
- [R] [A_1] [A_2]: 2-digits abbreviated code dialing
- [L_n]: Single key dialing

Mixed dialing of normal dialing, redialing and repertory dialing can be done. In that case, however, redialing must come to the first part. If the digits of the mixed dialed number is up to 32, that number can be redialed.

Memory Storing/Clearing Function

(1) Storing of telephone number

Off-Hook [S] [D_1] ..... [D_n] [S] [A_1] [A_2] (Store into 2-digits abbreviated code address)

[S] [D_1] ..... [D_n] [S] [L] (Store into single key address)

Storing operation can be continued leaving the telephone off hook. When the storing of a telephone number has been completed, a sound is generated to indicate that the next number's storing is allowed. The first [STORE] key input can be omitted from the second number.

If the empty space of the repertory memory is less than 16 digits, an alarm sound is generated at the first [STORE] key input. In other words, if an alarm is not generated at the first [STORE] key input, minimum 16 digits can be newly stored.

An alarm sound is generated at the 500th digit input showing the memory has no more capacity. That 500th input digit can be stored in the memory, however, if the 501st digit is input, an alarm sound is generated again. That input digit is neglected and the entire key operation is disabled until the telephone is hooked on.

Maximum digits of a telephone number to be stored is 32. [TONE] signal and [PAUSE] signal are counted as one digit respectively.

If the 33rd digit is input, an alarm sound is generated and the entire key operation is disabled until the telephone is hooked on.

24 telephone numbers can be abbreviated to single key address codes, which are [L_1] ~ [L_{24}] . Other than those single key address codes, maximum 30 telephone numbers can be abbreviated to 2-digit address codes, which are 00 ~ 29, so fas as total stored digits in the repertory memory do not exceed 500.

[0] ~ [2] can be used for the first digit [A_1] , and [0] ~ [9] can be used for the second digit [A_2] . If a wrong number is used, an alarm sound is generated and that input is neglected.

(2) Mixed Storing

Off-Hook [S] [D_1] ..... [D_n] [R] [A_1] [A_2] [S] [A'_1] [A'_2]

..... Store into 2-digit abbreviated code address

Off-Hook [S] [L_m] [D_1] ..... [D_n] [L_n] [S] [L'_n]

..... Store into single key address

The telephone number once stored in the repertory memory can be used as a part of the newly stored telephone number in the form of abbreviated code ([L_n] or [R] [A_1] [A_2]). Maximum 32 digits can be mixed-stored. Either [L_n] or [R] [A_1] [A_2] is counted as 3 digits.

Therefore, if [L_n] key or [R] key is pressed at 31st or 32nd digit, an alarm sound is generated and storing is disabled.

Abbreviated code used for the newly stored number must not include abbreviated code of the other telephone number.

(3) Clearing of Telephone Number

Off-Hook [S] [S] [A_1] [A_2]

[S] [S] [L_n]

Clearing operation can be continued leaving the telephone off hook. Pressing [STORE] key twice followed by [L_n] key or 2-digit code clears the stored number in that address. Clearing operation and storing operation can be done alternately leaving the telephone off-hook.

If a wrong address code is input after pressing [STORE] key twice, an alarm sound is generated and that key input is neglected.

Redial Inhibition

Off-Hook [R] [A_1] [A_2] (After signals sent out) [S] [S]

Off-Hook [D_1] ..... [D_n] (After signals sent out) [S] [S]

Pressing [STORE] key twice after all signals have been sent out to the line disables the redialing of that telephone number. It is applicable to any of normal dialing, repertory dialing and mixed dialing. Redialing is also disabled when more than 32 digits are dialed or after telephone number's clearing/storing operation.

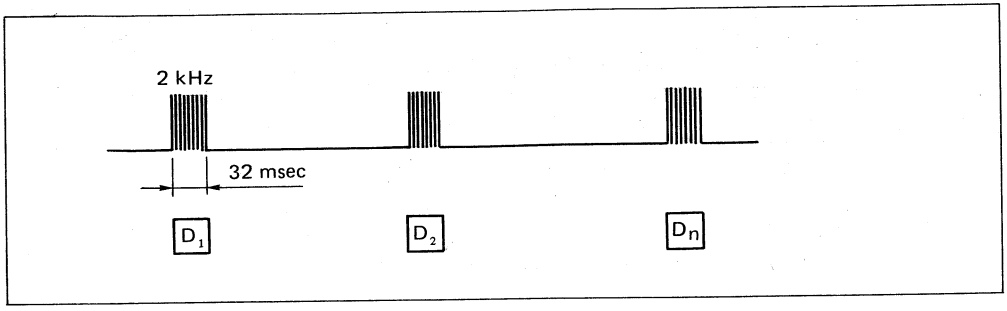
Others

When there is no data in the specified memory address, an alarm sound is generated and that key input is neglected.

SOUND OUTPUT WAVEFORM

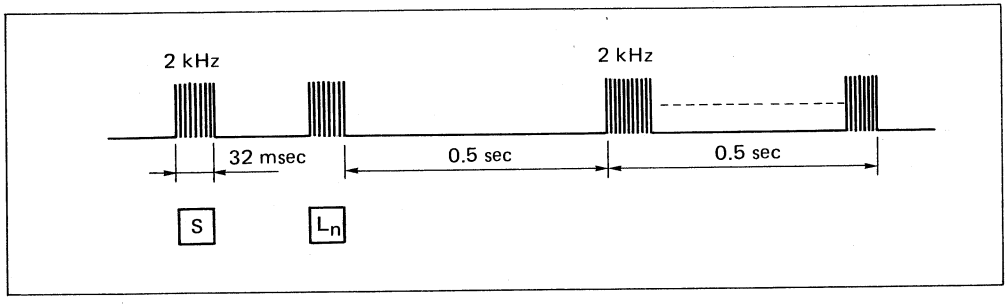
Operation Confirmation Sound

It is output for valid key input.



Storing Confirmation Sound

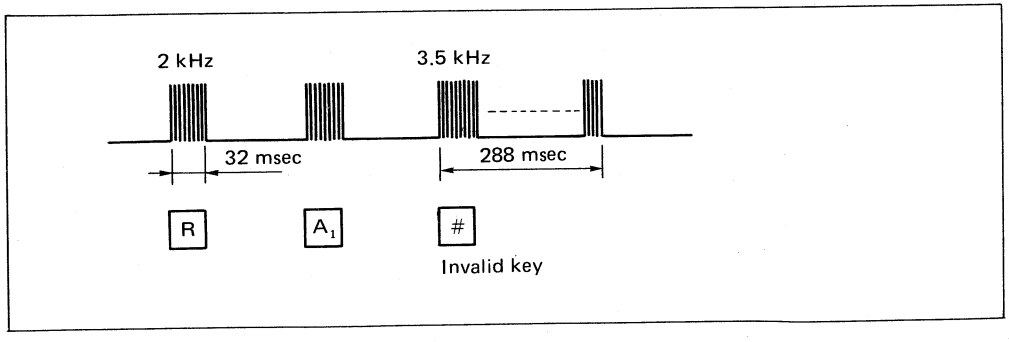
It is output when storing or clearing of telephone number has been completed.



Alarm Sound (a)

It is output for the followings.

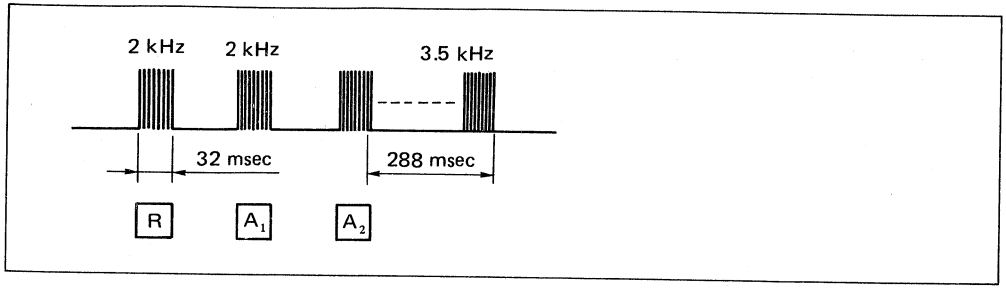
- Wrong key input.
- 33rd digit input for storing.
- STORE key input when the empty capacity of repertory memory is less than 16 digits.



III

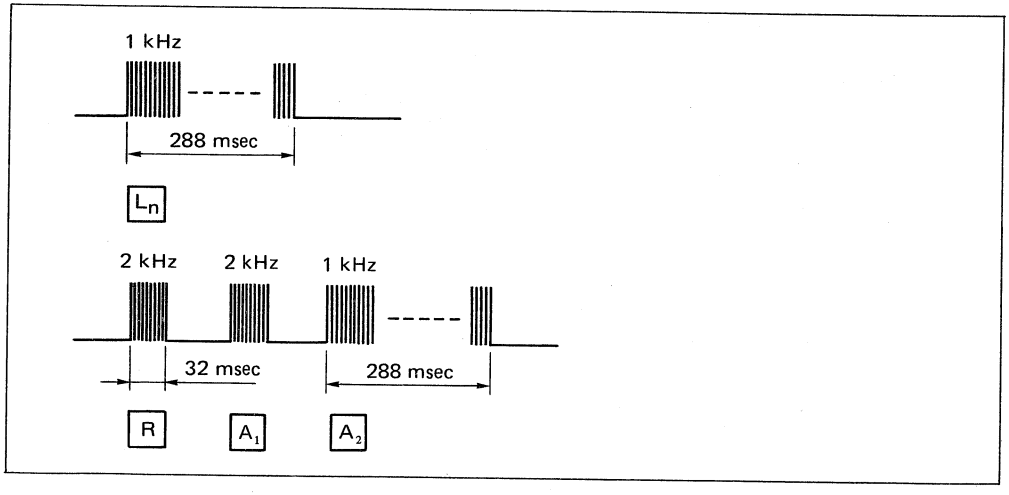
Alarm Sound (b)

It is used when the repertory number using other telephone number's abbreviated code as a part of it is used as a part of newly stored number.



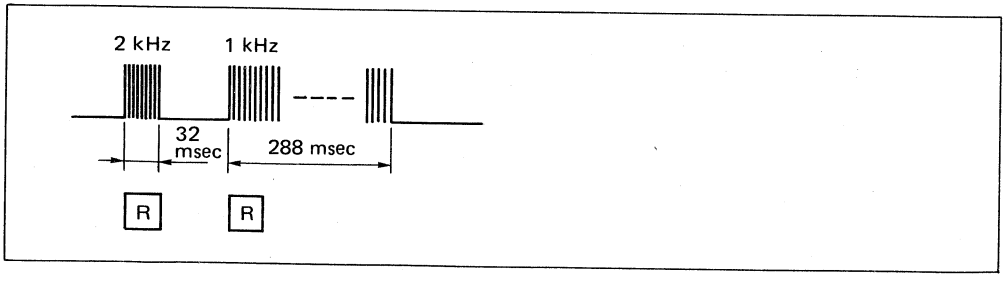
Alarm Sound (c)

It is output when there is no data in the accessed memory address.



Alarm Sound (d)

It is output when redial is prohibited.



ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Condition	Limits	Unit
Supply Voltage	V_{DD}	Ta = 25°C	-0.3 ~ +7.0	V
Input/Output Voltage	V_{IO}	Ta = 25°C	V_{SS}-0.3 ~ V_{DD}+0.3	V
Power Dissipation	P_D	Ta = 25°C	200	mW
Operating Temperature	Topr	—	-20 ~ +75	°C
Storage Temperature	Tstg	—	-55 ~ +125	°C

DC Characteristics

V_{DD} = 3.0 V, V_{SS} = 0 V, f_{OSC} = 3.579545 MHz, T_a = -20 ~ +75°C

Parameter	Symbol	Condition		Min	Typ	Max	Unit
Operating Voltage	V_{DD}			2.5	—	6.0	V
Memory Retention Voltage	V_{DDM}	Standby mode		1.2	—	6.0	V
Current Consumption (1)	I_{DDP}	Pulse Mode, No load		—	300	600	μA
Current Consumption (2)	I_{DDT}	Tone Mode, No load		—	1.2	2.4	mA
Memory Retention Current	I_{DDM}	ON HOOK,	V_{DD} = 2.5 V, Ta = 25°C	—	—	0.2	μA
Output Current	I_{OH1}	$\overline{\text{MUTE}}$, $\overline{\text{XMIT MUTE}}$, DP	V_{OH} = 2.6 V	-200	—	—	μA
	I_{OL1}		V_{OL} = 0.4 V	500	—	—	μA
Output Current	I_{OH2}	C_1 ~ C_4	V_{OH} = 2.6 V	-1	—	—	mA
	I_{OL2}		V_{OL} = 0.4 V	10	—	—	μA
Output Current	I_{OH3}	DP MODE OUT BD	V_{OH} = 2.6 V	-20	—	—	μA
	I_{OL3}		V_{OL} = 0.4 V	10	—	—	μA
Input Current	I_{IH1}	$\overline{\text{HS}}$	V_{IH} = 3.0 V	—	—	2	μA
	I_{IL1}		V_{IL} = 0 V	-20	—	-180	μA
Input Current	I_{IH2}	R_1 ~ R_7	V_{IH} = 3.0 V	10	—	90	μA
	I_{IL2}		V_{IL} = 0 V	—	—	-2	μA
Input Current	I_{IH3}	LSEL, MB, DRS MODE SEL AC, TEST	V_{IH} = 3.0 V	30	—	300	μA
	I_{IL3}		V_{IL} = 0 V	—	—	-2	μA

III

AC Characteristics

f_{OSC} = 3.579545 MHz, 2.5 V ≤ V_{DD} ≤ 6.0 V, T_a = -20 ~ +75°C

Parameter	Symbol	Condition		Min	Typ	Max	Unit
Key Input Time	T_{KIN}			33	—	—	mS
Tone Output	V_{OUT}	ROW side only R_L = 1 KΩ	V_{DD} = 2.5 V	150	250	350	mV rms
			V_{DD} = 4.0 V	200	340	570	
High/Low Level Ratio	dB_{CR}			1.0	2.0	3.0	dB
Distortion	$\%_{Dis}$			—	5	10	%

Tone Output Frequency

f_{OSC} = 3.579545 MHz

Key Input	Nominal Frequency (Hz)	Output Frequency (Hz)	Distortion (%)
R_1	697	699.1	+0.30
R_2	770	766.2	-0.49
R_3	852	847.4	-0.54
R_4	941	948.0	+0.74
C_1	1209	1215.9	+0.57
C_2	1336	1331.7	-0.32
C_3	1477	1471.9	-0.35

Signal Output Timing

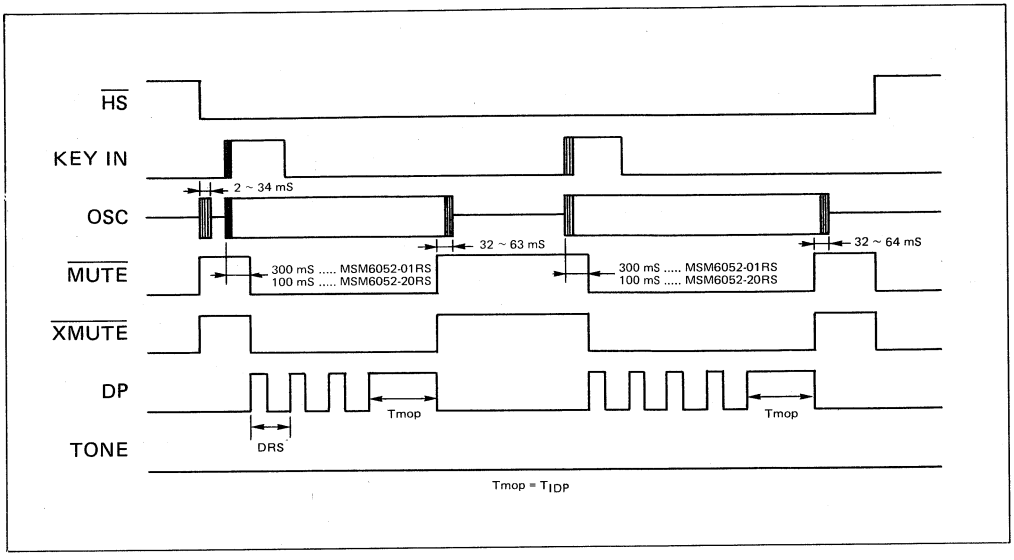
f_{OSC} = 3.579545 MHz

Parameter	Symbol	Condition	Typ	Unit
Tone Output Time	T_{tone}	Tone auto dial	100	mS
Inter Digit Pause	T_{IDP_1}	Tone auto dial	100	mS
	T_{IDP_2}	Pulse auto dial (10 pps)	800	mS
	T_{IDP_3}	Pulse auto dial (20 pps) MSM6052-01RS	450	mS
	T_{IDP_3}	Pulse auto dial (20 pps) MSM6052-20RS	500	mS

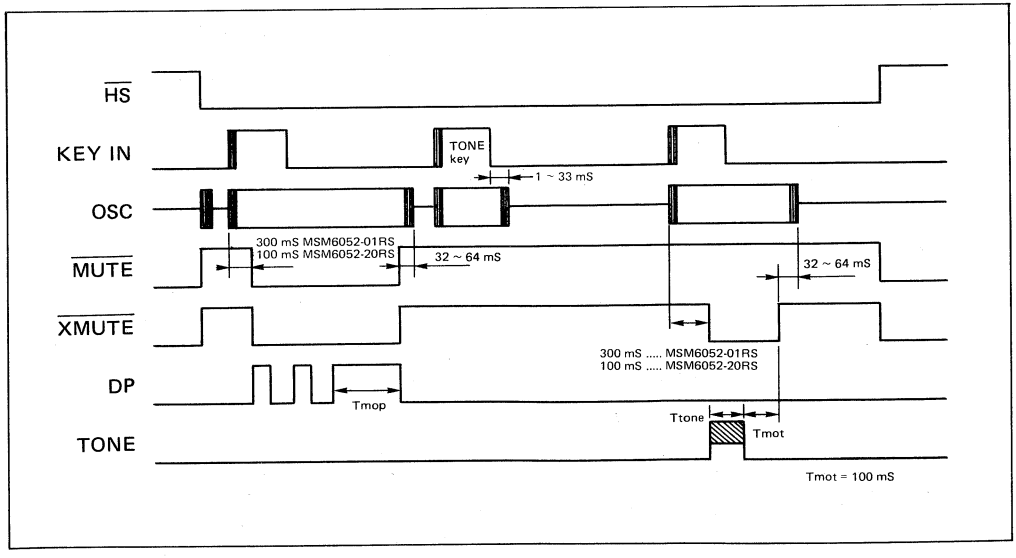
TIMING CHART

DP MODE TIMING CHART

1) Normal dialing

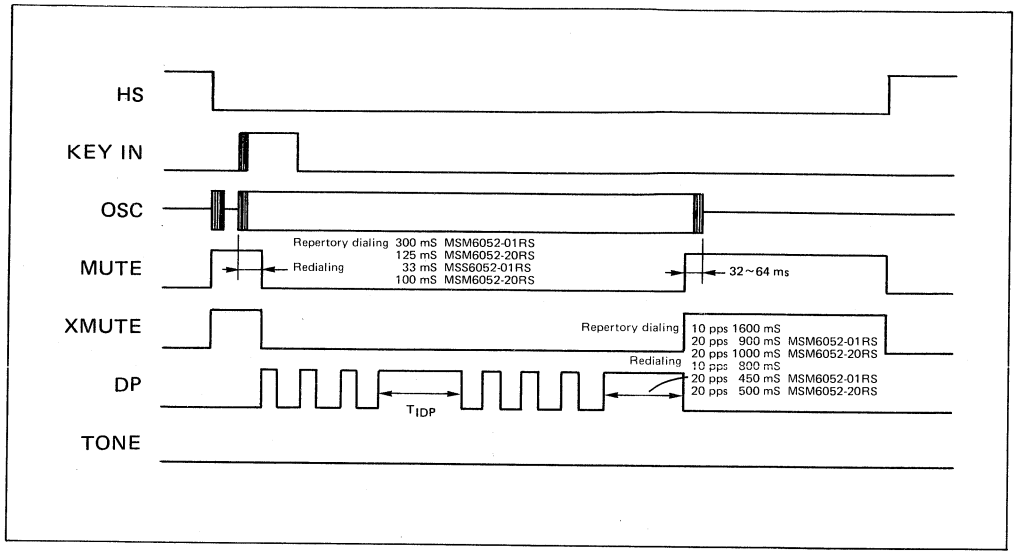


2) Mode change-over by Tone key



III

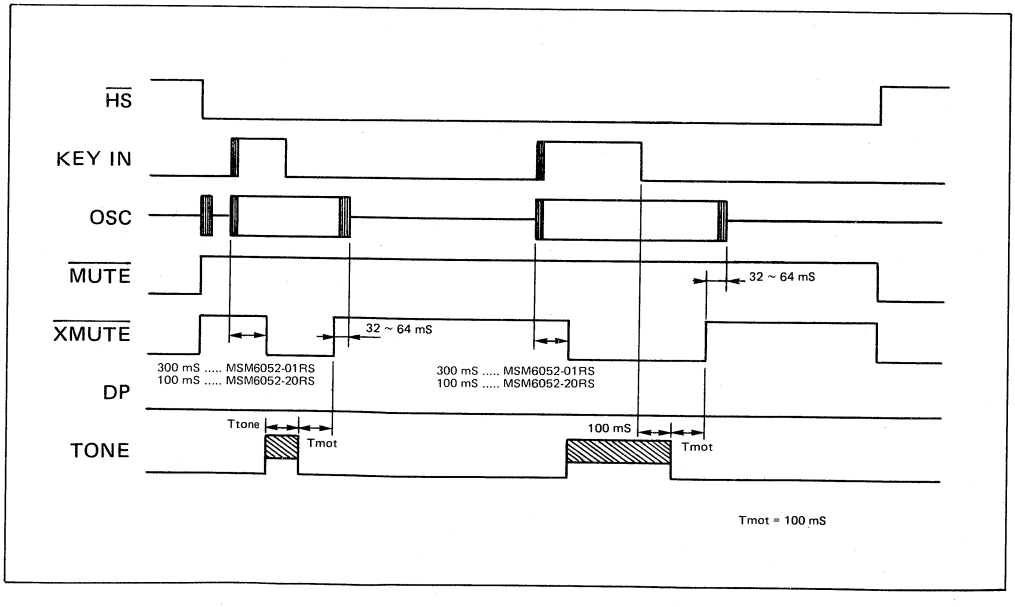
3) Repertory dialing



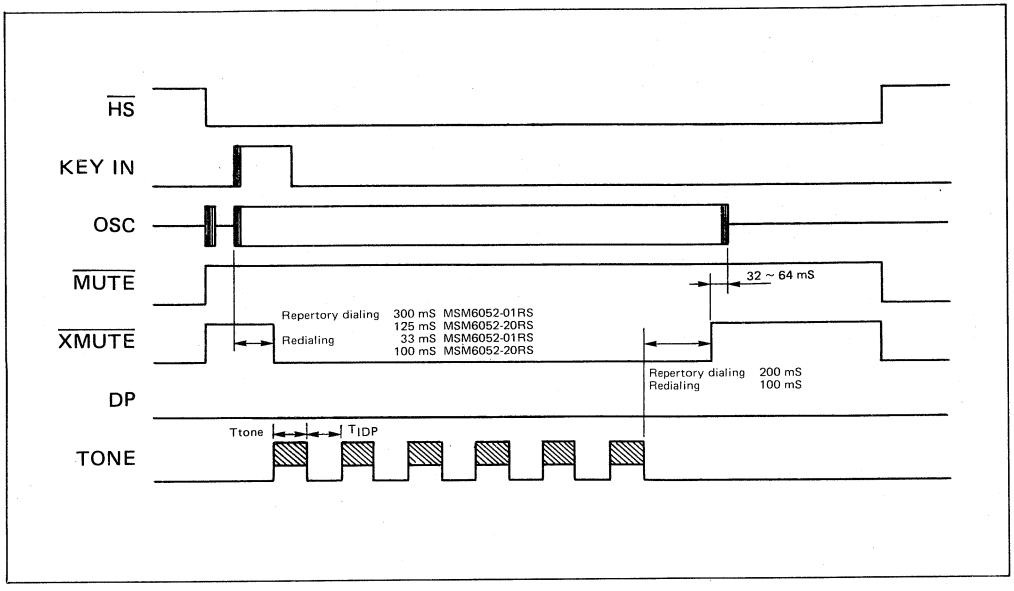
III

DTMF MODE TIMING CHART

1) Normal dialing



2) Repertory dialing, Last number re-dial



III

MSM6052-05GS/10RS/11RS

TONE/PULSE SWITCHABLE REPERTORY DIALER

GENERAL DESCRIPTION

The MSM6052-05GS, MSM6052-10RS and MSM6052-11RS are Tone/Pulse switchable repertory dialer which are fabricated by OKI's low power consumption CMOS silicon gate technology. All of these LSIs can generate either DTMF (Dual Tone Multi Frequency) signal or DP (Dial Pulse) signal.

The repertory memory has a capacity of 500 digits. Maximum 54* telephone numbers of 32 digits maximum per telephone number can be stored in it, so far as the total number of stored digits does not exceed 500 digits.

All of these LSIs operate on 2.5 V ~ 6.0 V single supply voltage. Stand-by current is 0.2 μA maximum and the memory retention voltage is 1.2 V.

FEATURES

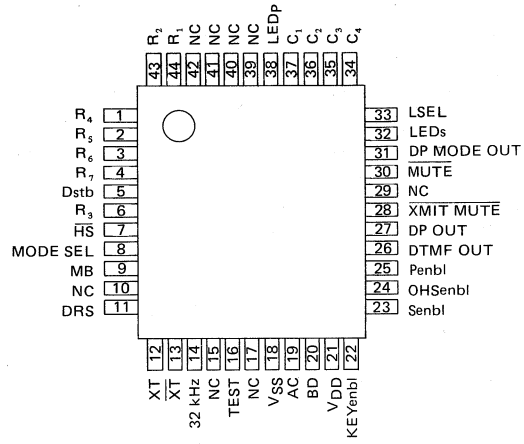
- Either DTMF or DP signal can be generated.
- 500 digits repertory memory (54* numbers maximum, 32 digits maximum/number).
- 24 telephone numbers which can be recalled by single key operation and additional 30* telephone numbers which can be recalled by 2-digits abbreviated code.
- Mixed dialing, Mixed storing (Repertory memory can be stored as a part of another repertory memory).
- Last number redial (32 digits maximum)
- Auto pause 4 sec.
- Pulse rate 10/20 pps pin selectable.
- Make/Break ratio 34/66 or 40/60 pin selectable.
- Alarm output for wrong operations.
- 3.58 MHz for ceramic resonator oscillation circuit on-chip.
- Supply voltage range 2.5 V ~ 6 V.
- Low stand-by current 0.2 μA maximum.

	MSM6052-05GS	MSM6052-10RS	MSM6052-11RS
Memory Storing/ Clearing	Both of On-Hook memory storing/clearing and Off-Hook memory storing/clearing or On-Hook memory storing/clearing only selectable		On-Hook memory storing/clearing only
Keyboard Interface	Matrix keyboard input or 4-bit parallel data input selectable		Matrix keyboard input
Package	44 pin plastic FLAT package	40 pin plastic DIP package	28 pin plastic DIP package

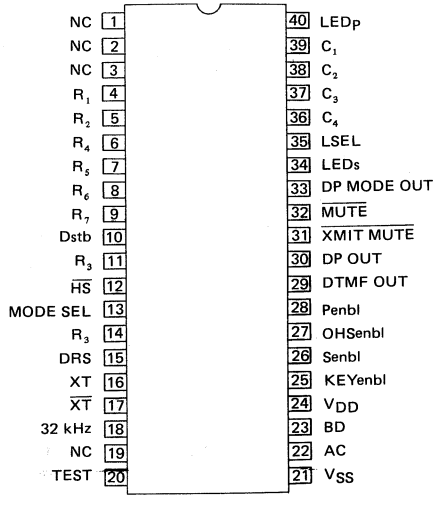
* In case of MSM6052-05GS and MSM6052-10RS, "Senbl" pin has to be set at "H" level to enable 30 numbers stored into 2-digits abbreviated code.

PIN CONFIGURATION

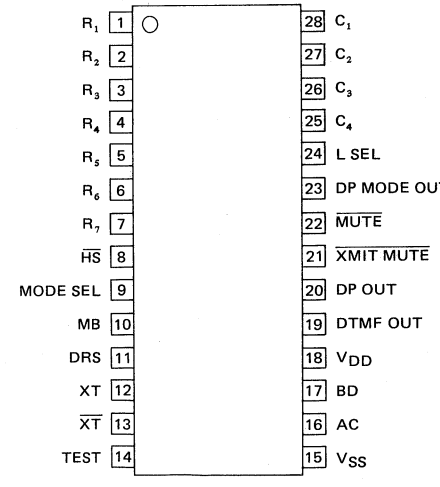
MSM6052-05GS



MSM6052-10RS



MSM6052-11RS

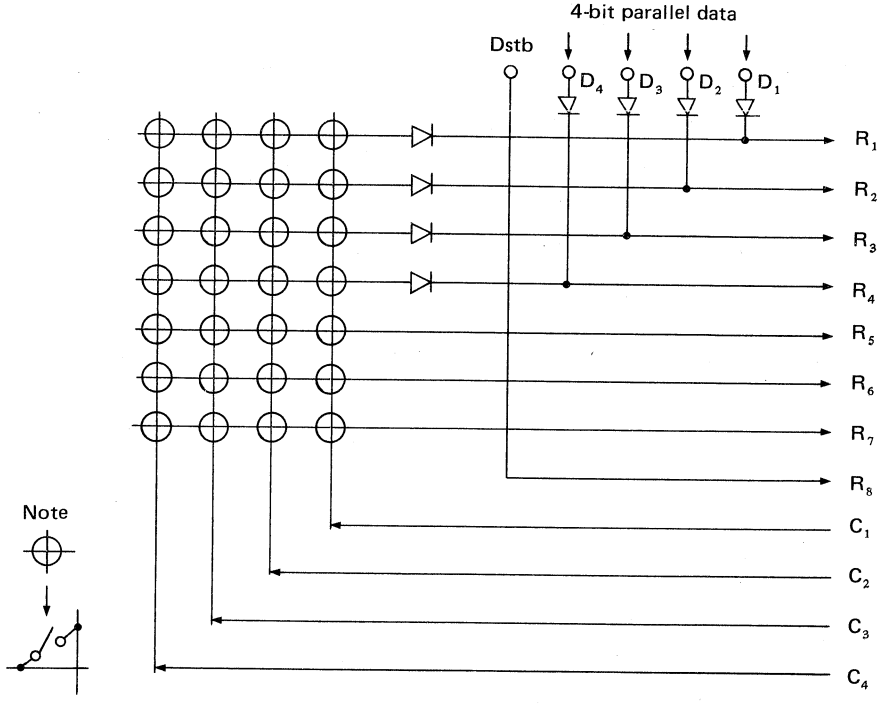


III

KEYBOARD INTERFACE

Both of MSM6052-05GS and MSM6052-10RS have an option to choose either keyboard input or 4-bit parallel data input. This option is selected by the status of KEYenble pin.

As for MSM6052-11RS, data is only input from the keyboard. The interface of MSM6052-05GS and MSM6052-10RS with the keyboard and 4-bit parallel data input is described in the Figure 1, while the interface of MSM6052-11RS with the keyboard is described in the Figure 2.



Either single contact matrix keyboard input or 4-bit parallel data input is selected by the status of KEYenbl pin.
When Keyenbl pin is at "H" level: Single contact keyboard Input.
When KEYenbl pin is at "L" level: 4-bit parallel data input.

Figure 1 MSM6052-05GS, MSM6052-10RS keyboard interface.
(Interface with single contact matrix keyboard and 4-bit parallel data input)

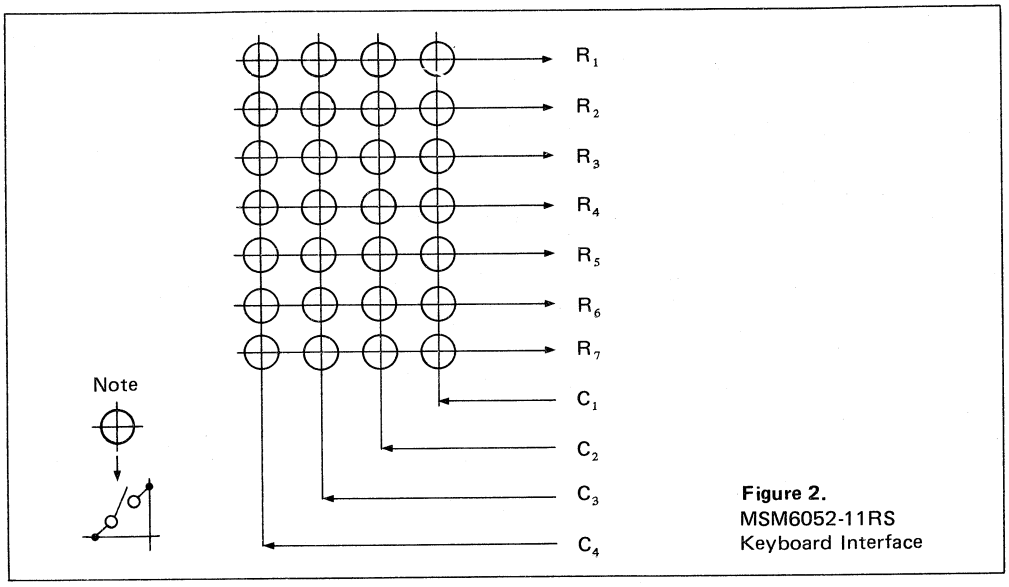
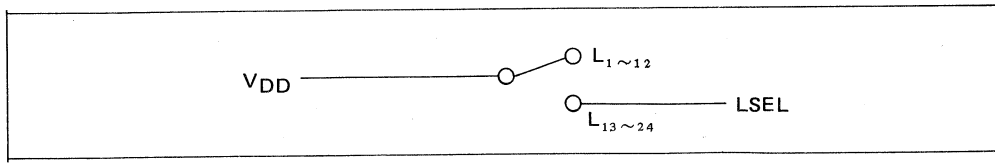


Figure 2.
MSM6052-11RS
Keyboard Interface

Interface with a single contact matrix keyboard

Output pin / Input pin	C1	C2	C3	C4
R1	1	2	3	RECALL
R2	4	5	6	STORE
R3	7	8	9	PAUSE/REDIAL
R4	*	0	#	TONE
R5	L1/L13	L2/L14	L3/L15	L4/L16
R6	L5/L17	L6/L16	L7/L17	L8/L19
R7	L9/L21	L10/L22	L11/L23	L13/L24



A 7 x 4 matrix single contact keyboard shall be used. L1/L13 ~ L12/L24 are single key dialing keys. By connecting or disconnecting LSEL to/from V_{DD}, two telephone numbers can be assigned for each key.

So, the 24 numbers in total can be recalled by single key operation. *In addition to it, maximum 30 numbers can be abbreviated into 2-digit address code (00 ~ 29).

* In this case, Senbl pin of MSM6052-05GS and MSM6052-10RS shall be set to "H" level.

4-bit parallel data input (Only MSM6052-05GS and MSM6052-10RS)

When 4-bit parallel data input is selected by setting KEYenbl pin at "L" level, operation is executed by 4-bit data and strobe signals.

In this case, however, dialing by single key operation cannot be used.

Figure 3 shows an 4-bit parallel data input timing, while Figure 4 shows the 4-bit data and its corresponding data input from the keyboard.

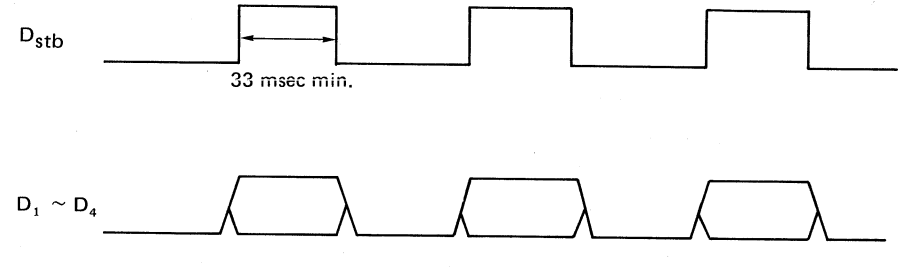


Figure 3 4-bit parallel data input timing

HEX Data	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
KEY Data	STORE	1	2	3	4	5	6	7	8	9	0	*	#	TONE	REDIAL/PAUSE	RECALL

Note: $C_1 \sim C_4$ shall be set at "L" level when OFF-Hooked in the stand-by mode. Oscillation will stop when key input or 4-bit parallel data input is stopped.

Figure 4 4-bit parallel data and its corresponding key data

PIN DESCRIPTION

Pin Name	Pin No.			Function
	–05	–10	–11	
$R_1 \sim R_7$ $C_1 \sim C_4$	1~4, 6, 34~37, 43, 44	4~9, 11, 36~39	1~7, 25~28	Key input pins. As for MSM6052-11RS, $C_1 \sim C_4$ are set to low level in on-hook mode, while they are set to high level in off-hook standby mode. As for MSM6052-05GS and MSM6052-10RS, the $C_1 \sim C_4$ conditions are as follows. Keyboard input: On-hook mode: Low Off-hook stand-by mode: High 4-bit parallel data input: Constantly low
Dstb	5	10	–	(Only MSM6052-GS and MSM6052-10RS) When 4-bit parallel data input is selected, the data strobe signal is input to this pin.
$\overline{HS}$	7	12	8	Hook switch input pin. $\overline{HS}$ = "H" level or open : On-hook $\overline{HS}$ = "L" level : Off-hook
LSEL	33	35	24	Selection pin for single key dialing. LSEL = "L" or open : $L_1 \sim L_{12}$ LSEL = "H" : $L_{13} \sim L_{24}$
MB	9	14	10	Make/Break ratio selection pin. MB = "L" or open : 40/60% MB = "H" : 34/66% Note: This input is sensed in the transition stage from On-hook to Off-hook.
DRS	11	15	11	Dial rate selection pin. DRS = "L" or open : 10 pps DRS = "H" : 20 pps Note: This input is sensed in the transition stage from On-hook to Off-hook.
MODE SEL	8	13	9	DTMF/DP mode selection pin. MODE SEL = "L" or open : DP mode MODE SEL = "H" : DTMF mode If [TONE] key is pressed in the DP mode, the DFMF mode is established. Note: This input is sensed in the transition stage from On-hook to Off-hook.
DTMF OUT	26	29	19	DTMF output pin.

III

Pin Name	Pin No.			Function
	–05	–10	–11	
DP OUT	27	30	20	Dial pulse output pin. This pin is at "H" level for "Make", and at "L" level for "Break". A "L" level output is also obtained when $\overline{HS}$ = "H" or open (On-hook).
$\overline{XMIT\ MUTE}$	28	31	21	Transmitter mute output pin. When $\overline{HS}$ = "H" or open (On-hook) : $\overline{XMIT\ MUTE}$ = "L" When $\overline{HS}$ = "L" (Off-hook) i. While DP signal or DTMF signal is being output : $\overline{XMIT\ MUTE}$ = "L" ii. All other times : $\overline{XMIT\ MUTE}$ = "H"
$\overline{MUTE}$	30	32	22	Mute output pin. When $\overline{HS}$ = "H" or open (On-hook) : $\overline{MUTE}$ = "L" When $\overline{HS}$ = "L" (Off-hook) i. While DP signal is being output : $\overline{MUTE}$ = "L" ii. All other times : $\overline{MUTE}$ = "H"
DP MODE OUT	31	33	23	Dial pulse mode output pin. When $\overline{HS}$ status is changed from "H" or (On-hook) to "L" (Off-hook), either "H" level or "L" level signal is output from this pin by following conditions. MODE SEL = "L" : DP MODE OUT = "H" level output MODE SEL = "L" level output DP MODE OUT = "L" level output A "L" level signal is output from DP MODE OUT pin even when MODE SEL = "L" and $\overline{HS}$ = "L", if [TONE] key is pressed.
XT, $\overline{XT}$	12, 13	16, 17	12, 13	Ceramic resonator connection pin. Since MSM6052 is provided with an on-chip oscillation inverter and feed-back resistor, a 3.58 MHz ceramic resonator and capacitors are to be connected to XT and $\overline{XT}$.
AC	19	22	16	Internal initialization pin. When this IC is powered on, a reset signal ("H" level). has to be applid to this pin.
V_{DD}, V_{SS}	18, 21	21, 24	15, 18	V_{DD} : Positive power supply pin (2.5 V ~ 6.0 V) V_{SS} : Negative power supply pin (Ground)
TEST	16	20	14	Test pin. This pin should be left open.
BD	20	23	17	Buzzer output pin.

III

Pin Name	Pin No.			Function
	–05	–10	–11	
KEYenbl	22	25	–	(Only MSM6052-05GS and MSM6052-10RS) Either matrix keyboard input or 4-bit parallel data input is selected according to the status of this pin. KEYenbl = "H" : matrix keyboard input operation. KEYenbl = "L" : 4-bit parallel data input
OHSenbl	24	27	–	(Only MSM6052-05GS and MSM6052-10RS) Memory storage method is determined by the status of this pin. OHSenbl = "H" : Both of On-hook memory storing and Off-hook memory storing are possible. OSHenbl = "L" : Only On-hook memory storing is possible.
Senbl	23	26	–	(Only MSM6052-05GS and MSM6052-10RS) Memory storing into 2-digits abbreviated code is enabled/disabled by the status of this pin. Senbl = "H" : Memory storage into 2-digits abbreviated code is enabled. Senbl = "L" : Memory storage into 2-digits abbreviated code is disabled.
Penbl	25	28	–	(Only MSM6052-05GS and MSM6052-10RS) Manual pause cancel function is enabled/disabled by the status of this pin. Penbl = "H" : Manual pause cancel function is enabled. Penbl = "L" : Manual pause cancel function is disabled. When manual pause cancel function is disabled, [PAUSE] key is only used to establish the pause.
LEDs	32	34	–	(Only MSM6052-05GS and MSM6052-10RS) A "H" level signal is output during the memory store/clear operation. All other times, a "L" level signal is output.
LEDp	38	40	–	(Only MSM6052-GS and MSM6052-10RS) A "H" level signal is output when a pause is established, while a "L" level signal is output at all other times.
32 kHz	14	18	–	(Only MSM6052-056S and MSM6052-10RS) Output terminal of 32 kHz lock.

III

FUNCTIONAL DESCRIPTION

Dialing Function

(1) Normal Dialing

Off-Hook [D_1] [D_2] [D_3] ----- [D_n]

([D_n] designates for [0] ~ [9], [✳], [#], [P/R] or [TONE] keys)

* [P/R] : [PAUSE/REDIAL]

The maximum number of digits which can be dialed out at a time in the DP mode is 32 digits. Any additional digit is dialed out only after the first 32 digits are dialed out.

Before the first 32-digits are dialed out, any key input from the keyboard is inhibited.

If more than 32-digits are dialed out either in DTMF or DP mode, redialing of that number is disabled.

Note: In the DP mode, [✳] and [#] key inputs are invalid.

(2) Redialing

Off-Hook [P/R]

When [P/R] key is firstly pressed once after the telephone is On-hooked, the last dialed-out telephone number is dialed out.

[P/R] : [PAUSE/REDIAL]

If the redial function is inhibited, an alarm tone is generated and normal dialing can be executed after that.

III

(3) Repertory Dialing

Off-Hook [R] [A_1] [A_2] ------- 2-digits abbreviated code dialing

or

Off-Hook [L_n] ------- Single key dialing

[R] : [RECALL]

[L_n] : [L_1/L_{12}] ~ [L_{13}/L_{24}]

[A_1] : [0], [1], [2]

[A_2] : [0] ~ [9]

In case of 2-digits abbreviated code dialing, an alarm tone is generated if any key other than [0] [1] or [2] key is pressed after [R] key.

In this case, however, if [R] key is pressed again after the alarm tone and 2-digits abbreviated code is addressed after [R] key, the memory contents of that 2-digits abbreviated code will be dialed out. In this case, if any key other than [R] key is firstly pressed after the alarm tone, an alarm tone will be generated again.

An alarm tone is also generated if the specified repertory memory has no contents, or if anotehr repertory has been specified within the selected repertory.

(4) Mixed Dialing

Off-Hook [P/R] [D_1] ----- [D_n] [R] [A_1] [A_2] [L_n]

↑ Redial — Normal dialing — 2-digits abbreviated code dialing — ↑ Single key dialing

Consecutive dialing of redialing, normal dialing, 2-digits abbreviated code dialing and single key dialing is possible. In case of mixed dialing, however, redialing of the last dialed number can be executed only once and it must come to the first part of the mixed dialing.

If the digits of the mixed dialed number do not exceed 32, that mixed dialed number can be redialed. (In this case, both of 2-digits abbreviated code memory contents and single key memory contents are counted as 3-digits. The digits of the redialing, however, depends on the contents of the redialing.)

(5) Pause

When the [PAUSE] key is pressed, transmission of DTMF/DP signal will temporarily be suspended after that digit. This pause is automatically released 4 seconds later. In addition to this automatic pause releasing, manual pause cancelling by pressing the [PAUSE] key during the 4-seconds pause is available for MSM6052-11RS. As for MSM6052-05GS and MSM6052-10RS, this manual pause cancelling function is enabled/disabled by the status of Penbl pin. (Refer to the Note below.)

By this manual pause canceling function by pressing [PAUSE] key during the 4-seconds pause, multi digits pause can also be cancelled by a single pause cancel operation.

Note: As for MSM6052-05GS and MSM6052-10RS, the status of Penbl pin enables/disables the manual pause cancel function.

Penbl = "H" : Pause can be manually cancelled by pressing [PAUSE] key.

Penbl = "L" : Pause cannot be cancelled manually.

(6) Switching to DTMF mode

When [TONE] key is pressed in the DP mode, the mode is switched to DTMF mode from that digit.

When [TONE] key is pressed during the DP signal is being transmitted out, a pause will automatically be inserted after the transmission of DP signal has been completed. DTMF mode is established and signals are transmitted after this pause has been released.

This pause can also be cancelled manually. (Refer to (5) Pause.)

(7) Key input confirmation tone

As for MSM6052-11RS, an operation confirmation tone is generated for the input by [0] ~ [9], [RECALL], [STORE], [PAUSE/REDIAL] and [TONE] keys in the DP mode and input by [RECALL], [STORE], [PAUSE/REDIAL] and [TONE] keys in the DTMF mode.

As for MSM6052-05GS and MSM6052-10RS, no operation confirmation tone is generated for the input by these keys. An operation confirmation tone, however, will be generated for memory storing/clearing operation.

Memory Storing/Clearing Function

As for MSM6052-05GS and MSM6052-10RS, two different types of memory storing/clearing operations are available and these are determined by the status of OHSenbl pin.

As for MSM6052-11RS, only On-Hook memory storing/clearing is available.

MSM6052-05GS	MSM6052-10RS	MSM6052-11RS
OHSenbl pin = "H" level:	Memory storing/clearing is possible both in On-Hook and *Off-Hook condition	Only On-Hook condition
OHSenbl pin = "L" level:	Only On-Hook condition	

Memory storing/clearing operation condition

* When Off-Hook memory storing/clearing is available, memory storing/clearing operation can be done even after the dialing operation.

Memory storing/clearing operation is commenced by pressing [STORE] key and is stopped when any of following conditons is established.

i. When the memory storing/clearing operation has completed.
ii. When the interval between any two key inputs exceeds 20 seconds.
iii. When the number of digits exceeds 32.
iv. When total number of digits stored in the memory exceeds 500.

An alarm tone is generated for above iii. and iv.

A key input confirmation tone is generated for all key inputs.

III

(1) Storing of telephone number

Memory storing operation can be done by following operations.

[S] [D_1] [D_2] ----- [D_n] [S] [A_1] [A_2] ----- Store into 2-digits abbreviated code address

[S] [D_1] [D_2] ----- [D_n] [S] [L_n] ----- Store into single key address

[S] : [STORE]

In case of storing telephone number into 2-digits abbreviated code address, [A_1] shall be any of [0], [1] or [2] and [A_2] shall be any of [0] ~ [9]. For any input other than these keys, an alarm tone is generated.

In this case, however, by pressing [STORE] key again enables to select the 2-digits abbreviated code address again.

If any key other than [STORE] key is pressed, an alarm tone is generated.

If the empty space of the repertory memory is less than 16 digits, an alarm tone is generated at the first [STORE] key input. In other words, if an alarm is not generated at the first [STORE] key input, minimum 16 digits can be newly stored.

An alarm tone is generated at the 500th digit input showing the memory has no more capacity. That 500th input digit can be stored in the memory, however. if the 501st digit is input, an alarm tone is generated again and memory storing operation is cancelled.

Maximum digits of a telephone number to be stored is 32. [TONE] key input and pause information by [PAUSE/REDIAL] key input are counted as one digit respectively.

If the 33rd digit is input, an alarm sound is generated and memory storing operation is cancelled.

24 telephone numbers can be abbreviated to single key dialing address, which are [L_1] ~ [L_{24}] . Other than those single key dialing address, maximum 30 telephone numbers can be abbreviated to *2-digit address codes, which are [00] ~ [29] , so far as total stored digits in the repertory memory do not exceed 500.

* In this case, Senbl pin of MSM6052-05GS and MSM6052-10RS has to be set to "H" level.

(2) Mixed Storing

[S] [P/R] [D_1] [D_2] ----- [D_n] [R] [A_1] [A_2] [L_n] [S] [A'_1] [A'_2]

----- Store into 2-digits abbreviated code address

[S] [P/R] [D_1] [D_2] ----- [D_n] [R] [A_1] [A_2] [L_n] [S] [L_m]

----- Store into single key address

[P/R]	:	Last dialed telephone number
[D_1] ~ [D_n]	:	Normal dial
[R] [A_1] [A_2]	:	Already stored telephone number
[L_n]	:	Already stored telephone number
[A'_1] [A'_2]	:	Newly stored address
[L_m]	:	Newly stored address

The telephone number once stored in the repertory memory can be used as a part of the newly stored telephone number in the form of abbreviated code. The last dialed telephone number can also be used as a part of newly stored telephone number, but in this case the last dialed telephone number should come to the first part of the newly stored telephone number. Otherewise, input by [PAUSE/REDIAL] key is regarded as a pause information.

Maximum 32 digits can be mixed stored. Either [L_n] or [RECALL] [A_1] [A_2] is counted as 3 digits, while number of the digit of the last dialed out telephone number depends on the contents of redialing.

If [L_n] key or [RECALL] key is pressed at the 31st or 32nd digit, an alarm sound is generated and storing is disabled.

Abbreviated code used for the newly stored number must not include abbreviated code of the other telephone number.

III

(3) Clearing of telephone number

[S] [S] [A_1] [A_2] ----- Clear the 2-digits abbreviated code address

[S] [S] [L_n] ----- Clear the single key address

Pressing [STORE] key twice followed by [L_n] or [A_1] [A_2] clears the stored number in that address.

(4) Redial Inhibition

Redialing is disabled by one of following conditions has been established.

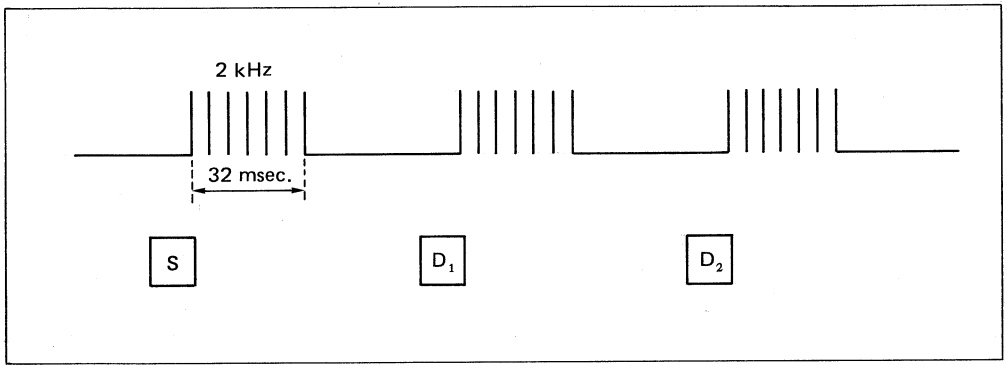
i. When more than 32 digits are dialed out in a single dialing operation.
ii. In the memory storing/clearing operation, [STORE] is pressed followed by any valid key input.
iii. When the telephone is On-hooked, [PAUSE/REDIAL] key is pressed twice prior to any key.

BUZZER OUTPUT WAVEFORM

Key Input Confirmation Tone

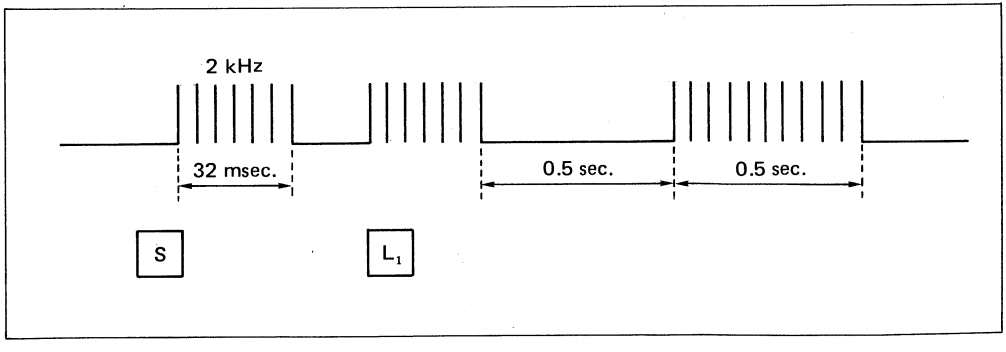
It is output for the following key input.

Operation	MSM6052-05GS	MSM6052-10RS	MSM6052-11RS	
Normal operation	–		DP mode	[0] ~ [9], All Function keys
			DTMF mode	All Function keys
Memory storing/ Clearing operation	Valid key inputs		Valid key inputs	



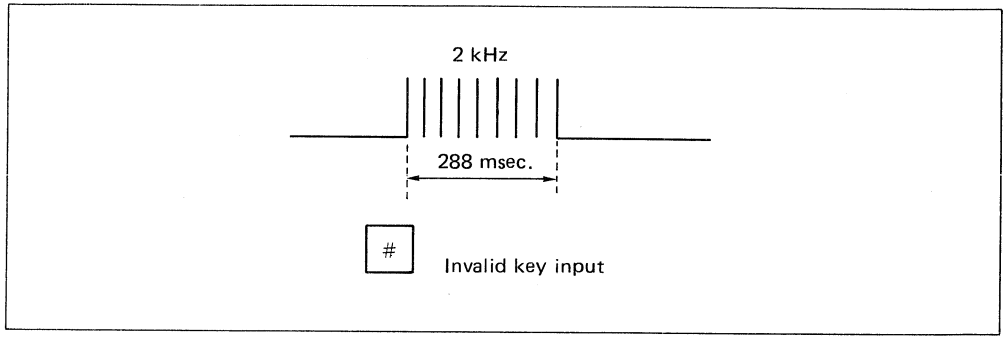
Memory Storing/Clearing Confirmation Tone

It is output when storing/clearing of telephone number has been completed.

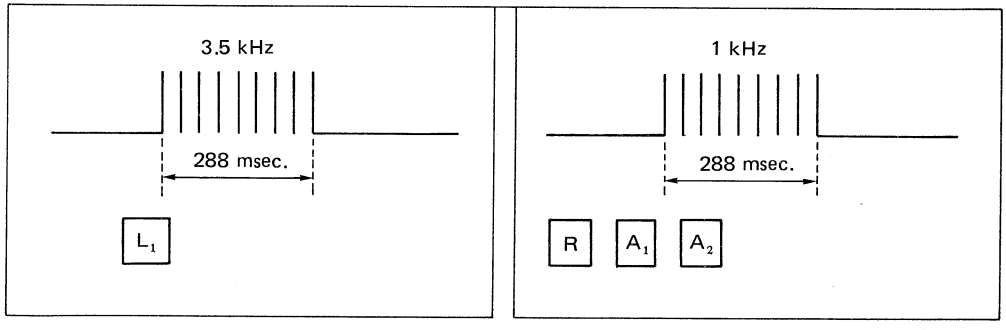


Alarm Sound

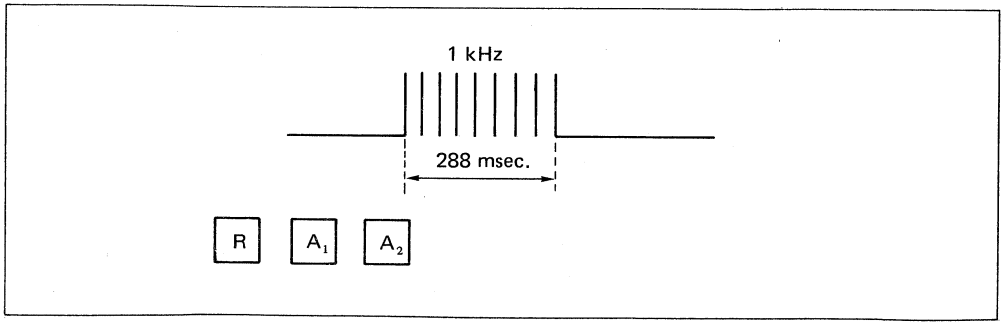
i. It is output for the followings.
- Wrong key input
- 33rd digit input for storing
- [STORE] key input when the empty capacity of repertory memory is less than 16 digits



ii. It is output when the repertory number, using other telephone number's abbreviated code as a part of it, is used as a part of newly stored number.



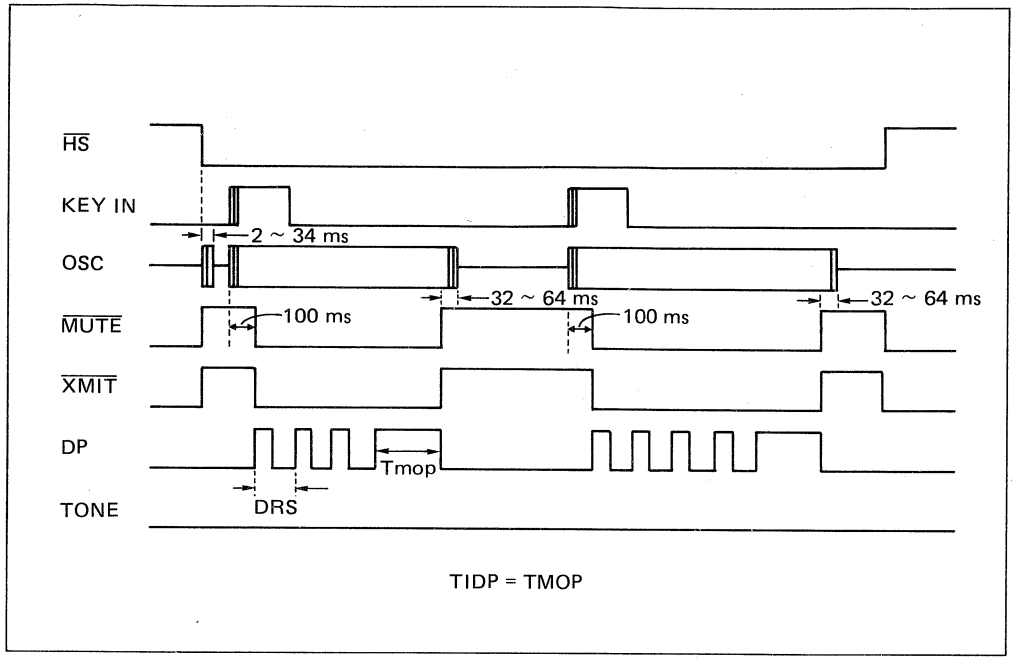
iii. It is output when there is no data in the accessed memory address. It is also output when redial is prohibited.



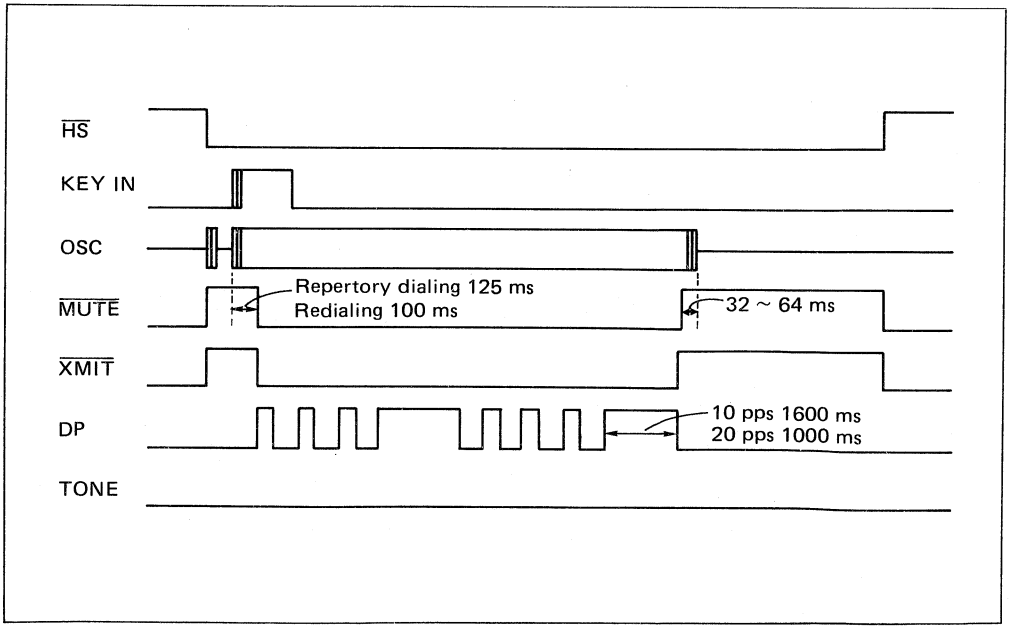
TIMING CHART

DP mode Timing chart

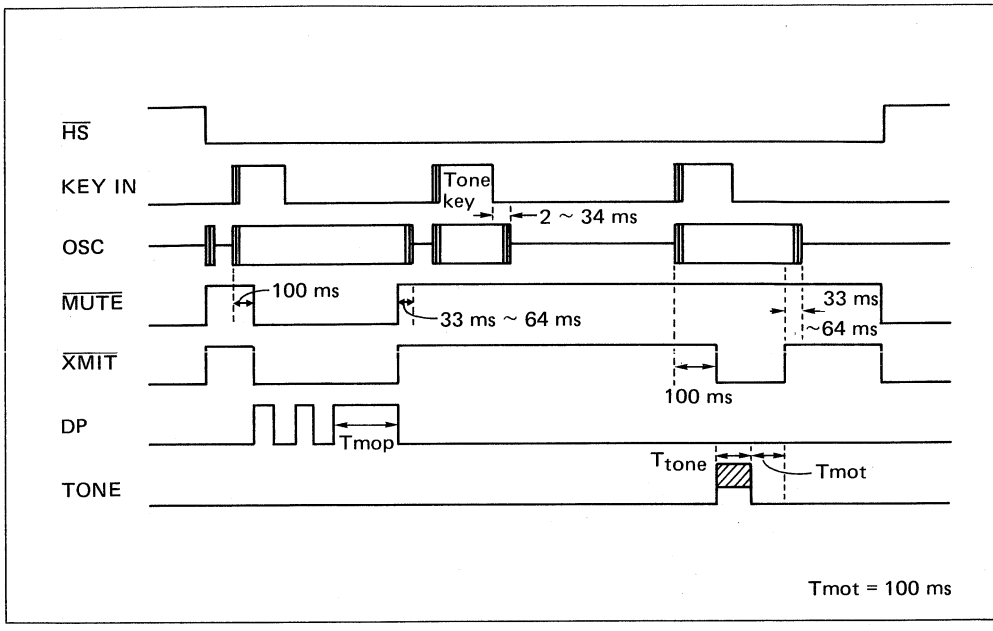
1) Normal dialing



2) Repertory dialing

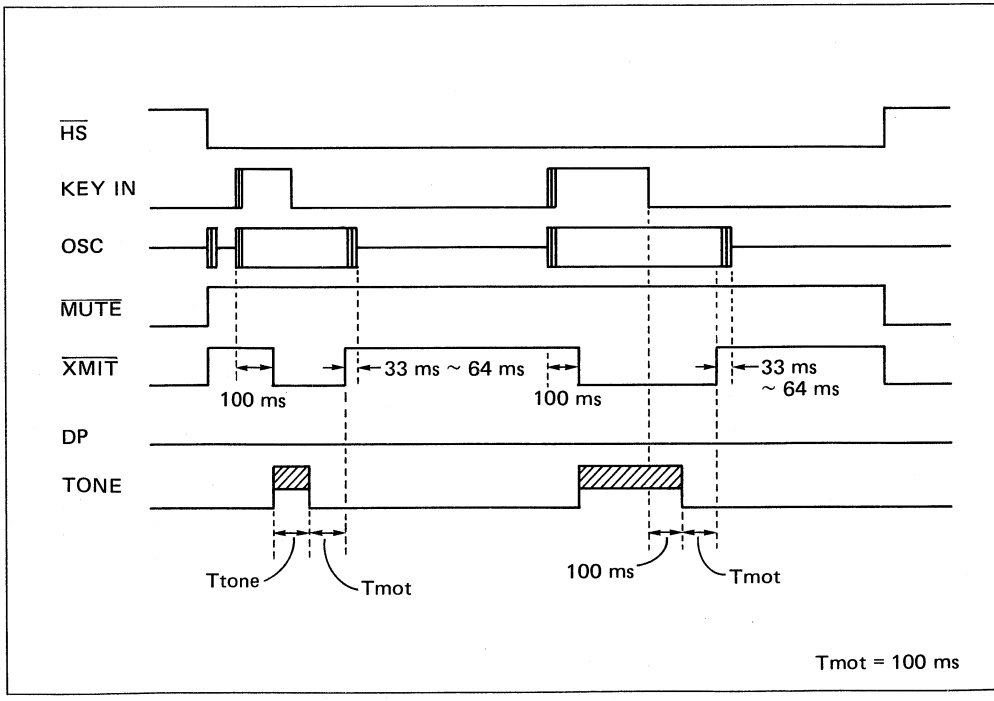


3) Mode change-over by TONE key

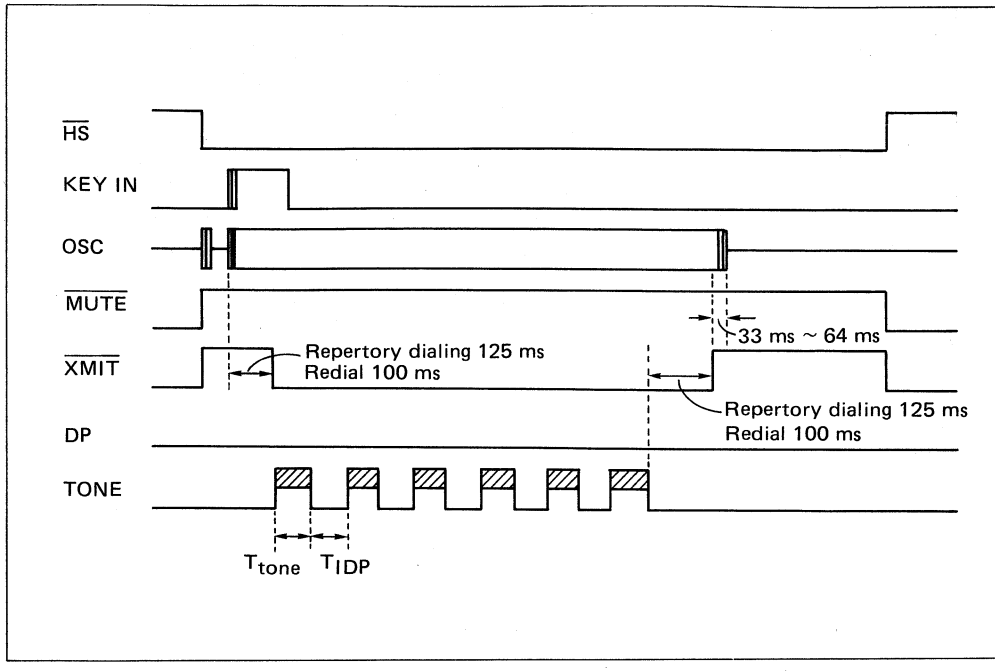


DTMF mode timing chart

1) Normal dialing



2) Repertory dialing, Redialing



Signal output timing

Parameter	Symbol	Condition	Typical	Unit
Tone Output Time	T tone	Tone auto-dial	100	ms
Inter Digit Pause	TIDP 1	Tone auto-dial	100	ms
	TIDP 2	Pulse auto-dial (10 pps)	800	ms
	TIDP 3	Pulse auto-dial (20 pps)	500	ms

fosc = 3.579545 MHz

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Ratings	Unit
Power Supply Voltage	V_{DD}	Ta = 25°C	−0.3 ~ 7	V
Input Voltage	V_I	Ta = 25°C	−0.3 ~ V_{DD} +0.3	V
Output Voltage	V_O	Ta = 25°C	−0.3 ~ V_{DD} +0.3	V
Power Dissipation	P_D	Ta = 25°C	200 max	mW
Storage Temperature	T_{stg}	—	−55 ~ +125	°C

Operating Ranges

Parameter	Symbol	Conditions	Ratings	Unit
Power Supply Voltage	V_{DD}	f_{osc} = 3.58 MHz	2.5 ~ 6	V
Memory Retention Voltage	V_{DDM}	—	1.2 ~ 6	V
Operating Temperature	T_{OP}	—	−20 ~ 75	°C

DC Characteristics

V_{DD} = 3.0 V, V_{SS} = 0 V, f_{OSC} = 3.579545 MHz, Ta = -20 ~ +75°C

Parameter	Symbol	Conditions		V_{DD}	Min	Typ	Max	Unit
"H" output current (1)	I_{OH1}	$\overline{\text{MUTE}}$ / XMIT MUTE / DP OUT	V_{OH} = 2.6 V	3.0 V	−0.2	—	—	mA
"L" output current (1)	I_{OL1}		V_{OL} = 0.4 V	3.0 V	0.5	—	—	mA
"H" output current (2)	I_{OH2}	$C_1 \sim C_4$	V_{OH} = 2.6 V	3.0 V	−1.0	—	—	mA
"L" output current (2)	I_{OL2}		V_{OL} = 0.4 V	3.0 V	10	—	—	μA
"H" output current (3)	I_{OL3}	DP MODE OUT / LEDs / BD	V_{OH} = 2.6 V	3.0 V	−20	—	—	μA
"L" output current (3)	I_{OL3}		V_{OL} = 0.4 V	3.0 V	10	—	—	μA
"H" output current (4)	I_{OH4}	LEDp	V_{OH} = 2.6 V	3.0 V	−150	—	—	μA
"L" output current (4)	I_{OL4}		V_{OL} = 0.4 V	3.0 V	300	—	—	μA
"H" output current (5)	I_{OH5}	32 KHz	V_{OH} = 2.5 V	3.0 V	−40	—	—	μA
"L" output current (5)	I_{OH5}		V_{OL} = 0.4 V	3.0 V	25	—	—	μA
"H" input voltage	V_{IH}	—		3.0 V	2.2	—	—	V
				6.0 V	4.4	—	—	
"L" input voltage	V_{IL}	—		3.0 V	—	—	0.8	V
				6.0 V	—	—	1.6	

Parameter	Symbol	Conditions		V_{DD}	Min	Typ	Max	Unit
"H" input current (1)	I_{IH_1}	$\overline{HS}$	V_{IH} = 6.0 V	6.0 V	–	–	2	μA
"L" input current (1)	I_{IL_1}		V_{IL} = 0 V	3.0 V	–20	–	–180	μA
				6.0 V	–40	–	–360	
"H" input current (2)	I_{IH_2}	$R_1 \sim R_8$	V_{IH} = 6.0 V	6.0 V	20	–	180	μA
			V_{IH} = 3.0 V	3.0 V	10	–	90	
"L" input current (2)	I_{IL_2}		V_{IL} = 0 V	6.0 V	–	–	–2	μA
"H" input current (3)	I_{IH_3}	MB DRS LSEL MODESEL AC TEST	V_{IH} = 6.0 V	6.0 V	60	–	600	μA
			V_{IH} = 3.0 V	3.0 V	30	–	300	
"L" input current (3)	I_{IL_3}		V_{IL} = 0 V	6.0 V	–	–	–2	μA
"H" input current (4)	I_{IH_4}	KEYenbl Senbl OHSenbl Penbl	V_{IH} = 6.0 V	6.0 V	–	–	2	μA
"L" input current (4)	I_{IL_4}		V_{IL} = 0 V	6.0 V	–	–	–2	μA
Power supply current (1)	I_{DDP}	Pulse mode, No load		3.0 V	–	0.3	0.6	mA
				6.0 V	–	1.2	2.4	
Power supply current (2)	I_{DDT}	Tone mode, No load		3.0 V	–	1.2	2.4	mA
				6.0 V	–	3.5	7.0	
Power supply current (3)	I_{DDM}	When on-hook mode No load (Ta = 25°C)		2.5 V	–	–	0.2	μA

AC Characteristics

f_{OSC} = 3.579545 MHz, 2.5 V ≤ V_{DD} ≤ 6.0 V, Ta = –20 ~ +75°C

Parameter	Symbol	Conditions	V_{DD}	Min	Typ	Max	Unit
Cycle time	t_{CY}	f = 3.579545 MHz	3.0 V	–	17.9	–	μs
Tone output	V_{OUT}	For row only R_L = 1 kΩ	2.5 V	–	250	–	mV rms
			4.0 V	–	350	–	
			6.0 V	–	480	–	
High/low level ratio	dB_{CR}	–	3.0 V	1	2	3	dB
			6.0 V	1	2	3	
Distortion	% dis	R_L = 1 kΩ	3.0 V	–	1	5	%
			6.0 V	–	1	5	
Switch input time	T_{KIN}	–	–	33	–	–	ms

III

DTMF Tone Output Frequency

	Nominal frequency (Hz)	Output frequency (Hz)	Distortion (%)
R_1	697	699.1	+0.30
R_2	770	766.2	-0.49
R_3	852	847.4	-0.54
R_4	941	948.0	+0.74
C_1	1209	1215.9	+0.57
C_2	1336	1331.7	-0.32
C_3	1477	1471.9	-0.35

f_{OSC} = 3.579545 MHz

OKI semiconductor

MSM6052-25RS

TONE/PULSE SWITCHABLE REPERTORY DIALER

GENERAL DESCRIPTION

The MSM6052-25RS is a repertory tone/pulse switchable dialer which is fabricated by OKI's low power consumption CMOS silicon gate technology. This LSI can generate either DTMF (Dual Tone Multi Frequency) signal or DP (Dial Pulse) signal.

The repertory memory has a capacity of 505 digits. Maximum 52 telephone numbers of 32 digits maximum/number can be stored in it, so far as total number of stored digits does not exceed 505.

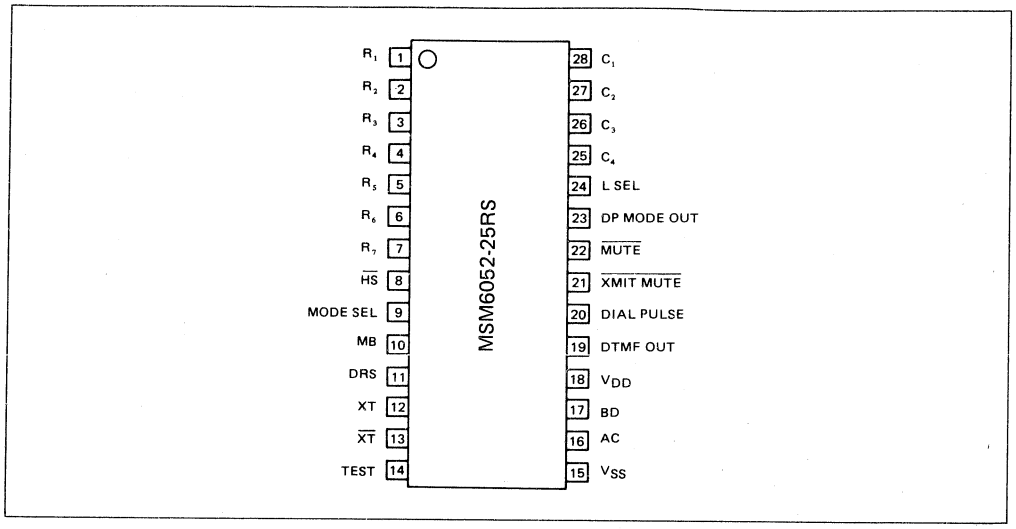
It operates on 2.5 V ~ 6 V single supply. Standby current is 0.2 μA maximum (V_{DD} = 2.5 V Ta = 25°C) and memory retention voltage is 1.2 V.

FEATURES

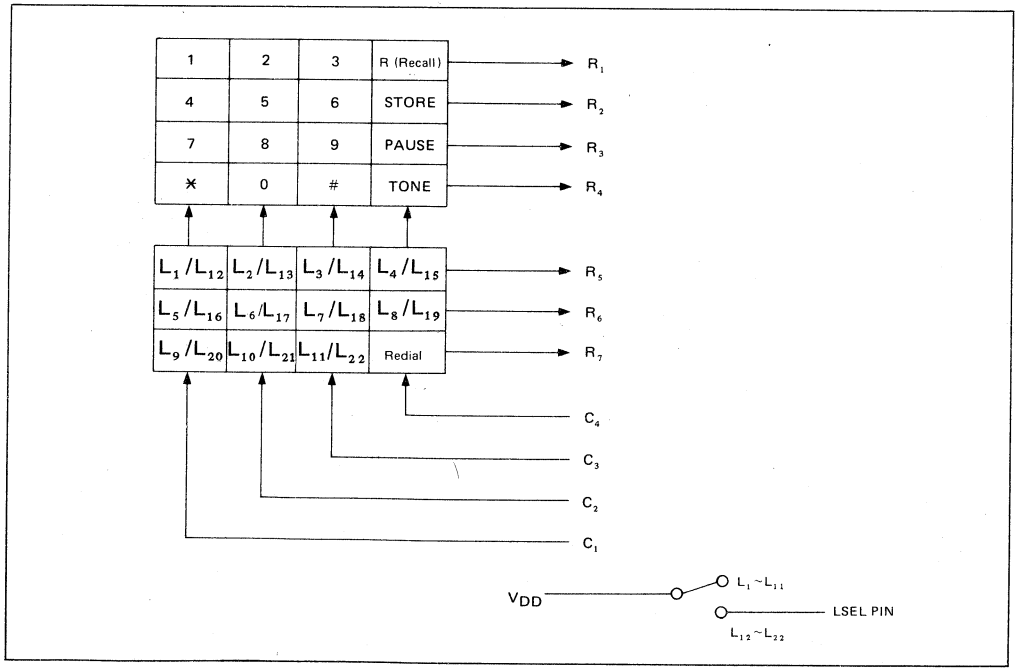
- Either DTMF signal or DP signal generation.
- DP/TONE output starts 100 msec after keying in normal dialing
- 505 digits repertory memory. (52 numbers maximum, 32 digits maximum/number).
- 22 numbers repertory dialing by single key dialing plus maximum 30 numbers repertory dialing by 2-digit abbreviated code dialing.
- Last number redial (32 digits maximum).
- Mixed dialing/storing.
- Auto insersion of 4 seconds access pause.
- Pulse rate 10/20 pps pin selectable.
- Make/Break ratio 34/66 or 40/60 pin selectable.
- Tone output for valid key input (2 kHz, 32 msec).
- Alarm tone for wrong operations.
- Single contact matrix keyboard to be used.
- 3.58 MHz oscillation circuit on chip for ceramic resonator.
- Supply voltage range 2.5 V ~ 6 V.
- Low standby current 0.2 μA maximum. (V_{DD} = 2.5 V, Ta = 25°C)
- 28-pin plastic DIP Package.

III

PIN CONFIGURATION



KEYBOARD INTERFACE



A 7 x 4 single contact keyboard shall be used. L_1/L_{12}~L_{11}/L_{22} are one touch memory recall keys. By connecting or disconnecting LSEL to/from V_{DD}, two telephone numbers can be assigned for each key. So, the 22 numbers in total can be recalled by single key operation.

In addition to it, maximum 30 numbers can be abbreviated into 2-digit address code (00 ~ 29).

PIN DESCRIPTION

Pin Name	Pin No.	Function
$R_1 \sim R_7$ $C_1 \sim C_4$	1 ~ 7 25 ~ 28	Key input pins. $C_1 \sim C_4$ are set to low level in on-hook mode, while they are set to high level in off-hook standby mode. When the key input is off, key scanning and oscillation stop. Single contact keyboard shall be connected.
$\overline{HS}$	8	Hook switch input pin. $\overline{HS}$ = High: On-hook $\overline{HS}$ = Low: Off-hook
LSEL	24	Selection pin for $L_1 \sim L_{11}$ or $L_{12} \sim L_{22}$ for single-key dialing. LSEL = Low: $L_1 \sim L_{11}$ LSEL = High: $L_{12} \sim L_{22}$
MB	10	Make/Break ratio selection pin. MB = Low: 40/60 MB = High: 34/66 This input is sensed during the transition stage from On-hook to Off-hook.
DRS	11	Dial rate selection pin. DRS = Low: 10 pps DRS = High: 20 pps This input is sensed during the transition stage from On-hook to Off-hook.
MODE SEL	9	DP/DTMF mode selection pin. MODE SEL = Low: DP mode MODE SEL = High: DTMF mode The status at off-hook is maintained. If TONE key is pressed when this pin is being set to low level, the DTMF mode is established.
XT, $\overline{XT}$	12, 13	Ceramic resonator connection pins. Since this LSI is provided with oscillation inverter and feed-back resistor, 3.58 MHz ceramic resonator and capacitors are connected to XT and $\overline{XT}$ pin.
V_{DD}, V_{SS}	18, 15	V_{DD}: Positive power supply pin. 2.5 V ~ 6 V. V_{SS}: Negative power supply pin (Ground).
AC	16	IC initial pin. When IC is powered on, "H" level reset signal has to be applied to this pin.
TEST	14	Test pin.

Pin Name	Pin No.	Function
BD	17	Buzzer output pin. It outputs key tone for valid key input. It also outputs various alarm/confirming tone. Refer to "Sound output waveforms" for details.
DTMF OUT	19	DTMF output pin. In case of double keying or pressing some key without releasing a previous key, DTMF output is disabled.
DIAL PULSE	20	Dial pulse output pin. Make: High Break: Low $\overline{HS}$ = High (On hook): Low
$\overline{XMIT\ MUTE}$	21	Transmit mute output pin. When $\overline{HS}$ = High (On-hook): Low When $\overline{HS}$ = Low (Off-hook) ① While DP signal or DTMF signal is being sent out: Low ② All other times: High
$\overline{MUTE}$	22	Mute output pin. When $\overline{HS}$ = High (On-hook): Low When $\overline{HS}$ = Low (Off-hook) ① While DP is being sent out: Low ② All other times: High
DP MODE OUT	23	Dial Pulse Mode output pin. MODE SEL = High: Low MODE SEL = Low: High When mode is changed to DTMF mode by TONE key input: Low

FUNCTIONAL DESCRIPTION

Dialing Function

(1) Normal Dialing

Off-Hook [D_1] ..... [D_N]

Maximum 32 digits can be sent out at a time. Further key inputs are effective only after the first 32 digits have been sent out to the line. If more than 32 digits are dialed, redialing of that number is disabled. Pressing [PAUSE] key causes 4 seconds access pause. The access pause is released automatically 4 seconds later or manually by pressing [PAUSE], [RECALL], [STORE] or [TONE] key again.

Switching from DP dialing to DTMF dialing can be done during the course of dialing. By pressing [TONE] key during DP mode, the mode is changed to DTMF mode. When [TONE] key is pressed, if DP signal is being sent out, the mode will be changed after sending out all DP signal and an access pause of 4 seconds is automatically inserted. An access pause can be released earlier by pressing [PAUSE], [RECALL], [STORE] or [TONE] key, if so desired.

(2) Redialing

Off-Hook [Redial]

The last dialed number can be redialed by pressing [Redial] key. The functions of [TONE] and [PAUSE] signals included in the redialed number are same as in the repertory dialing. When the redialing is being prohibited, an alarm sound is generated at the [Redial] key input. The normal dialing can follow after that leaving the telephone off hook.

III

(3) Repertory Dialing

Off-Hook [R] [A_1] [A_2]

Off-Hook [L_n]

The telephone numbers abbreviated to [L_n] code can be dialed by single key operation ([L_1] ~ [L_{22}]), while those abbreviated to 2-digit can be dialed by pressing [RECALL] key followed by 2-digit code.

If a wrong address code is input, an alarm sound is generated.

If a stored number has an access pause, dialing halts for 4 seconds or until [PAUSE], [RECALL], [STORE] or [TONE] key is pressed. If a stored number has a [TONE] signal, the dialing mode is changed from DP mode to DTMF mode, and dialing halts for 4 seconds or until [PAUSE], [RECALL], [STORE] or [TONE] key is pressed.

(4) Mixed Dialing

Off-Hook [Redial] [D_1] ..... [D_n] [R] [A_1] [A_2] [L_n]

- [Redial]: Redial
- [D_1] ..... [D_n]: Normal dialing
- [R] [A_1] [A_2]: 2-digits abbreviated code dialing
- [L_n]: Single key dialing

Mixed dialing of normal dialing, redialing and repertory dialing can be done. In that case, however, redialing must come to the first part. If the digits of the mixed dialed number is up to 32, that number can be redialed.

Memory Storing/Clearing Function

(1) Storing of telephone number

Off-Hook [S] [D_1] ..... [D_n] [S] [A_1] [A_2] (Store into 2-digits abbreviated code address)

[S] [D_1] ..... [D_n] [S] [L] (Store into single key address)

Storing operation can be continued leaving the telephone off hook. When the storing of a telephone number has been completed, a sound is generated to indicate that the next number's storing is allowed. The first [STORE] key input can be omitted from the second number.

If the empty space of the repertory memory is less than 16 digits, an alarm sound is generated at the first [STORE] key input. In other words, if an alarm is not generated at the first [STORE] key input, minimum 16 digits can be newly stored.

An alarm sound is generated at the 505th digit input showing the memory has no more capacity. That 505th input digit can be stored in the memory, however, if the 506th digit is input, an alarm sound is generated again. That input digit is neglected and the entire key operation is disabled until the telephone is hooked on.

Maximum digits of a telephone number to be stored is 32. [TONE] signal and [PAUSE] signal are counted as one digit respectively.

If the 33rd digit is input, an alarm sound is generated and the entire key operation is disabled until the telephone is hooked on.

24 telephone numbers can be abbreviated to single key address codes, which are [L_1] ~ [L_{22}] . Other than those single key address codes, maximum 30 telephone numbers can be abbreviated to 2-digit address codes, which are 00 ~ 29, so fas as total stored digits in the repertory memory do not exceed 505.

[0] ~ [2] can be used for the first digit [A_1] , and [0] ~ [9] can be used for the second digit [A_2] . If a wrong number is used, an alarm sound is generated and that input is neglected.

(2) Mixed Storing

Off-Hook [S] [D_1] ..... [D_n] [R] [A_1] [A_2] [S] [A'_1] [A'_2]

..... Store into 2-digit abbreviated code address

Off-Hook [S] [L_m] [D_1] ..... [D_n] [L_n] [S] [L'_n]

..... Store into single key address

The telephone number once stored in the repertory memory can be used as a part of the newly stored telephone number in the form of abbreviated code ([L_n] or [R] [A_1] [A_2]). Maximum 32 digits can be mixed-stored. Either [L_n] or [R] [A_1] [A_2] is counted as 3 digits.

Therefore, if [L_n] key or [R] key is pressed at 31st or 32nd digit, an alarm sound is generated and storing is disabled.

Abbreviated code used for the newly stored number must not include abbreviated code of the other telephone number.

(3) Clearing of Telephone Number

Off-Hook [S] [S] [A_1] [A_2]

[S] [S] [L_n]

Clearing operation can be continued leaving the telephone off hook. Pressing [STORE] key twice followed by [L_n] key or 2-digit code clears the stored number in that address. Clearing operation and storing operation can be done alternately leaving the telephone off-hook.

If a wrong address code is input after pressing [STORE] key twice, an alarm sound is generated and that key input is neglected.

III

Redial Inhibition

Off-Hook [R] [A_1] [A_2] (After signals sent out) [S] [S]

Off-Hook [D_1] ..... [D_n] (After signals sent out) [S] [S]

Pressing [STORE] key twice after all signals have been sent out to the line disables the redialing of that telephone number. It is applicable to any of normal dialing, repertory dialing and mixed dialing. Redialing is also disabled when more than 32 digits are dialed or after telephone number's clearing/storing operation.

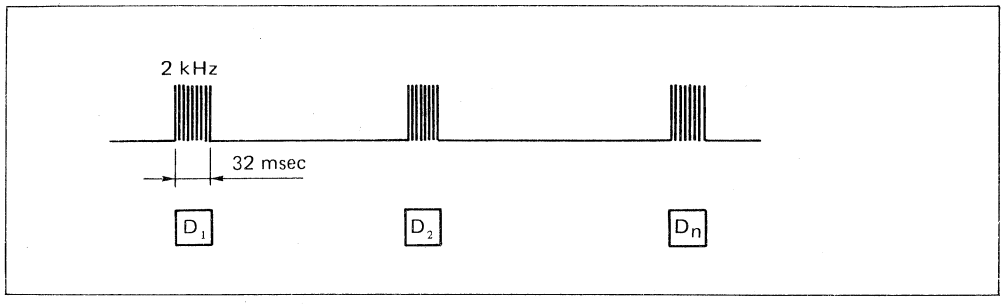
Others

When there is no data in the specified memory address, an alarm sound is generated and that key input is neglected.

SOUND OUTPUT WAVEFORM

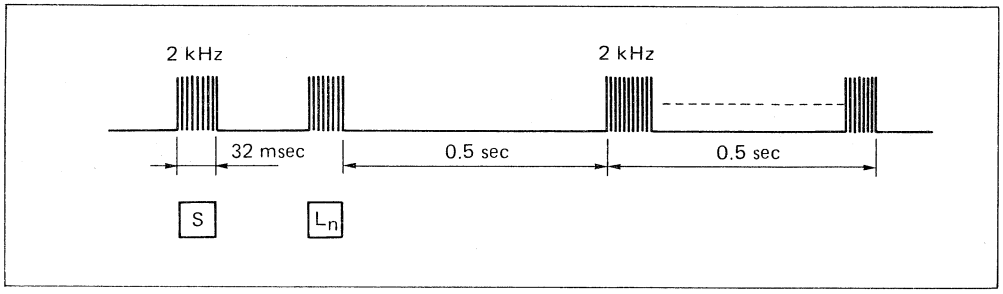
Operation Confirmation Sound

It is output for valid key input.



Storing Confirmation Sound

It is output when storing or clearing of telephone number has been completed.

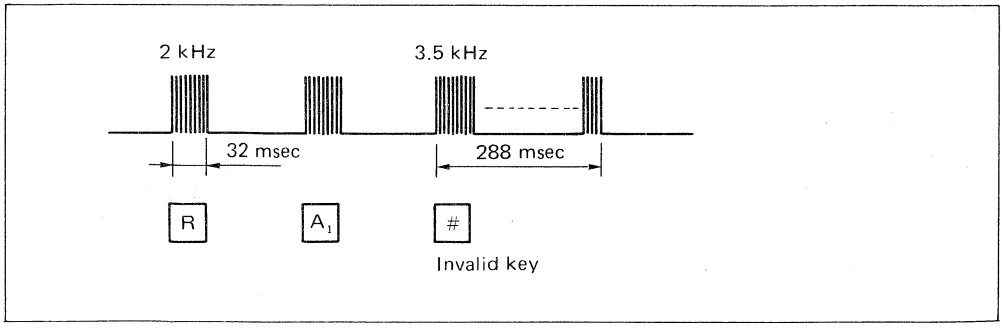


III

Alarm Sound (a)

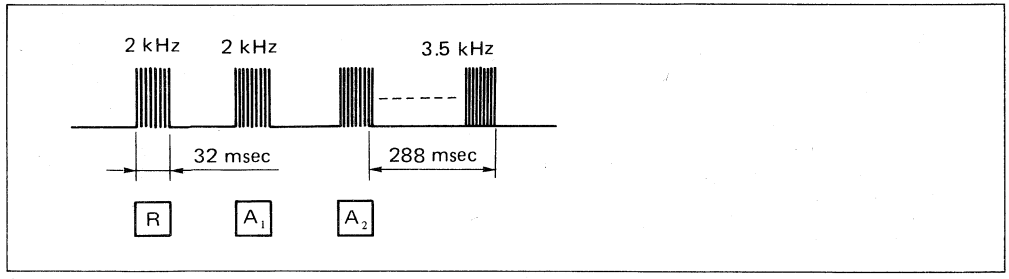
It is output for the followings.

- Wrong key input.
- 33rd digit input for storing.
- STORE key input when the empty capacity of repertory memory is less than 16 digits.



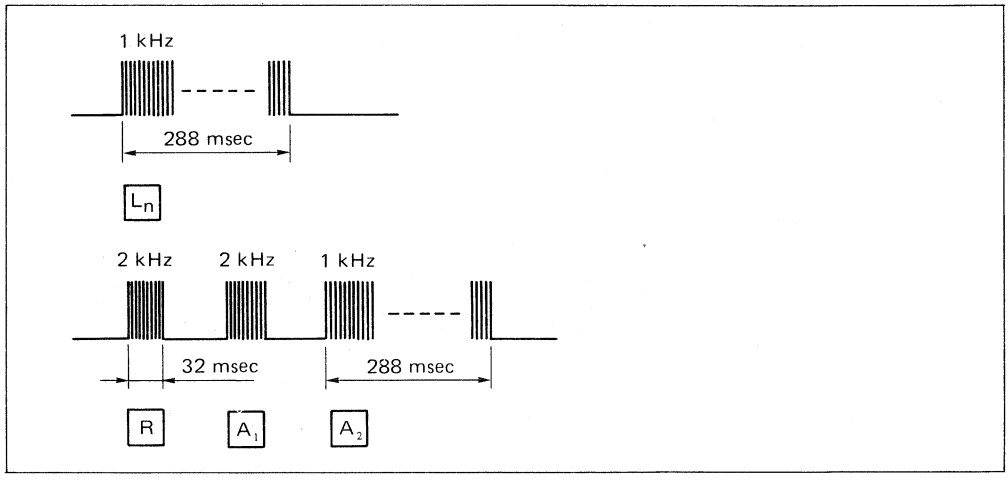
Alarm Sound (b)

It is used when the repertory number using other telephone number's abbreviated code as a part of it is used as a part of newly stored number.



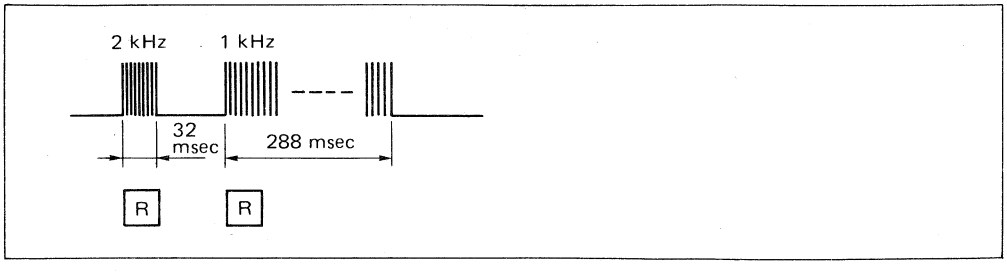
Alarm Sound (c)

It is output when there is no data in the accessed memory address.



Alarm Sound (d)

It is output when redial is prohibited.



ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Condition	Limits	Unit
Supply Voltage	V_{DD}	Ta = 25°C	-0.3 ~ +7.0	V
Input/Output Voltage	V_{IO}	Ta = 25°C	V_{SS}-0.3 ~ V_{DD}+0.3	V
Power Dissipation	P_D	Ta = 25°C	200	mW
Operating Temperature	Topr	—	-20 ~ +75	°C
Storage Temperature	Tstg	—	-55 ~ +125	°C

DC Characteristics

V_{DD} = 3.0 V, V_{SS} = 0 V, f_{OSC} = 3.579545 MHz, T_a = -20 ~ +75°C

Parameter	Symbol	Condition		Min	Typ	Max	Unit
Operating Voltage	V_{DD}			2.5	—	6.0	V
Memory Retention Voltage	V_{DDM}	Standby mode		1.2	—	6.0	V
Current Consumption (1)	I_{DDP}	Pulse Mode, No load		—	300	600	μA
Current Consumption (2)	I_{DDT}	Tone Mode, No load		—	1.2	2.4	mA
Memory Retention Current	I_{DDM}	ON HOOK,	V_{DD} = 2.5 V Ta = 25°C	—	—	0.2	μA
Output Current	I_{OH1}	$\overline{MUTE}$, $\overline{XMIT\ MUTE}$, DP	V_{OH} = 2.6 V	-200	—	—	μA
	I_{OL1}		V_{OL} = 0.4 V	500	—	—	μA
Output Current	I_{OH2}	C_1 ~ C_4	V_{OH} = 2.6 V	-1	—	—	mA
	I_{OL2}		V_{OL} = 0.4 V	10	—	—	μA
Output Current	I_{OH3}	DP MODE OUT BD	V_{OH} = 2.6 V	-20	—	—	μA
	I_{OL3}		V_{OL} = 0.4 V	10	—	—	μA
Input Current	I_{IH1}	$\overline{HS}$	V_{IH} = 3.0 V	—	—	2	μA
	I_{IL1}		V_{IL} = 0 V	-20	—	-180	μA
Input Current	I_{IH2}	R_1 ~ R_7	V_{IH} = 3.0 V	10	—	90	μA
	I_{IL2}		V_{IL} = 0 V	—	—	-2	μA
Input Current	I_{IH3}	LSEL, MB, DRS MODE SEL AC, TEST	V_{IH} = 3.0 V	30	—	300	μA
	I_{IL3}		V_{IL} = 0 V	—	—	-2	μA

AC Characteristics

f_{OSC} = 3.579545 MHz, 2.5 V ≤ V_{DD} ≤ 6.0 V, T_a = -20 ~ +75°C

Parameter	Symbol	Condition		Min	Typ	Max	Unit
Key Input Time	T_{KIN}			33	–	–	mS
Tone Output	V_{OUT}	ROW side only R_L = 1 KΩ	V_{DD} = 2.5 V	150	250	350	mV rms
			V_{DD} = 4.0 V	200	340	570	
High/Low Level Ratio	dB_{CR}			1.0	2.0	3.0	dB
Distortion	$\%_{Dis}$			–	5	10	%

Tone Output Frequency

f_{OSC} = 3.579545 MHz

Key Input	Nominal Frequency (Hz)	Output Frequency (Hz)	Distortion (%)
R_1	697	699.1	+0.30
R_2	770	766.2	-0.49
R_3	852	847.4	-0.54
R_4	941	948.0	+0.74
C_1	1209	1215.9	+0.57
C_2	1336	1331.7	-0.32
C_3	1477	1471.9	-0.35

III

Signal Output Timing

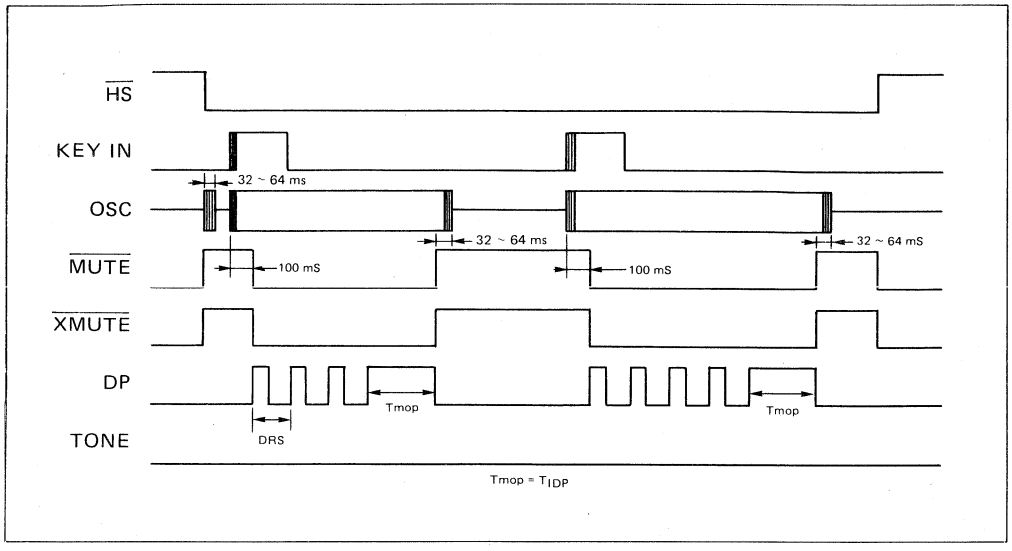
f_{OSC} = 3.579545 MHz

Parameter	Symbol	Condition	Typ	Unit
Tone Output Time	T_{tone}	Tone auto dial	100	mS
Inter Digit Pause	T_{IDP_1}	Tone auto dial	100	mS
	T_{IDP_2}	Pulse auto dial (10 pps)	800	mS
	T_{IDP_3}	Pulse auto dial (20 pps)	500	mS

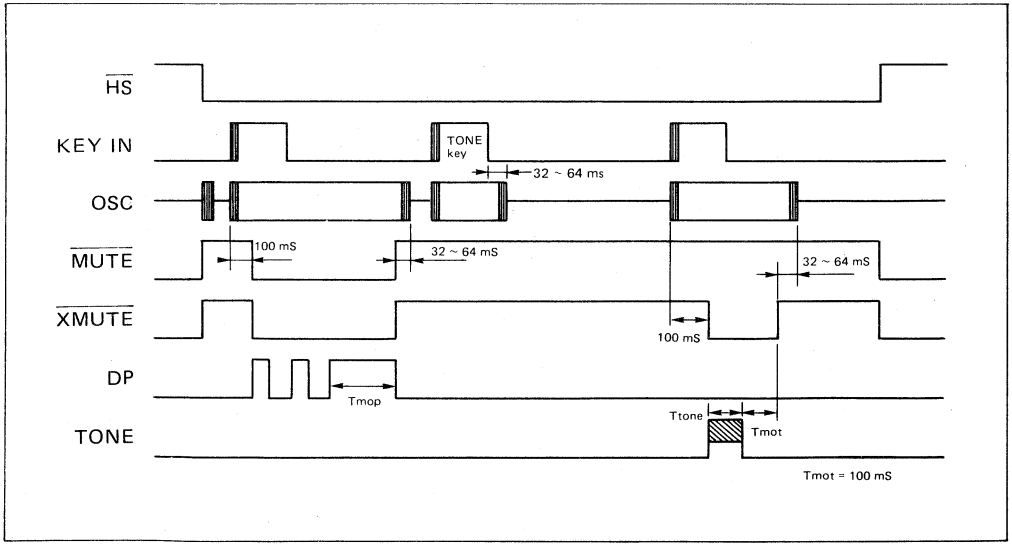
TIMING CHART

DP MODE TIMING CHART

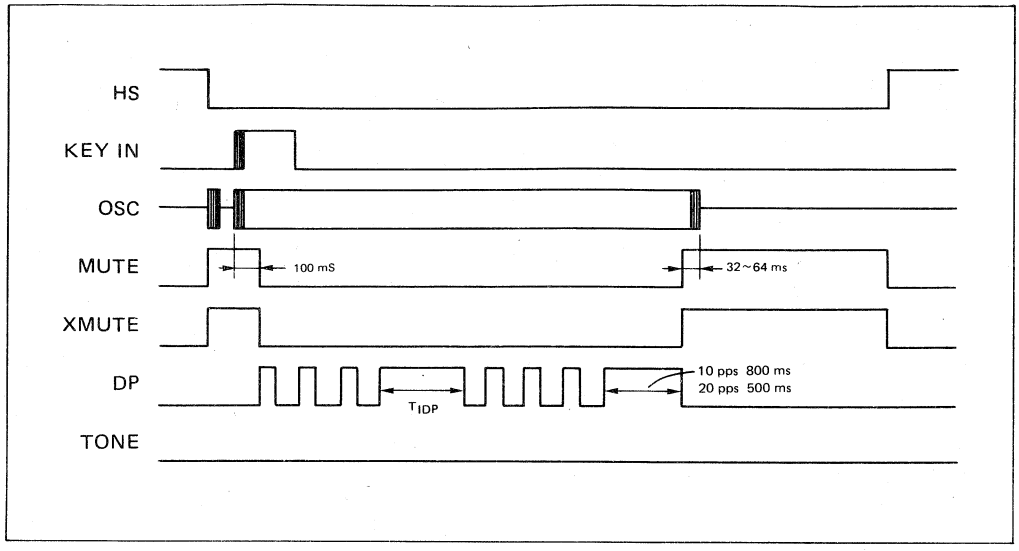
1) Normal dialing



2) Mode change-over by Tone key

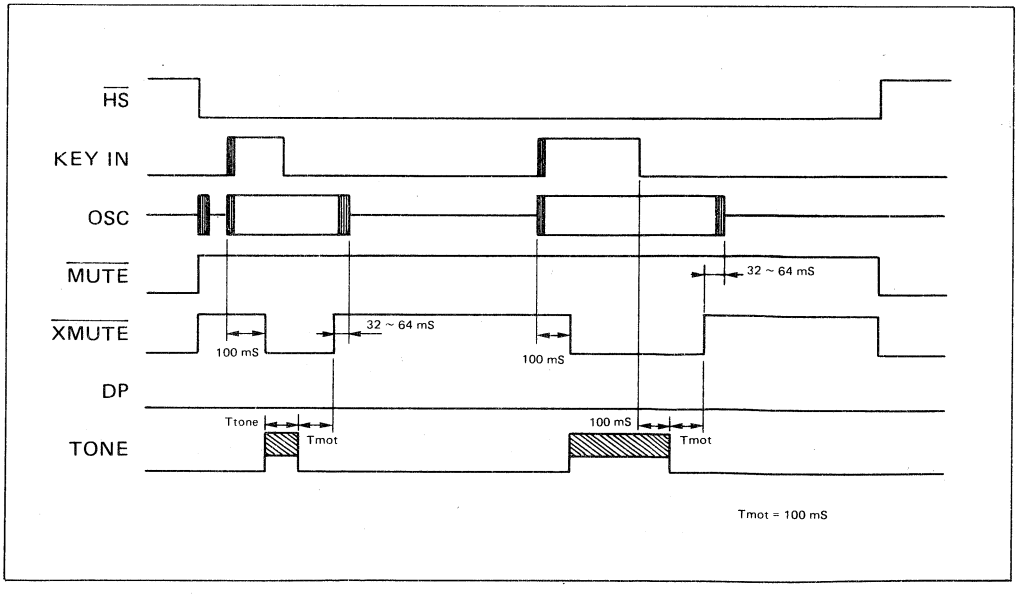


3) Repertory dialing

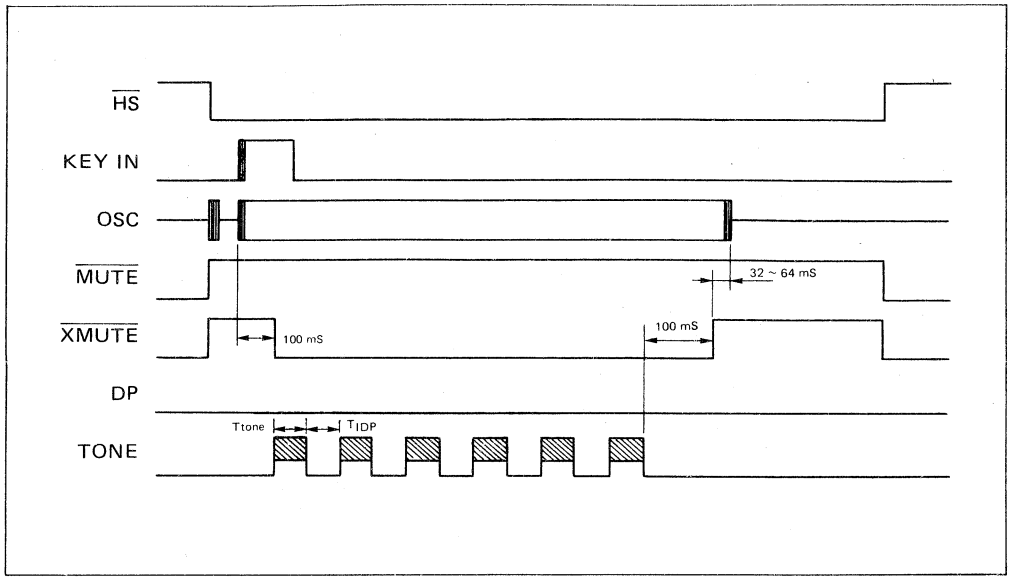


DTMF MODE TIMING CHART

1) Normal dialing



2) Repertory dialing, Last number re-dial



Preliminary

OKI semiconductor

MSM5070RS/MSM5071RS

TONE/PULSE SWITCHABLE DIALER WITH REDIAL

GENERAL DESCRIPTION

The MSM5070RS and the MSM5071RS are TONE/PULSE switchable dialers, with a redial function, which are fabricated by low power consumption CMOS metal gate technology.

The only difference between the MSM5070RS and MSM5071RS is Make/Break Ratio.

The MSM5070RS has 33/67% Make/Break Ratio, while MSM5071RS has 40/60% Make/Break Ratio.

These LSI can generate either DTMF or DP signal.

The maximum number of digits which can be dialed out are 31 digits. If the last dialed telephone number exceeds 32 digits, this redial memory area is used as a FIFO momory.

The operating voltage of these LSIs are 2.5 V – 5 V, while the minimum voltage required for memory retention is 1.2 V.

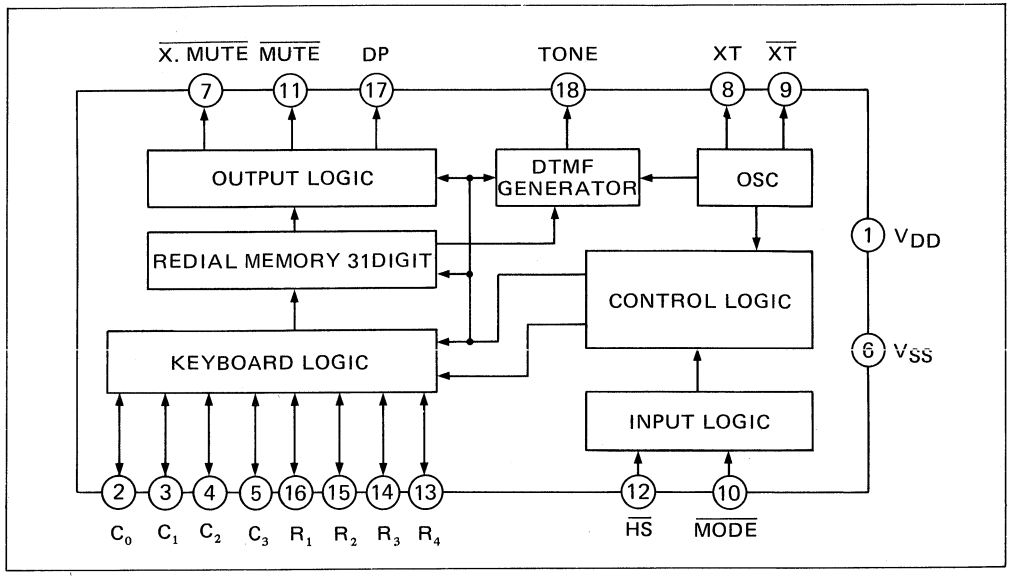
FEATURES

- Auto switching of DTMF/DP signal for redial function
- Last number redial, 31 digits maximum (If the dialed out telephone number exceeds 32 digits, this redial memory area is used as a FIFO memory.)
- Manual pause (By pressing either PAUSE or TONE key)
- Pulse rate selectable, 10 pps/20 pps
- Either single contact keyboard or standard 2 of 8 keyboard can be used
- Operating voltage, 2.5 V – 5 V
- Memory retention voltage, 1.2 V minimum
- 3.58 MHz crystal oscillation
- MUTE/XMIT MUTE output
- 18 pin plastic DIP package

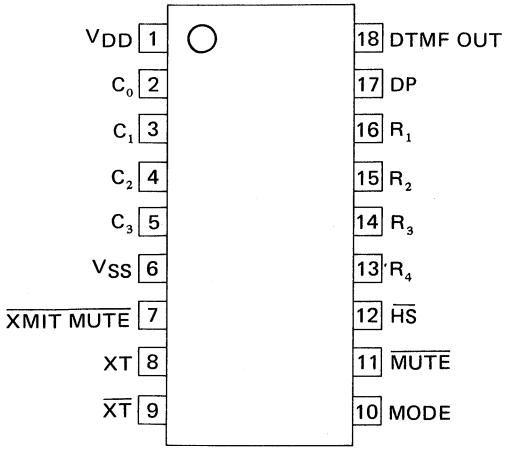
Make/Break Ratio	Type No.
33/67%	MSM5070RS
40/60%	MSM5071RS

III

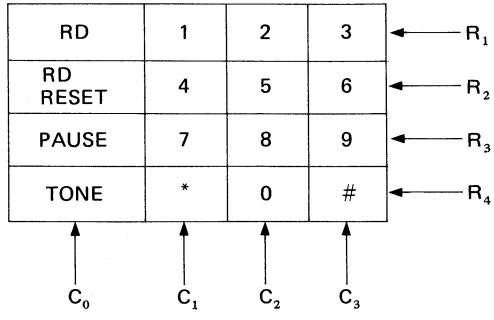
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION

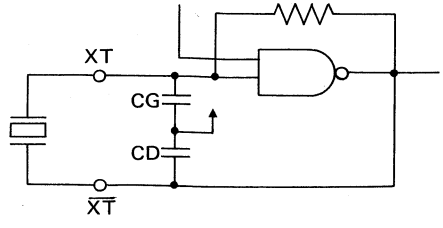


KEYBOARD LAYOUT



4 x 4 matrix keyboard as shown above shall be used. Either single contact keyboard or standard 2 of 8 keyboard can be used.

PIN DESCRIPTION

Pin Name	Pin No.	Function
$R_1 \sim R_4$ $C_0 \sim C_3$	13 ~ 16 2 ~ 5	Key input pins scanned at 500 Hz. Single contact keyboard or 2 of 8 keyboard shall be connected.
HS	12	HOOK SWITCH input pin, pulled up to V_{DD}. $\overline{HS}$ = Open: "ON HOOK" HS = V_{SS} : "OFF HOOK"
DTMF OUT	18	DTMF output pin. Open emitter output.
DP	17	Dial pulse output pin. MAKE : High level BREAK: Low level "ON HOOK": Low level CMOS Output
$\overline{MUTE}$	11	MUTE output pin. "ON HOOK" : Low level During DP output: Low level All other time (When $\overline{HS}$ = Low level): High level CMOS output
$\overline{XMIT\ MUTE}$	7	MUTE output pin for transmitter. ($\overline{HS}$ = Open) "ON HOOK" : Low level During DP or DTMF output: Low level All other time (When $\overline{HS}$ = Low level): High level
MODE	10	Mode selection pin. MODE = "V_{DD}": DTMF mode MODE = "Open": DP mode, 10 pps MODE = "V_{SS}" : DP mode, 20 pps
XT, $\overline{XT}$	8, 9	3.58 MHz crystal connection pin. Since both MSM5070RS and MSM5071RS are provided with on-chip CG, CD and Rfb, no external components are required for the connection except a crystal oscillator. 

III

FUNCTIONAL DESCRIPTION

Redial

The maximum number of digits which can be stored in the redial memory area is 31 digits. As for the number which exceeds 32 digits, this memory area is used as a FIFO memory, in this case the redial function is prohibited.

By pressing [RR] key, the redial function is disabled. If [RR] key is pressed or the telephone is ON HOOKed during DTMF/DP signal is being output, signal output is stopped and the redial is disabled.

Note: [RR] : [RD RESET]

Mode Selection

Signal output mode is selected by the condition of MODE pin (pin 10) as described in PIN DESCRIPTION.

Mode change from DP mode to DTMF mode

DTMF mode can be established automatically by connecting MODE pin to V_{DD} or pressing TONE key during DP mode. The mode cannot be changed from DTMF mode to DP mode by the input from the keyboard.

If the mode is changed from DP mode to DTMF mode by pressing the TONE key, a pause is automatically inserted and the output of signal is disabled until the pause is manually released.

Pause

A pause is inserted by pressing the [PAUSE] key or [TONE] key. This pause is manually released by pressing any key. At that time, [PAUSE], [REDIAL] and [TONE] keys function only to release a pause, and their original functions are suppressed. In case of other keys, however, they provide not only a pause release function but also their original function.

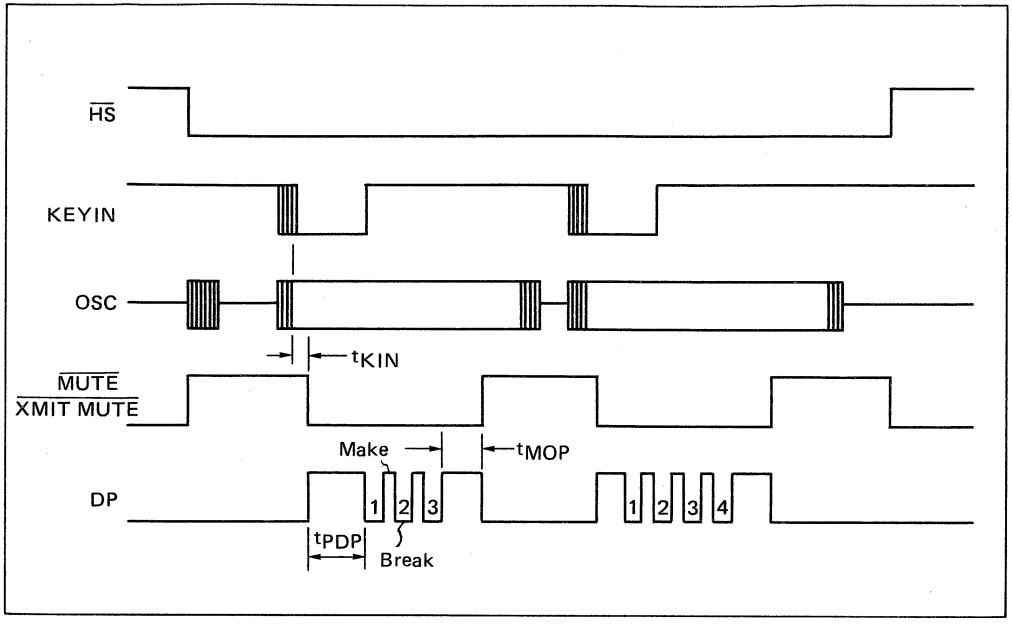
If a pause is used during the course of dialing, this 'pause' information is automatically inseterd. In case of redial, however, the pause condition has to be released manually.

Mixed Dialing

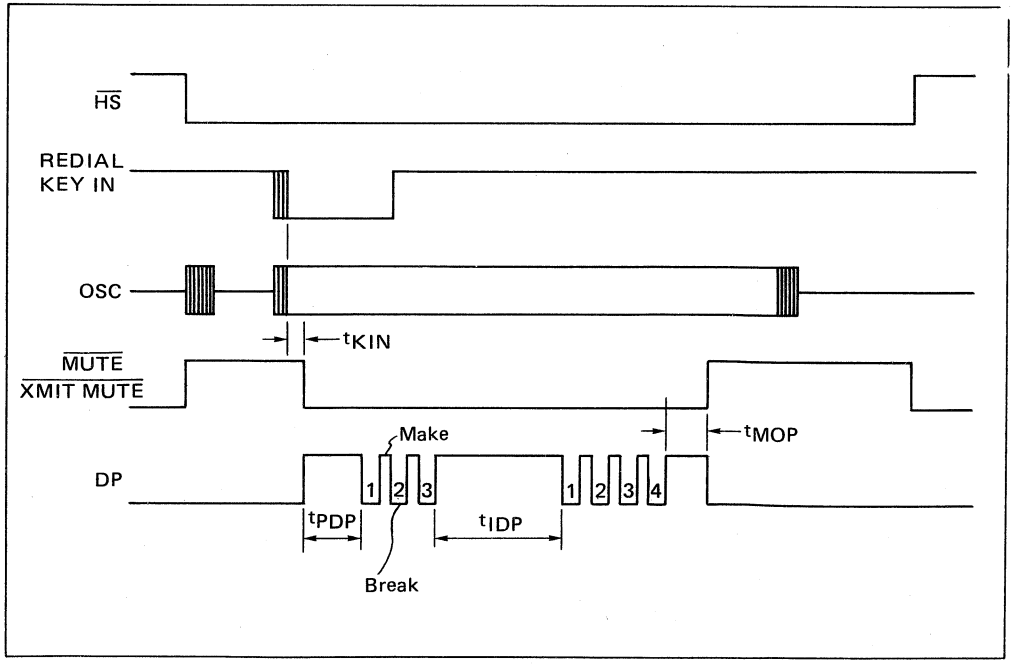
After the stored number has been redialed, normal dialing can be added. In that case, the repertory number plus added number is stored in the memory for the next redialing, if the total digits are within 31. If the total digits are more than 31, redialing is disabled.

DP MODE TIMING CHART

- **Normal Dialing**



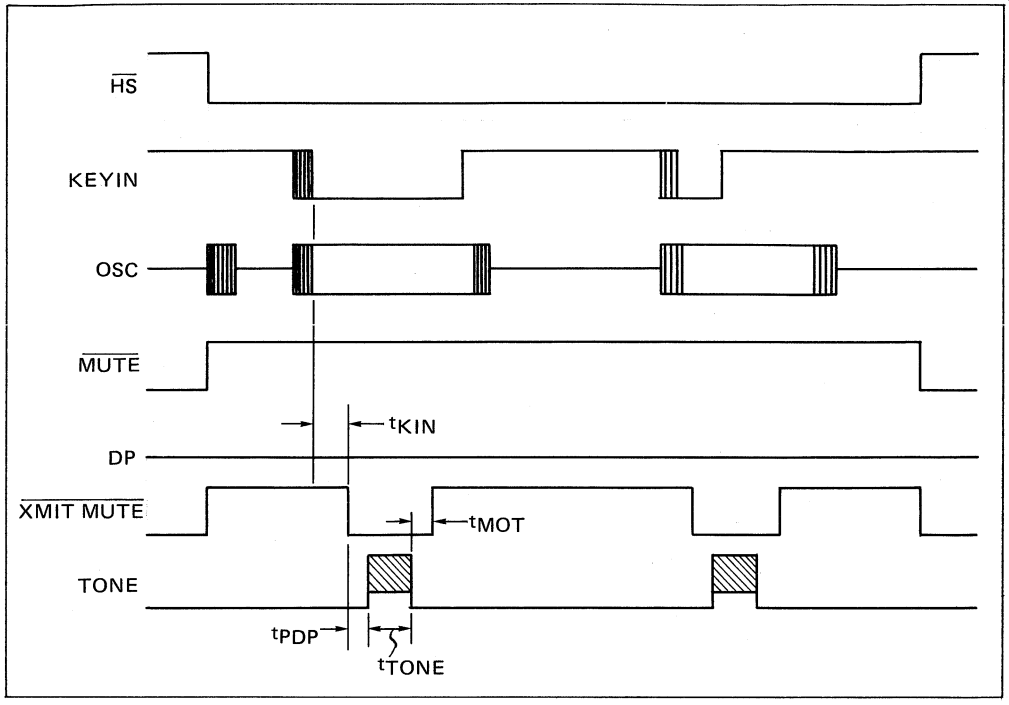
- **Redial**



III

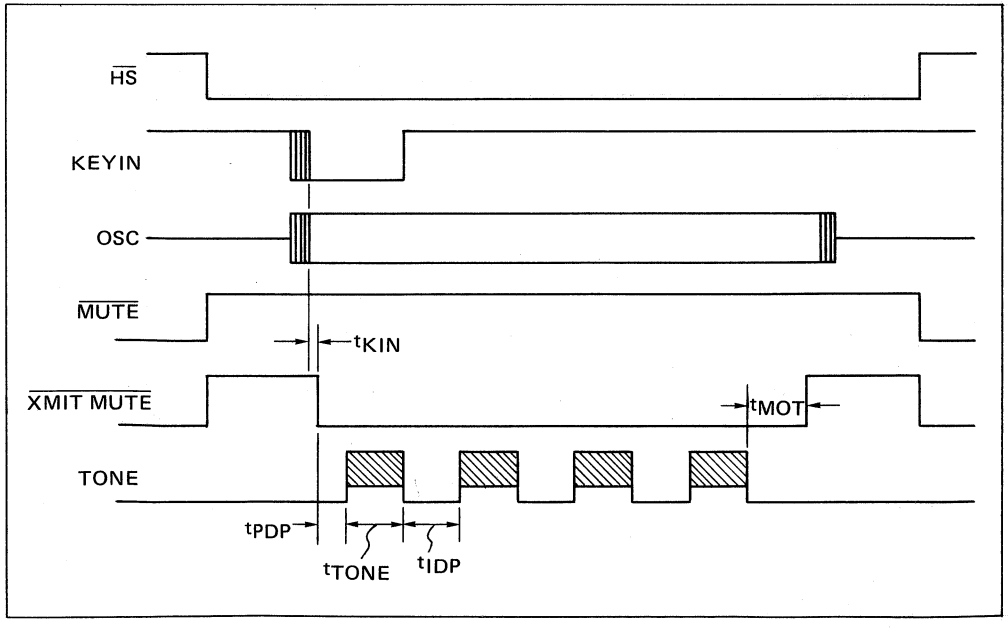
DTMF MODE TIMING CHART

- **Normal Dialing**



III

- **Redial**



AC CHARACTERISTICS

1) Key Operation Time

$f_{X\text{-}TAL}$ = 3.579545 MHz $2.5 \geqq V_{DD} \leqq 5.0$ V

Parameter	Symbol	Min	Typ	Max	Unit
Effective key input time	t_{KD}	35	—	—	ms
Key scanning frequency	f_{KEY}	—	500	—	Hz
Key input time	t_{KIN}	32.7	34.7	36.7	ms
On-Hook confirming time	t_{ONH}	2	—	—	ms

2) DTMF Output Frequency

$f_{X\text{-}TAL}$ = 3.579545 MHz

Key input	Nominal frequency (Hz)	Output frequency (Hz)	Distortion (%)
R_1	697	699.1	+0.30
R_2	770	766.2	-0.49
R_3	852	847.4	-0.54
R_4	941	948.0	+0.74
C_1	1209	1215.9	+0.57
C_2	1336	1331.7	-0.32
C_3	1477	1471.9	-0.35

3) DTMF Signal

$f_{X\text{-}TAL}$ = 3.579545 MHz

Parameter	Symbol	Min	Typ	Max	Unit
Tone output time	t_{TONE}	—	100	—	ms
Predigit pause	t_{PDP}	63.3	65.3	67.3	ms
Interdigit pause	t_{IDP}	—	100	—	ms
Mute time after DP	t_{MOT}	—	100	—	ms

4) DP Signal

$f_{X\text{-}TAL}$ = 3.579545 MHz

Type No.	Make %	Dial pulse PPS	Break ms	t_{PDP} ms	t_{IDP} ms	t_{MOP} ms
MSM5070RS	33	10	67	98.3±2	831.3±2	800
		20	33.5	31.8±2	465.3±2	450
MSM5071RS	40	10	60	105.3±2	905.3±2	800
		20	30	35.3±2	485.3±2	450

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	V_{DD}	Ta = 25°C	−0.3 ~ 6.0	V
Input voltage	V_{IN}	Ta = 25°C	V_{SS} −0.3 ~ V_{DD} +0.3	V
Output voltage	V_{OUT}	Ta = 25°C	V_{SS} −0.3 ~ V_{DD} +0.3	V
Power dissipation	P_D	Ta = 25°C	200	mW
Operating temperature	T_{OP}	—	−20 ~ +75	°C
Storage temperature	T_{stg}	—	−55 ~ +125	°C

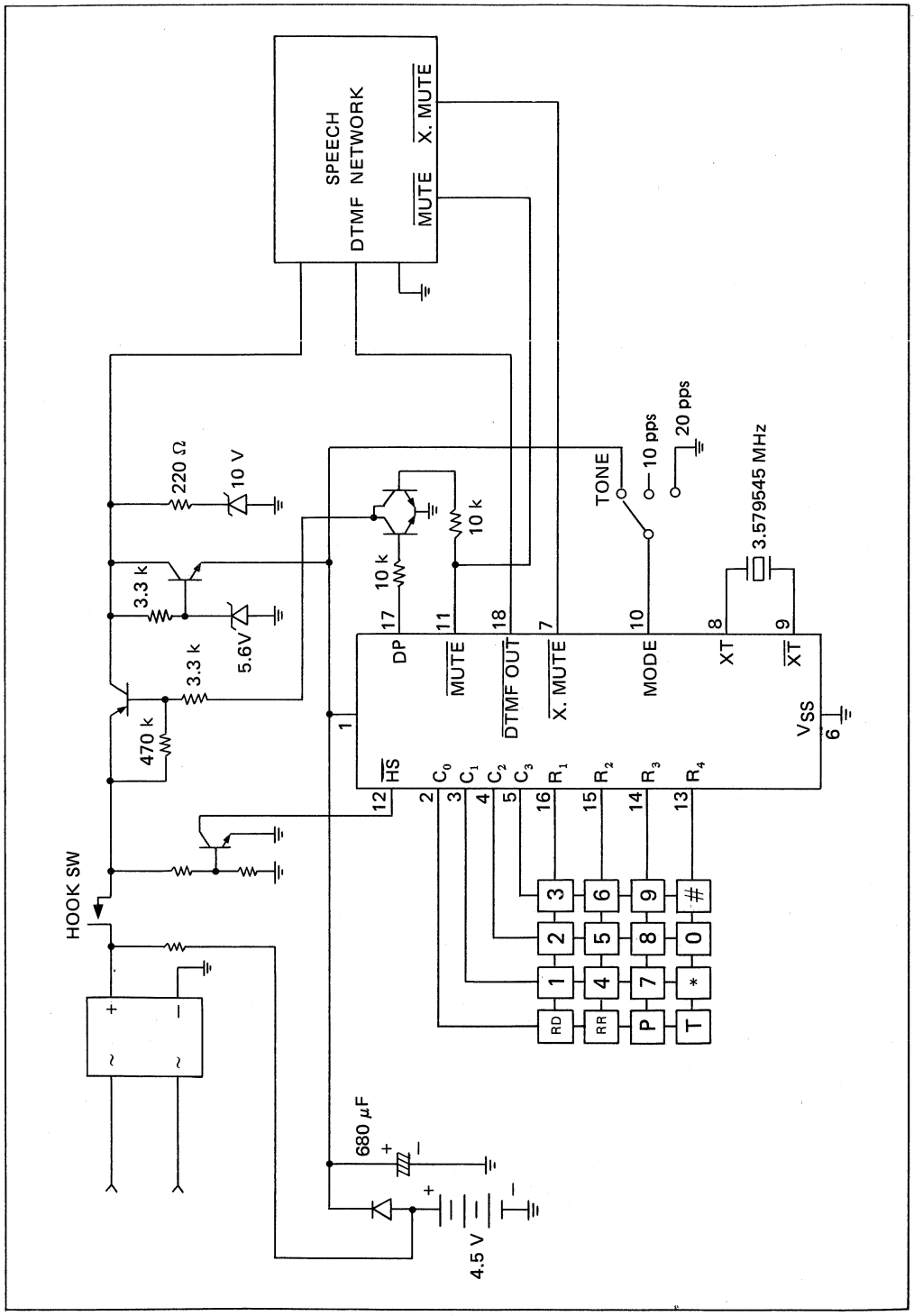
ELECTRICAL CHARACTERISTICS

$f_{X\text{-}TAL}$ = 3.57945 MHz Ta = 25°C

Parameter	Symbol	Condition		Rating Min	Rating Typ	Rating Max	Unit
Operating voltage	V_{DD}	—		2.5	—	5.0	V
Power consumption (1)	I_{DD}	No load, during tone output, V_{DD} = 5 V		—	3	6	mA
Power consumption (2)	I_{DD2}	No load, key input off, operation halt, V_{DD} = 5 V		—	—	100	μA
Memory retention voltage	V_{DDH}	On hook, operation halt		1.2	—	5.0	V
Memory retention current	I_{DDH}	On hook, operation halt, V_{DD} = 2.5 V		—	—	0.2	μA
Input voltage (1) (C_0~C_3, R_1~R_4) $\overline{HS}$	V_{IH1}	V_{DD} = 2.5 ~ 5 V		$0.8V_{DD}$	—	V_{DD}	V
	V_{IL1}			V_{SS}	—	$0.2V_{DD}$	
Input voltage (2) (MODE)	V_{IH2}	V_{DD} = 2.5 ~ 5 V		$0.9V_{DD}$	—	V_{DD}	V
	V_{IM2}			$0.4V_{DD}$	$0.5V_{DD}$	$0.6V_{DD}$	
	V_{IL2}			V_{SS}	—	$0.1V_{DD}$	
Input current (1) ($\overline{HS}$)	I_{IH1}	V_{DD} = 5 V	V_{IH} = 5.0 V	—	—	−1	μA
	I_{IL1}		V_{IL} = 0.0 V	−60	−120	−240	
Input current (2) (C_0~C_3, R_1~R_4)	I_{IH2}	V_{DD} = 5 V	V_{IH} = 1.2 V	−20	−30	−50	μA
	I_{IL2}		V_{IL} = 1.2 V	120	180	275	
Input current (3) (MODE)	I_{IH3}	V_{DD} = 5 V	V_{IH} = 4.5 V	110	160	250	μA
	I_{IM3}		V_{IM} = 2.5 V	−20	0	20	
	I_{IL3}		V_{IL} = 0.5 V	−110	−160	−250	
Output voltage (1) (MODE)	V_{OM}	V_{DD} = 2.5 ~ 5 V Open		$0.45V_{DD}$	$0.5V_{DD}$	$0.55V_{DD}$	V
Output current ($\overline{XMITMUTE}$, $\overline{MUTE}$, DP)	I_{OH1}	V_{DD} = 3 V	V_{OH} = 2.6 V	−0.2	—	—	mA
	I_{OL1}		V_{OL} = 0.4 V	0.5	—	—	
Oscillation rise time	t_{RISE}	V_{DD} = 2.5 ~ 5 V		—	3.0	10	mS
Tone output voltage	V_{OUT}	V_{DD} = 3 V R_L = 1 kΩ		—	300	—	mV RMS
High/Low ratio	dBCR	V_{DD} = 2.5 ~ 5 V		1.5	2.0	2.5	dB
Distortion	% Dis	V_{DD} = 2.5 ~ 5 V		—	—	10	%
Internal capacitance	CD, CG	V_{DD} = 2.5 ~ 5 V		—	12	—	pF

III

MSM5070RS/MSM5071RS APPLICATION CIRCUIT



MSM6224RS

DTMF TONE DIALER LSI

GENERAL DESCRIPTION

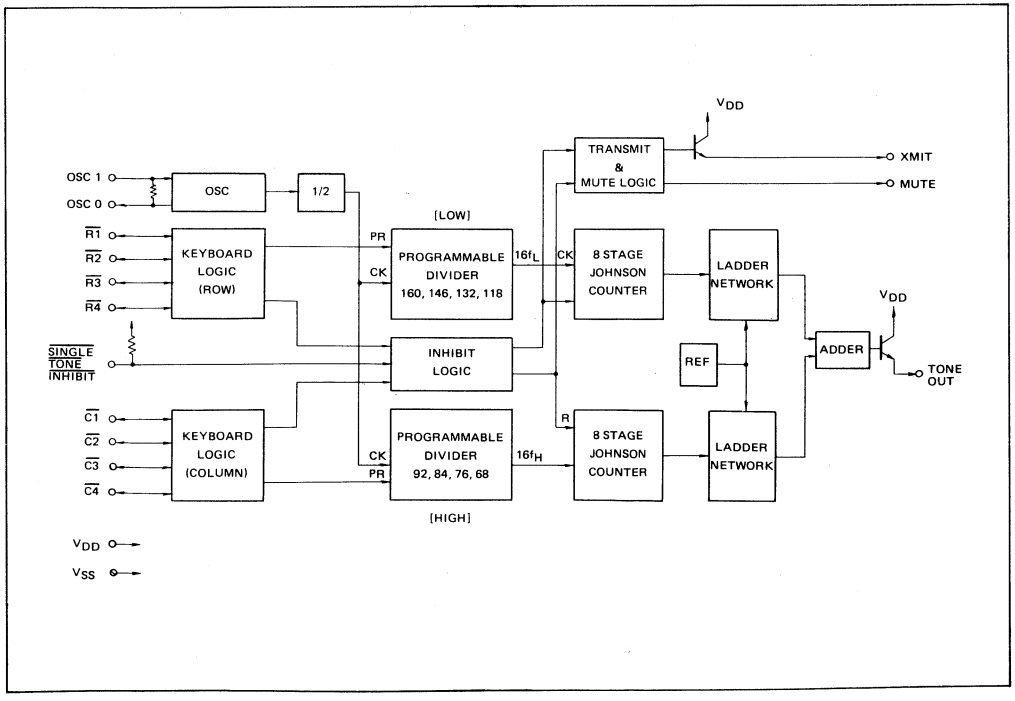
The MSM6224RS is a TONE dialer LSI which is fabricated by OKI's low power consumption CMOS silicon gate technology.

The MSM6224RS can generate 16 kinds of DTMF (Dual Tone Multi Frequency) signals each of which consists of 4 higher group frequency and 4 lower group frequency.

FEATURES

- Either the standard 2 of 8 keyboard or the calculator type keyboard can be used.
- Low power consumption by use of the CMOS silicon gate technology.
- Supply voltage 2.5 V ~ 8.5 V.
- Either the single tone or the dual tone ouptut.
- 3.579545 MHz crystal oscillation.

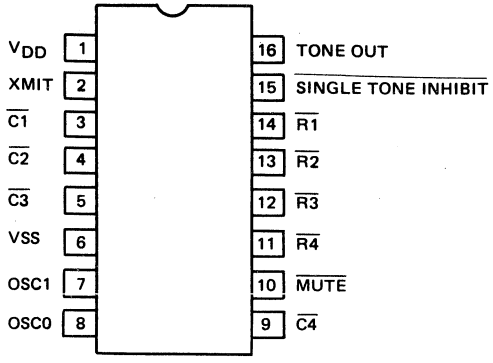
FUNCTIONAL BLOCK DIAGRAM



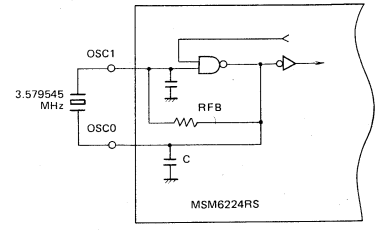
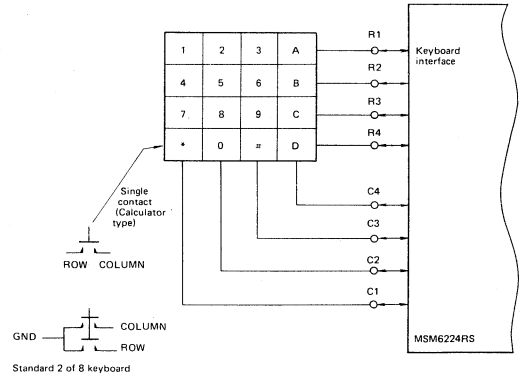
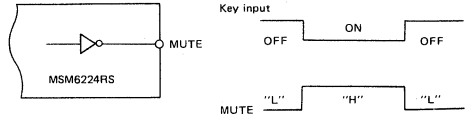
III

PIN CONFIGURATION

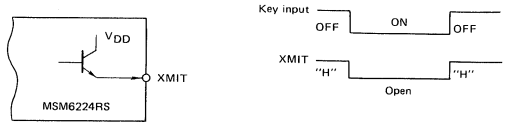
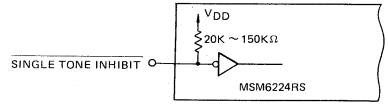
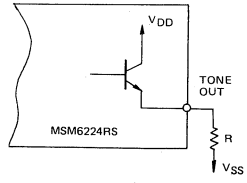
16 Lead Plastic DIP
(TOP View)



PIN DESCRIPTION

Pin Name	Pin No.	Function
OSC1, OSC0	7, 8	The 3.579545 MHz crystal oscillator is connected to these pins. A feedback resistor and the condensers are incorporated. 
$\overline{R1} \sim \overline{R4}$, $\overline{C1} \sim \overline{C4}$	14, 13, 12, 11, 3, 4, 5, 9	$\overline{R1} \sim \overline{R4}$ are the I/O pins of the row side, while $\overline{C1} \sim \overline{C4}$ are the I/O pins of the column side. All of those pins are provided with the pull up resistors internally. The resistance value is 20K ~ 150K ohms. The dual tone is output from the TONE OUT pin by connecting a row input to a column input or by setting both of a row input and a column input to the ground voltage. Either the calculator type keyboard or the standard 2 of 8 keyboard can be used with MSM6224RS.  The Table 1 shows the relation between the nominal frequency and the tone output frequency while the Table 2 shows the input conditions of $\overline{R1} \sim \overline{R4}$ and $\overline{C1} \sim \overline{C4}$. ● Refer to the note.
MUTE	10	The MUTE pin drives the external bipolar transistor by the CMOS output. This pin is low level when the key input is off, while it becomes high level when the key input is on. The MUTE is used for the mute of the receiver. 

III

Pin Name	Pin No.	Function
XMIT	2	The XMIT pin drives the external bipolar transistor by the NPN open emitter output. This pin is high level when the key input is off, while it becomes open when the key input is on. The XMIT pin is used for the mute of the transmitter. 
$\overline{\text{SINGLE TONE INHIBIT}}$	15	When more than two columns are selected against only one row, or when more than two rows are selected against only one column, the single tone is output from the TONE OUT pin. The $\overline{\text{SINGLE TONE INHIBIT}}$ pin is the negative logic input pin to control the output of the TONE OUT pin in those cases. Refer to the Table 2. When the input to this pin is high level, both of the single tone and dual tone are output from the TONE OUT pin. When the input to this pin is low level, however, the single tone is prohibited to output from the TONE OUT pin and becomes DC level. This pin is provided with the pull up resistance of 20K ~ 150K ohms. 
TONE OUT	16	The low group frequency and the high group frequency selected by the keyboard are synthesized and output from this TONE OUT pin. Because the output form is the NPN open emitter style, the load resistance must be connected externally. It is same for the case of the single tone output. The output amplitude of the high group is 1 ~ 2 dB bigger than that of the low group. The distortion of the dual tone is maximum 10%. 
V_{DD}, V_{SS}	1, 6	V_{DD} is a power supply pin. V_{SS} is a ground pin.

III

Note:

Table 1

Effective input		Nominal frequency	Tone output frequency	Accuracy	Remarks
(ROW)	$\overline{R1}$	697 Hz	699.1 Hz	+0.30 %	Low group
	$\overline{R2}$	770 Hz	766.2 Hz	-0.49 %	
	$\overline{R3}$	852 Hz	847.4 Hz	-0.54 %	
	$\overline{R4}$	941 Hz	948.0 Hz	+0.74 %	
(COLUMN)	$\overline{C1}$	1209 Hz	1215.9 Hz	+0.57 %	High group
	$\overline{C2}$	1336 Hz	1331.7 Hz	-0.32 %	
	$\overline{C3}$	1477 Hz	1471.9 Hz	-0.35 %	
	$\overline{C4}$	1633 Hz	1645.0 Hz	+0.73 %	

Table 2

Row input	Column input	Tone output*	Note
No	No	0V	
1	1	$f_L + f_H$	Dual tone
No	1	f_H	Single tone (Only column)
1	No	0V	
More than 2	No	0V	
More than 2	1	f_H	Single tone
No	More than 2	0V	
1	More than 2	f_L	Single tone
More than 2	More than 2	0V	

* The tone output shown is in the case when the load resistance is connected between the TONE OUT pin and the V_{SS}.

f_L: Low group f_H: High group

III

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Condition	Limit	Unit
Supply voltage	V_{DD}	Ta = 25°C	−0.3 ~ 9.5	V
Storage temperature	Tstg		−55 ~ +150	C°
Input voltage	V_I		V_{SS}-0.3~V_{DD}+0.3	V
Output voltage	V_O		V_{SS}-0.3~V_{DD}+0.3	V
Maximum current power dissipation	P_D	Ta = 70°C	500	mW

Operating Range

Parameter	Symbol	Condition	Limit	Unit
Supply voltage	V_{DD}	—	2.5 ~ 8.5	V
Operating temperature	T_{OP}	—	−30 ~ +70	C°

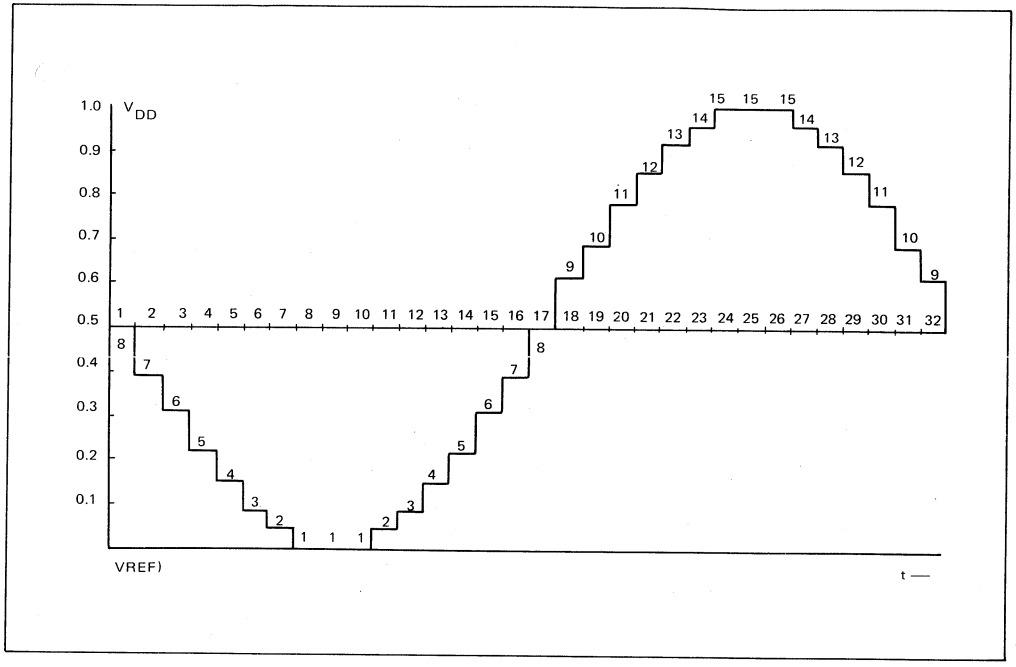
DC Characteristics

(Ta = −30 ~ +85°C)

Parameter	Symbol	Conditions	Limit			Unit	Applicable pin
			Min	Typ	Max		
"H" output voltage	V_{OH}	V_{DD}=3.0V I_{OH}=15mA	1.5			V	XMIT
		V_{DD}=10V I_{OH}=50mA	7.0				
"OFF" leak current	I_{OFF}	V_{DD}=8.5V V_{OF}=0V			100	μA	XMIT
"H" output current	I_{OH}	V_{DD}=3.0V V_{OH}=2.5V	0.17			mA	MUTE
		V_{DD}=8.5V V_{OH}=8.0V	0.57				
"L" output voltage	I_{OL}	V_{DD}=3.0V V_{OL}=0.5V	0.53			mA	MUTE
		V_{DD}=8.5V V_{OL}=0.5V	2.0				
"H" input voltage	V_{IH}		0.7 V_{DD}		V_{DD}		$\overline{C1}$~$\overline{C4}$, $\overline{R1}$~$\overline{R4}$
"L" input voltage	V_{IL}		V_{SS}		0.3 V_{DD}		"
"L" input current	I_{IL}	V_{DD}=8.5V V_{IL}=0V	0.0567		0.425	mA	"
"H" input current	I_{IH}	V_{DD}=8.5V V_{IH}=8.5V			10	μA	"
"TONE OUT" output voltage (Single tone)	V_{OUT}	V_{DD}=3.0V RL=1KΩ (Row tone)	235		437	mV rms	TONE OUT
Difference of high/ low band level	dB CR	V_{DD}=3.0 ~ 8.5V	1	1.5	2	dB	"
Distortion	% DIS	V_{DD}=3.0 ~ 8.5V			10	%	"
"H" input current	I_{IH}	V_{DD}=8.5V V_I=8.5V			1	μA	$\overline{SINGLE\ TONE\ INHIBIT}$
"L" input current	I_{IL}	V_{DD}=8.5V V_I=0V	0.0567		0.425	mA	"
"H" input voltage	V_{IH}		0.7 V_{DD}		V_{DD}	V	"
"L" input voltage	V_{IL}		V_{SS}		0.3 V_{DD}	V	"
Power consumption (Stand-by)	I_{DDS}	No load V_{DD}=8.5V Key-OFF			200	μA	"
Power consumption (Operating)	I_{DD}	No load V_{DD}=8.5V Key-ON			25	mA	
"L" output voltage	V_{OL}	V_{DD}=3V I_{OL}=0.2mA	0.4			V	C1~C4, R1~R4
TONE OUT Rise Time	tRise	V_{DD}=3.0 ~ 8.5V			5	mS	TONE OUT

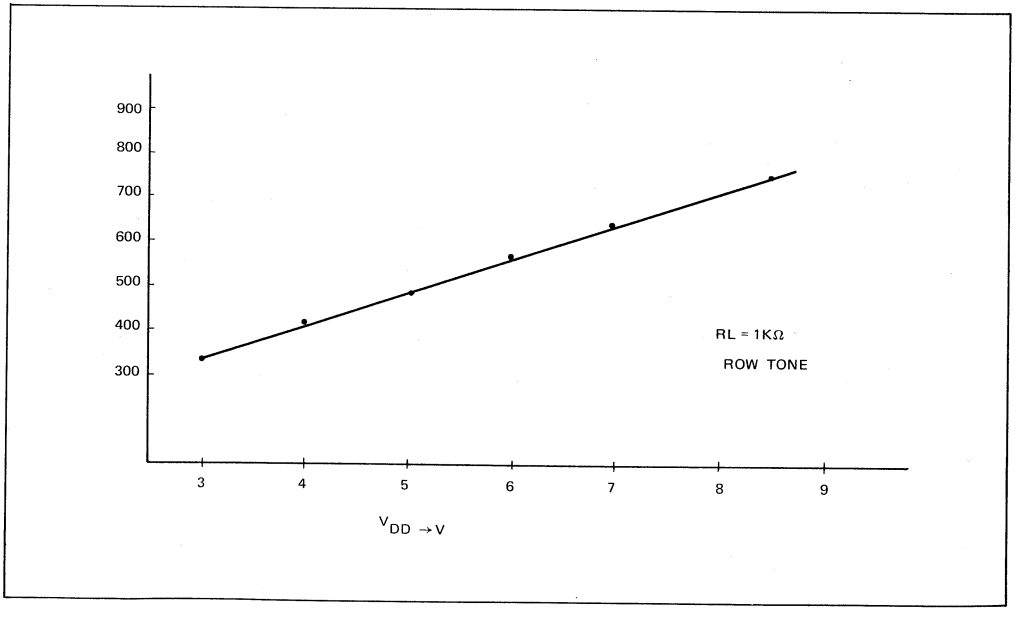
III

Sample Waveform of The Single Tone



III

Tone Amplitude (mV rms)



MSM6234RS

DTMF TONE DIALER LSI

GENERAL DESCRIPTION

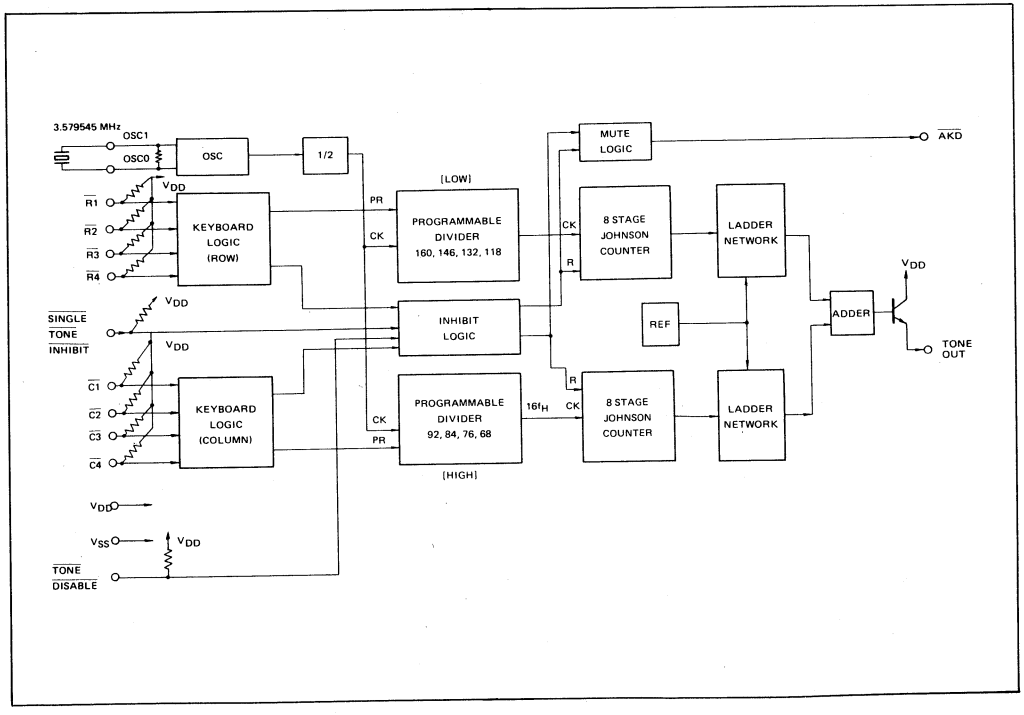
The MSM6234RS is a TONE dialer LSI which is fabricated by OKI's low power consumption CMOS silicon gate technology.

The MSM6234RS can generate 16 kinds of DTMF (Dual Tone Multi Frequency) signals each of which consists of 4 higher group frequency and 4 lower group frequency.

FEATURES

- The standard 2 of 8 keyboard can be used.
- The low power consumption by use of CMOS silicon gate technology.
- Supply voltage 2.5 V ~ 8.5 V.
- Either single tone or dual tone output.
- 3.579545 MHz crystal oscillation.
- Interface with microcomputer.

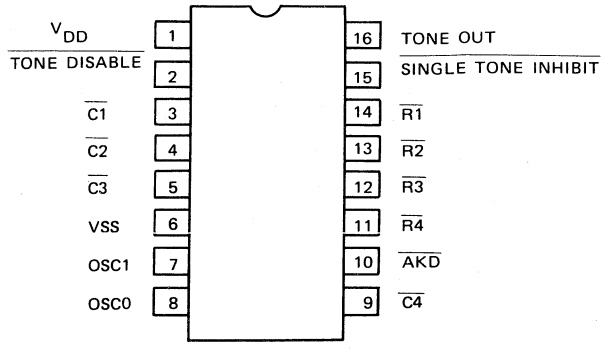
FUNCTIONAL BLOCK DIAGRAM



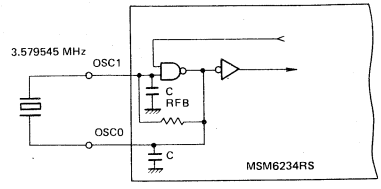
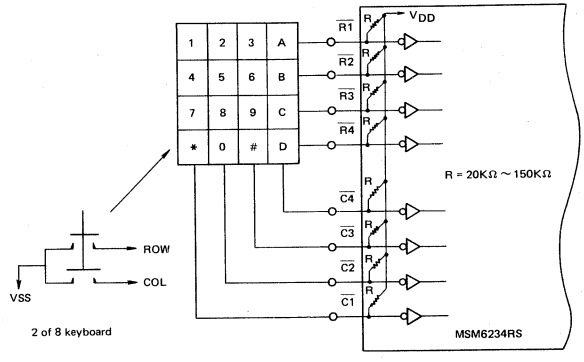
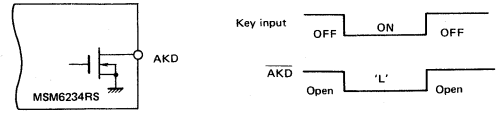
III

PIN CONFIGURATION

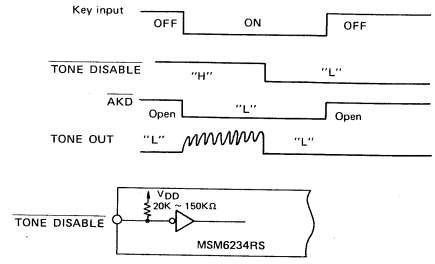
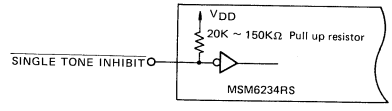
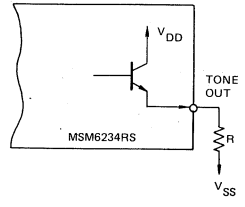
16 Lead Plastic DIP
(Top View)



PIN DESCRIPTION

Pin Name	Pin No.	Function
OSC1, OSC0	7, 8	The 3.579545 MHz crystal oscillator is connected to these pins. A feedback resistor and the condensers are incorporated. 
$\overline{R1} \sim \overline{R4}$ $\overline{C1} \sim \overline{C4}$	14, 13, 12, 11, 3, 4, 5, 9	Those are input pins of negative logic to be connected to the keyboard. The standard 2 of 8 keyboard can be used with MSM6234RS as illustrated below.  $\overline{R1} \sim \overline{R4}$ are the input pins of thr row side, while $\overline{C1} \sim \overline{C4}$ are the input pins of the column side. All of those pins are provided with the pull up resistor of 40K ~ 100K ohms internally. The dual tone is output from the TONE OUT pin, by setting both of a row input and a column input to the ground voltage. The Table 1 (See Note) shows the relation between the nominal frequency and the tone output frequency, while the Table 2 (See Note) shows the input condition of $\overline{R1} \sim \overline{R4}$ pins and $\overline{C1} \sim \overline{C4}$ pins. • Refer to the Note.
$\overline{AKD}$	10	$\overline{AKD}$ pins drives the external bipolar transistor by its N-channel open drain output. This pin is open when the key input is off, while it becomes low when the key input is on. $\overline{AKD}$ is used for the mute of the transmitter/receiver. 

III

Pin Name	Pin No.	Function
$\overline{\text{TONE DISABLE}}$	2	This is an input pin to control the output of the TONE OUT pin. When the input to this pin is high level, the TONE OUT pin normally operates. When the input to this pin is low level, however, the output from the TONE OUT pin is prohibited even if the key input is on. AKD is effective at that time. This pin is provided with the pull up resistance of 20K ~ 150K ohms internally. 
$\overline{\text{SYNGLE TONE INHIBIT}}$	15	When more than two columns are selected against only one row, or when more than 2 rows are selected against only one column, the single tone is output from the TONE OUT pin. This $\overline{\text{SINGLE TONE INHIBIT}}$ pin is a negative logic input pin to control the output of the TONE OUT pin in those cases. Refer to the Table 4. When the input to this pin is high level, both of the single tone and dual tone are output from the TONE OUT pin. When the input to this pin is low level, however, the single tone is prohibited to output from the TONE OUT pin and becomes DC level. This pin is provided with the pull up resistance of 20K ~ 150K ohms. 
TONE OUT	16	The low group frequency and the high group frequency selected by the keyboard are synthesized and output from this TONE OUT pin. Because the output form is the NPN open emitter style, the load resistance must be connected externally. It is same for the case of the single tone output. The output amplitude of the high group is bigger than that of the low group by 1 ~ 2 dB. The distortion of the dual tone is maximum 10%. 
V_{DD}, V_{SS}	1, 6	V_{DD} is a power supply pin. V_{SS} is a ground pin.

Note:

Table 1

Effective input		Nominal frequency	Tone output frequency	Accuracy	Remarks
(ROW)	$\overline{R1}$	697 Hz	699.1 Hz	+0.30 %	Low group
	$\overline{R2}$	770 Hz	766.2 Hz	-0.49 %	
	$\overline{R3}$	852 Hz	847.4 Hz	-0.54 %	
	$\overline{R4}$	941 Hz	948.0 Hz	+0.74 %	
(COLUMN)	$\overline{C1}$	1209 Hz	1215.9 Hz	+0.57 %	High group
	C2	1336 Hz	1331.7 Hz	-0.32 %	
	$\overline{C3}$	1477 Hz	1471.9 Hz	-0.35 %	
	$\overline{C4}$	1633 Hz	1645.0 Hz	+0.73 %	

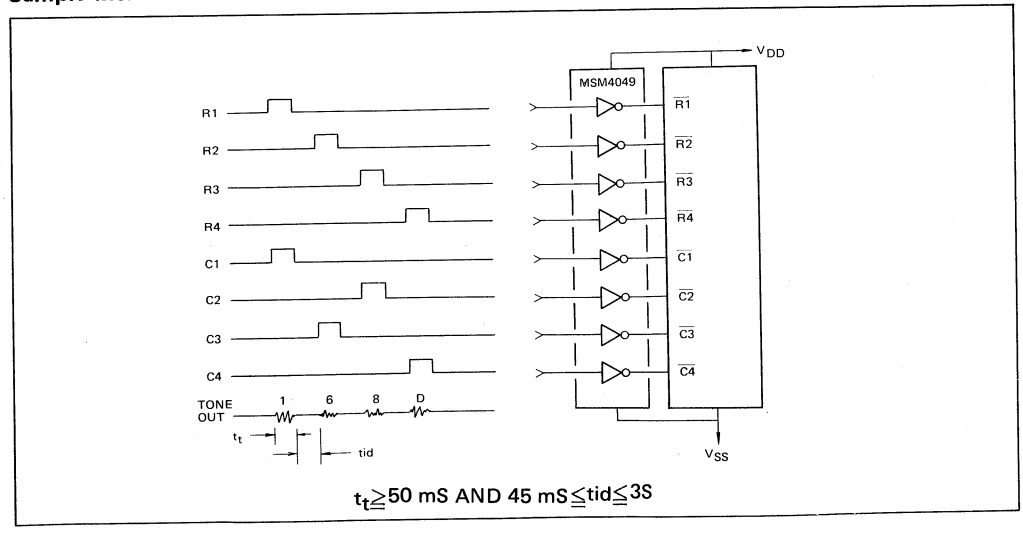
Table 2

Row input	Column input	Tone output*	Note
No	No	0V	
1	1	$f_L + f_H$	Dual tone
No	1	f_H	Single tone (Only column)
1	No	0V	
More than 2	No	0V	
More than 2	1	f_H	Single tone
No	More than 2	0V	
1	More than 2	f_L	Single tone
More than 2	More than 2	0V	

* The tone output shown is in the case when the load resistance is connected between the TONE OUT pin and the V_{SS}.

f_L: Low group f_H: High group

Sample interface circuit with microcomputer



$t_t \geqq 50$ mS AND 45 mS $\leqq$ tid $\leqq$ 3S

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Condition	Limit	Unit
Supply voltage	V_{DD}	Ta = 25°C	-0.3 ~ 9.5	V
Storage temperature	Tstg		-55 ~ +150	°C
Input voltage	V_I		GND-0.3~V_{DD}+0.3	V
Output voltage	V_O		GND-0.3~V_{DD}+0.3	V

Operating Range

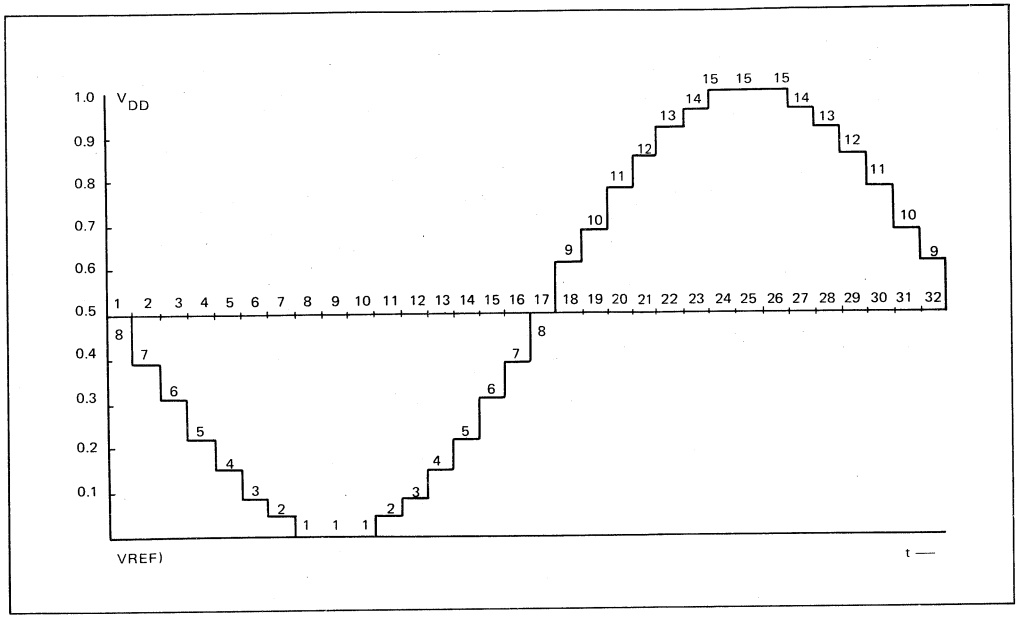
Parameter	Symbol	Condition	Limit	Unit
Supply voltage	V_{DD}	—	2.5 ~ 8.5	V
Operating temperature	T_{OP}	—	-30 ~ +70	°C

DC Characteristics

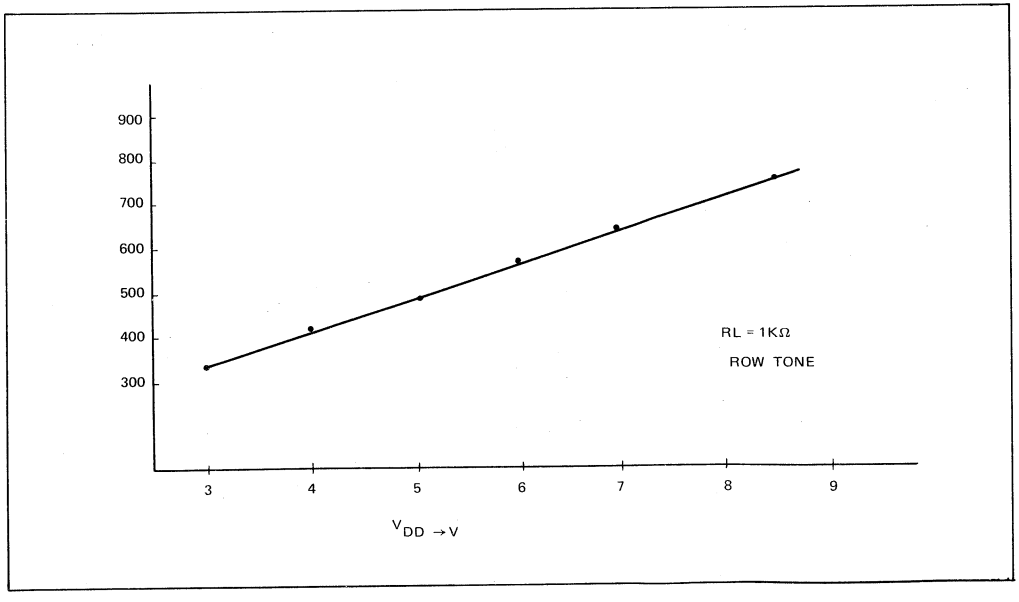
Parameter	Symbol	Conditions	Limit			Unit	Applicable pin
			Min	Typ	Max		
"H" input voltage	V_{IH}		0.7 V_{DD}		V_{DD}	V	$\overline{C1}$~$\overline{C4}$, $\overline{R1}$~$\overline{R4}$
"L" input voltage	V_{IL}		V_{SS}		0.3 V_{DD}	V	"
"L" input current	I_{IL}	V_{DD}=8.5V V_{IL}=0V	0.0567		0.425	mA	"
"H" input current	I_{IH}	V_{DD}=8.5V V_{IH}=10V			10	μA	"
"TONE OUT" output current	V_{OUT}	V_{DD}=3.0V R_L=1KΩ	235		437	mV rms	TONE OUT
Difference of high/ low band level	dB CR	V_{DD}=3.0 ~ 8.5V	1	1.5	2	dB	"
Distortion	% DIS	V_{DD}=3.0 ~ 8.5V			10	%	"
"H" input current	I_{IH}	V_{DD}=8.5V V_{IH}=8.5V			1	μA	$\overline{TONE}$ $\overline{DISABLE}$ $\overline{SIT}$*
"L" input current	I_{IL}	V_{DD}=8.5V V_{IL}=0V	0.0567		0.425	mA	"
"H" input voltage	V_{IH}		0.7 V_{DD}		V_{DD}	V	"
"L" input voltage	V_{IL}		V_{SS}		0.3 V_{DD}	V	"
Power consumption (Stand-by)	I_{DDS}	No load V_{DD}=8.5V Key-OFF			200	μA	"
Power consumption (Operating)	I_{DD}	No load V_{DD}=8.5V Key-ON			25	mA	
"L" output current	I_{OL}	V_{DD}=3V V_{OL}=0.5V	0.53	1.3		mA	$\overline{AKD}$
		V_{DD}=8.5V V_{OL}=0.5V	2.0	5.3			
"OFF" leak current	I_{OFF}				10	μA	$\overline{AKD}$
TONE OUT Rise Time	tRise	V_{DD}=3.0 ~ 8.5V		3.0	5.0	mA	TONE OUT

* $\overline{SIT}$ = $\overline{SINGLE\ TONE\ INHIBIT}$

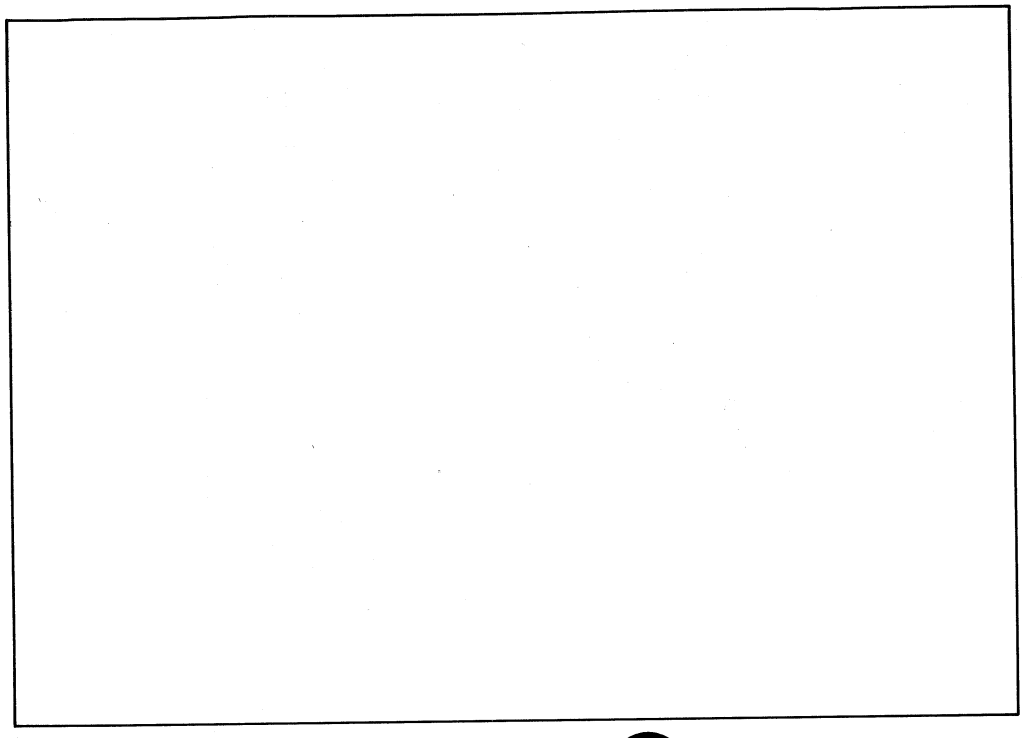
Sample Output Waveform of the Single Tone



Tone Amplitude (mV rms)

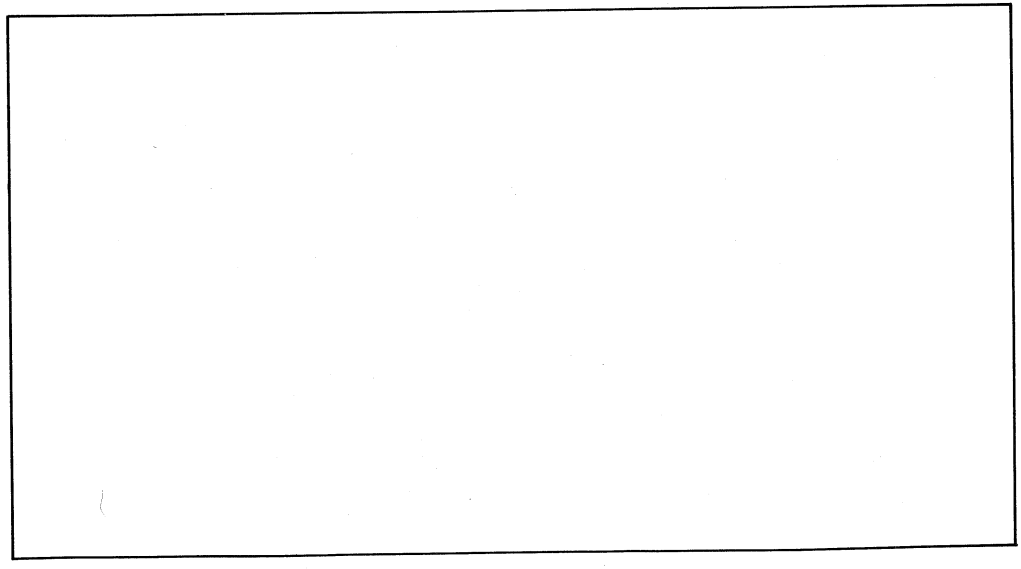


III



C. COMBO CODEC

III



OKI semiconductor

MSM6932 (μ-Law)/MSM6933 (A-Law)

SINGLE CHIP CODEC WITH FILTER (COMBO)

GENERAL DESCRIPTION

MSM6932 and MSM6933 are CMOS devices containing a companding CODEC and PCM filters on a single chip. It converts voice signals to PCM signals (μ-law or A-law) and vice versa. It contains analog pre-filter, transmit switched capacitor filter (SCF), receive SCF, analog post-filter and CODEC.

The transmit section and the receive section are designed to operate in both synchronous and asychronous applications.

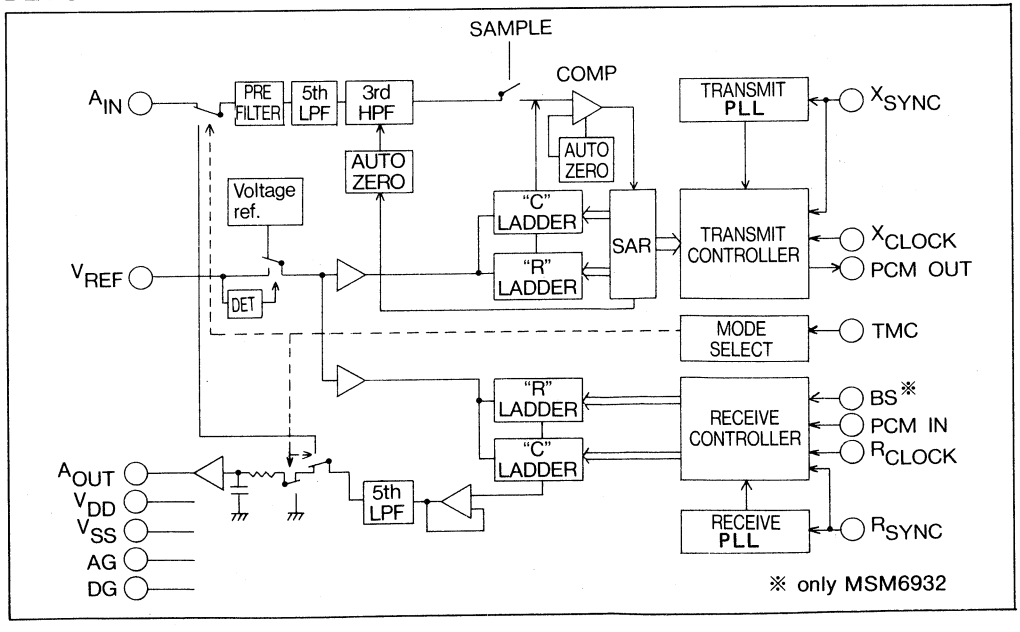
Each section requires sampling clock (8 kHz) and data clock (from 64 kHz to 2048 kHz) respectively.

FEATURES

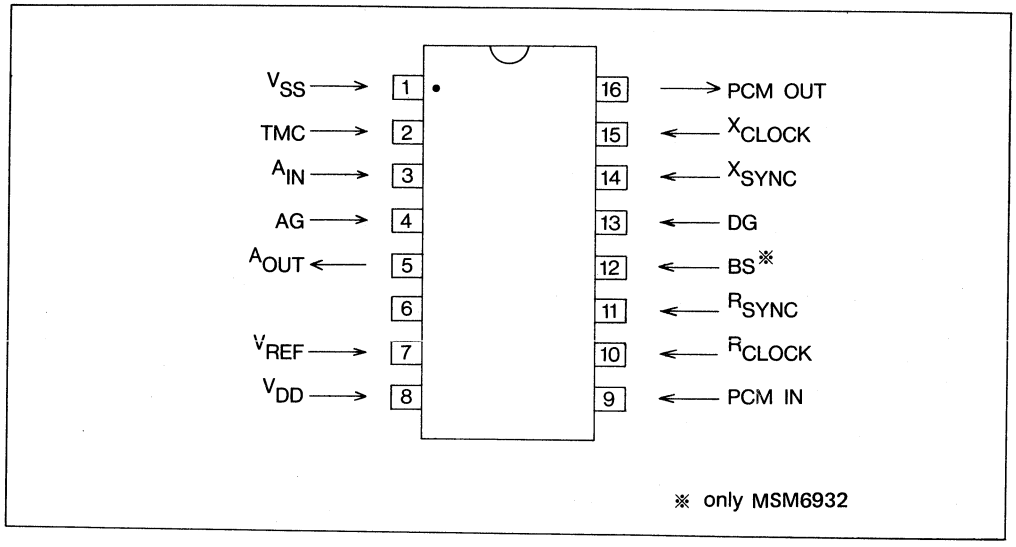
- Pre-channel Single Chip CODEC with Filters.
- ±5 V Power Supplies.
- Low Power Dissipation.
  65 mW operating (TYP)
  7 mW standby (TYP)
- Follows the μ-companding Law. (MSM-6932)
- Follows the A-companding Law. (MSM-6933)
- Synchronous or Asynchronous Operation.
- Serial Data Rate of 64KBPS to 2048-KBPS.
- On-chip Full Auto-ZERO Circuit.
- On-chip Analog Pre-Filter and Post-Filter.
- Excellent Power Supply Rejection Ratio
  25 dB (from 300 Hz to 300 kHz)
- On-chip Precision Voltage reference.

III

BLOCK DIAGRAM



PIN CONFIGURATION



III

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{DD}	-0.3 ~ +7	V
	V_{SS}	+0.3 ~ -7	V
Reference Voltage	V_{REF}	0 ~ V_{DD}	V
Analog Input Voltage	V_{AIN}	V_{SS} - 0.3 ~ V_{DD} + 0.3	V
Digital Input Voltage	V_{DIN}	-0.3 ~ V_{DD} + 0.3	V
Operating Temperature	T_{OP}	0 ~ 70	°C
Storage Temperature	T_{stg}	-55 ~ 150	°C

Recommended Operating Conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{DD}		4.75	5	5.25	V
	V_{SS}		-5.25	-5	-4.75	V
Reference Voltage	V_{REF}		—	2.5	—	V
Analog Input Voltage	V_{AIN}		$-V_{REF}$	—	$+V_{REF}$	V
Input High Voltage	V_{IH}	XSYNC, XCLOCK, PCM IN, RSYNC, RCLOCK, TMC, BS	2.0	—	V_{DD}	V
Input Low Voltage	V_{IL}		0	—	0.8	V
Clock Frequency	f_c	XCLOCK, RCLOCK	64	—	2048	kHz
Sync Pulse Frequency	f_s	XCLOCK, RSYNC	—	8	—	kHz
Clock Duty Ratio	D_R	XCLOCK, RCLOCK	—	50	—	%
Digital Input Rise Time	t_{Ir}	XSYNC, XCLOCK, PCM IN RSYNC, RCLOCK (Fig. 2)	—	—	50	ns
Digital Input Fall Time	t_{Ir}	XSYNC, XCLOCK, PCM IN RSYNC, RCLOCK (Fig. 2)	—	—	50	ns
XMIT. Sync Timing	t_{XS}	XCLOCK → XSYNC (Fig. 3)	50	—	—	ns
	t_{SX}	XSYNC → XCLOCK (Fig. 3)	150	—	—	ns
RCV. Sync Timing	t_{RS}	RCLOCK → RSYNC (Fig. 3)	50	—	—	ns
	t_{SR}	RSYNC → RCLOCK (Fig. 3)	100	—	—	ns
XMIT. Sync Pulse Width	t_{WX}	(Fig. 3)	1/fc	—	117	μs
RCV. Sync Pulse Width	t_{WR}	(Fig. 3)	1/fc	—	117	μs
PCM IN Set-up Time	t_{DS}	(Fig. 3)	100	—	—	ns
PCM IN Hold Time	t_{DH}	(Fig. 3)	100	—	—	ns
Analog Output Allowable Load	R_{AL}		10	—	—	kΩ
	C_{AL}		—	—	100	PF
Digital Output Allowable Load	R_{DL}		1	—	—	kΩ
	C_{DL}		—	—	100	PF
Operating Temperature	T_{OP}		0	—	70	°C

DC Characteristics

Parameter	Symbol	Condition		Min	Typ	Max	Unit
Supply Current (Operating)	I_{DD1}	V_{DD} = +5.25 V, V_{SS} = -5.25 V		—	—	11	mA
	I_{SS1}			—	—	11	mA
Supply Current (Stand-by)	I_{DD2}			—	1.0	3	mA
	I_{SS2}			—	0.3	1.5	mA
Reference Current	I_{REF}			—	—	100	μA
Input High Voltage	V_{IH}	V_{DD} = +5.25 V, V_{SS} = -5.25 V		2.0	—	—	V
Input Low Voltage	V_{IL}	V_{DD} = +4.75 V, V_{SS} = -4.75 V		—	—	0.8	V
Input Leakage Current	I_{IH}	V_{DD} = +5.25 V, V_{SS} = -5.25 V	V_I = 5 V	—	—	2.0	μA
	I_{IL}		V_I = 0 V	—	—	0.5	μA
Output Low Voltage	V_{OL}	V_{DD} = +4.75 V, V_{SS} = -4.75 V		—	—	0.4	V
Output Leakage Current	I_{OH}	V_{DD} = +5.25 V, V_{SS} = -5.25 V		—	—	10	μA
Input Capacitance	C_{IN}	Except for AIN		—	5	—	PF
		AIN		—	5	—	PF
Analog Input Resistance	R_{IN}	f_{IN} < 3.4 kHz		—	1	—	MΩ

AC Characteristics

Parameter	Symbol	Condition f (Hz)	Condition Level (dBmo)	Condition	Min	Typ	Max	Unit
XMIT FILTER Frequency Response	Loss S1	60	0	V_{DD} = +5 V, V_{SS} = -5 V	20	–	–	dB
	Loss S2	300	0		-0.1	–	0.2	dB
	Loss S3	810	0		Reference Value			
	Loss S4	2010	0		-0.1	–	0.2	dB
	Loss S5	3000	0		-0.1	–	0.2	dB
	Loss S6	3400	0		-0.1	–	0.8	dB
	Loss S7	4600	0		29	–	–	dB
RCV FILTER Frequency Response	Loss R1	300	0		-0.1	–	0.2	dB
	Loss R2	810	0		Reference Value			
	Loss R3	2010	0		-0.1	–	0.2	dB
	Loss R4	3000	0		-0.1	–	0.2	dB
	Loss R5	3400	0		-0.1	–	0.8	dB
	Loss R6	4600	0		29	–	–	dB
Total Frequency Response	Loss 1	60	0		20	–	–	dB
	Loss 2	300	0		-0.2	–	0.4	dB
	Loss 3	810	0		Reference Value			
	Loss 4	2010	0		-0.2	–	0.4	dB
	Loss 5	3000	0		-0.2	–	0.4	dB
	Loss 6	3400	0		-0.2	–	1.6	dB
Signal to Distortion Ratio (*1)	SD1	1020	3		36	–	–	dB
	SD2	1020	0		36	–	–	dB
	SD3	1020	-30		36	–	–	dB
	SD4	1020	-40		31	–	–	dB
	SD5	1020	-45		26	–	–	dB

*1: The measurement is taken with P-message filter.

III

Parameter	Symbol	Condition f (Hz)	Condition Level (dBmo)	Condition	Min	Typ	Max	Unit
Gain Tracking	GT1	1020	3	V_{DD} = +5 V, V_{SS} = -5 V	-0.4	—	0.4	dB
	GT2	1020	-10		Reference Gain Value			
	GT3	1020	-40		-0.4	—	0.4	dB
	GT4	1020	-50		-0.9	—	0.9	dB
	GT5	1020	-55		-2.9	—	2.9	dB
Idle Channel Noise *2	NIDL				—	—	-71	dBmOP
Absolute Delay Time					—	—	0.52	ms
Group Delay Time Frequency Response	t_{GD1}	500	0		—	—	1.5	ms
	t_{GD2}	600	0		—	—	0.75	ms
	t_{GD3}	1000	0		—	—	0.25	ms
	t_{GD4}	2600	0		—	—	0.25	ms
	t_{GD5}	2800	0		—	—	1.5	ms
Single Frequency Leakage Level	N1	8K			—	—	-50	dBmO
	N2	128K			—	—	-50	dBmO
Cross Talk Attenuation	C_R	810	0		66	—	—	dB
Digital Output Delay Time	t_{SD}			V_{DD} = +5 V, V_{SS} = -5 V, R_L = 2kΩ, C_L = 100PF	50	—	300	ns
	t_{XD1}				50	—	300	ns
	t_{XD2}				50	—	300	ns
	t_{XD3}				50	—	300	ns
Output Fall Time	t_{DOf}				—	—	100	ns
Absolute Gain *3	AVS	810	0	V_{DD} = +5 V, V_{SS} = -5 V	-0.5	0	0.5	dB
	AVR	810	0		-0.5	0	0.5	dB

*2: The measurement is taken with P-message filter.

*3: 0dB = 1.251 Vrms

PIN DESCRIPTION

<table>
<tr><th>Pin Name</th><th>Pin No.</th><th>Function</th></tr>
<tr><td>V_{SS}</td><td>1</td><td>V_{SS} is a negative supply pin. The voltage supplied to this pin should be −5 V ±5%.</td></tr>
<tr><td>TMC</td><td>2</td><td>Test mode control input pin.
TMC is a control input for operating mode selection, such as normal operating mode and analog loop-back mode.
The operating modes are listed in the following table.
<table>
<tr><th>"TMC"</th><th>Mode</th><th>"AOUT"</th><th>"AIN"</th></tr>
<tr><td>V_{IH}
(2.0 V ~ V_{DD})</td><td>Operating</td><td>Receive Signal Output Connected to $RCVF_{IL}$ Output</td><td>Xmit Signal Input</td></tr>
<tr><td>V_{IL}
(0 ~ 0.8 V)</td><td>Analog Loop Back (Refer to Fig. 1)</td><td>0 V</td><td>Disconnected</td></tr>
</table></td></tr>
<tr><td>AIN</td><td>3</td><td>A_{IN} is an analog signal input pin and is normally connected to the transmit filter input. The input analog signal is bandwidth-limited to 3.4 kHz and is converted to the 8 bits PCM signal.
The input analog signal must remain between + V_{REF} and − V_{REF} for accurate conversion.
In the analog loop-back mode, this pin is disconnected from any other circuits.</td></tr>
<tr><td>AG</td><td>4</td><td>Analog ground pin.
AG is connected to the analog system ground.</td></tr>
<tr><td>A_{OUT}</td><td>5</td><td>A_{OUT} is an analog signal output pin and is connected to the receive filter output. The output voltage range is ±2.5 V.</td></tr>
<tr><td>(NC)</td><td>6</td><td></td></tr>
<tr><td>V_{REF}</td><td>7</td><td>V_{REF} is an input of the external voltage reference. This pin is left in open or connected to AG to activate the internal voltage reference.</td></tr>
<tr><td>V_{DD}</td><td>8</td><td>V_{DD} is a positive supply pin. The voltage supplied to this pin should be + 5V ±5%.</td></tr>
<tr><td>PCM_{IN}</td><td>9</td><td>PCM_{IN} is an input pin of the PCM signal. This signal is serial data and is converted to the analog signal under control of R_{SYNC} and R_{CLOCK}. The input PCM data rates range from 64KBPS to 2048KBPS.</td></tr>
<tr><td>R_{CLOCK}</td><td>10</td><td>R_{CLOCK} is an input pin of the clock that provides the basic timing and control signals required for the input of the PCM signal.
The frequency of this clock must be coincident with the input PCM data rate.</td></tr>
</table>

Pin Name	Pin No.	Function
RSYNC	11	R_{SYNC} is an input pin of the pulse signal that is synchronized with R_{CLOCK} and is used for taking out the required signal from the input serial PCM data. This signal makes the whole operation in the receive section synchronized. When R_{SYNC} is connetected continuously low or continuously high, the receive section is powered down. The frequency of this signal is 8 kHz ± 50 ppm.
BS	12	7 bits control input pin. In the normal mode and the analog loop back mode, a positive or negative transient of BS signsl provides a 7 bits decode operation with MSM6932. (Refer to Fig. 4)
DG	13	Digital ground pin. DG is connected to the digital system ground.
X_{SYNC}	14	X_{SYNC} is an input pin of the pulse signal that is synchronized with X_{CLOCK} and makes the operation in the transmit section synchronized. The output signal from the PCM_{OUT} pin is naturally synchronized with this signal. When X_{SYNC} is connected continuously low or continuously high, the transmit section is powered down. The frequency of this signal is 8 kHz ± 50 ppm.
X_{CLOCK}	15	X_{CLOCK} is an input pin of the clock that provides the basic timing and control signals required for the output of PCM signal. Clock rates of 64 kHz ~ 2048 kHz can be used for X_{CLOCK}.
PCM_{OUT}	16	PCM_{OUT} is an output pin of the PCM signal. The result of conversion from analog to digital is output from this pin as 8 bits serial data. This data is shifted out under control of X_{SYNC} and X_{CLOCK}. Because of an open-drain output, wired-OR connections are easily performed.

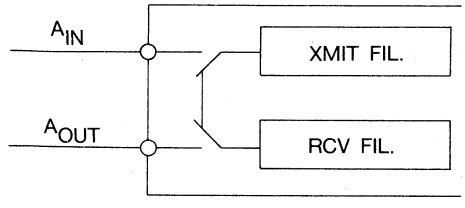
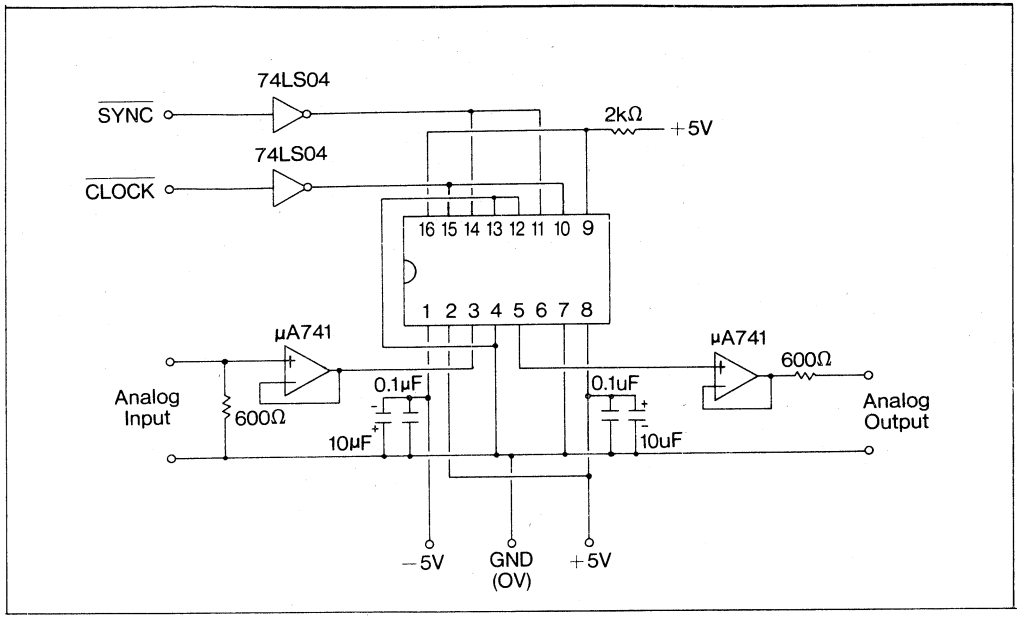


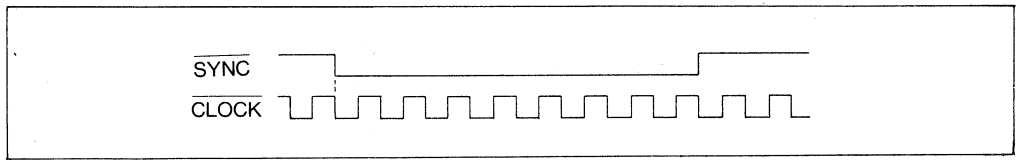
Figure 1

Note: A positive or negative transient of BS signal provides a 7 bits decode operation. (Refer to Fig. 4)
This pin is not connected to internal circuits with MSM6933.

TEST CIRCUIT



Note 1: $\overline{\text{SYNC}}$ and $\overline{\text{CLOCK}}$ timing.



Note 2: Make the connection wire between No. 4 pin and No. 13 pin as short as possible.
Note 3: Use a test socket with short leads.

III

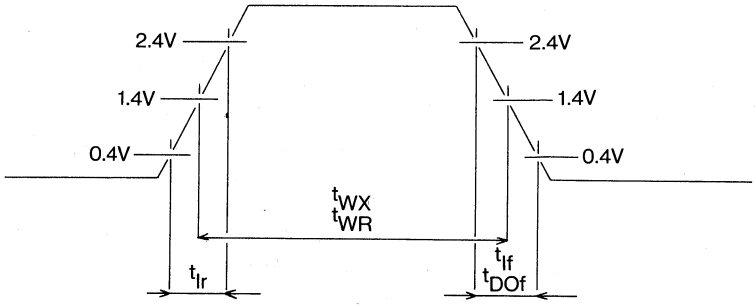


Figure 2 Definitions of Rise Time and Fall Time

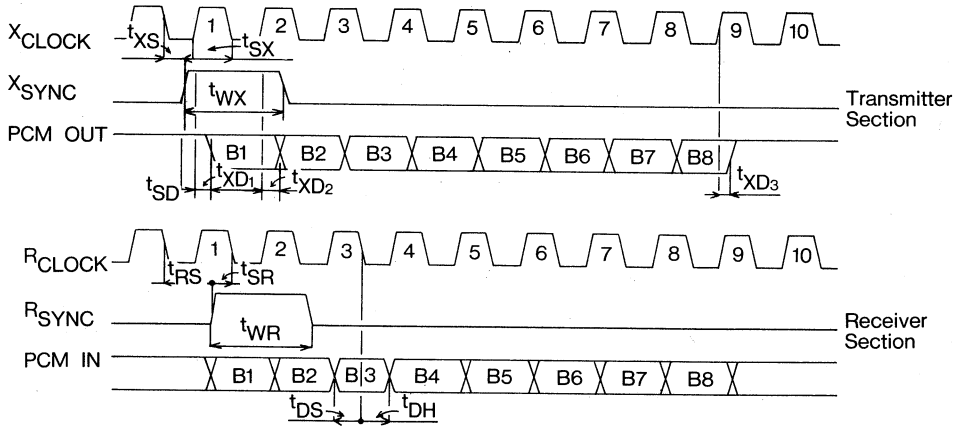


Figure 3 Basic Time Chart

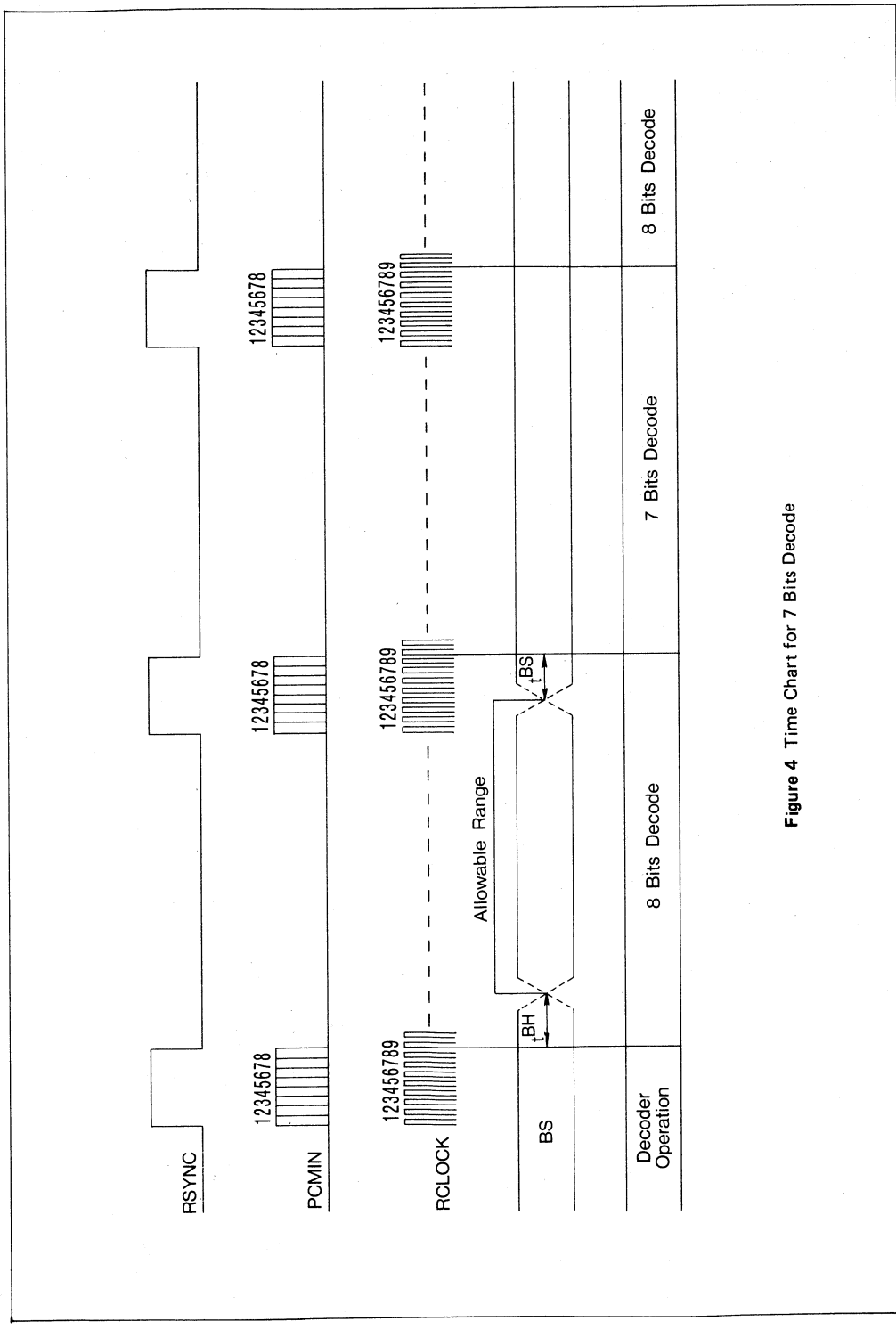


Figure 4 Time Chart for 7 Bits Decode

III

MSM6962/6982(μ-Law)
MSM6963/6983(A-Law)

SINGLE CHIP CODEC WITH FILTER (COMBO)

GENERAL DESCRIPTION

MSM6962, MSM6982, MSM6963 and MSM6983 are CMOS devices containing a companding CODEC and PCM filters on a single chip. It converts voice signals to PCM signals (μ-law or A-law) and vice versa. It contains analog pre-filter, transmit switched capacitor filter (SCF), receive SCF, analog post-filter and CODEC.

The transmit section and the receive section are designed to operate in both synchronous and asychronous applications.

Each section requires sampling clock (8 kHz) and data clock (512 kHz, 1024 kHz, 1536 kHz, 1544 kHz or 2048 kHz) respectively.

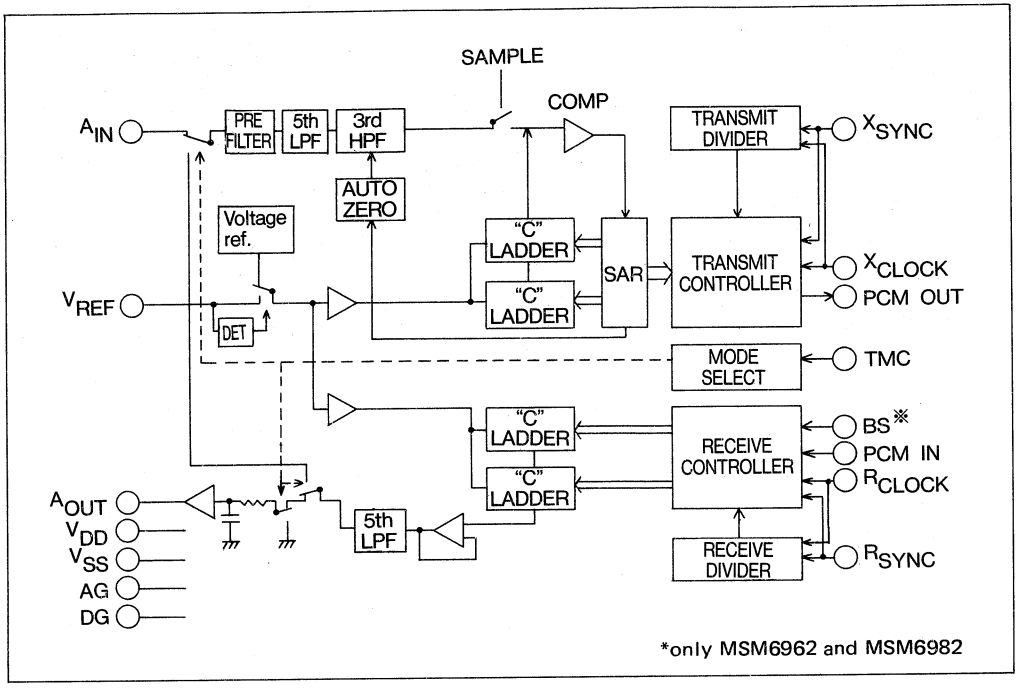
FEATURES

- Per-channel Single Chip CODEC with Filters.
- ±5 V Power Supplies
- Low Power Dissipatoin
  55 mW operating (TYP)
  4 mW standby (TYP)
- Follows the μ-companding Law. (MSM-6962 and MSM6982)
- Follows the A-companding Law. (MSM-6963 and MSM6983)
- Synchronous or Asynchronous Operation.
- Serial Data Rate of 512KBPS, 1024-KBPS, 1536KBPS, 1544KBPS or 2048-KBPS.
- On-chip Full Auto-ZERO Circuit.
- On-chip Analog Pre-Filter and Post-Filter.
- Excellent Power Supply Rejection Ratio
  30 dB (from 300 Hz to 300 kHz)
- On-chip Precision Voltage reference.

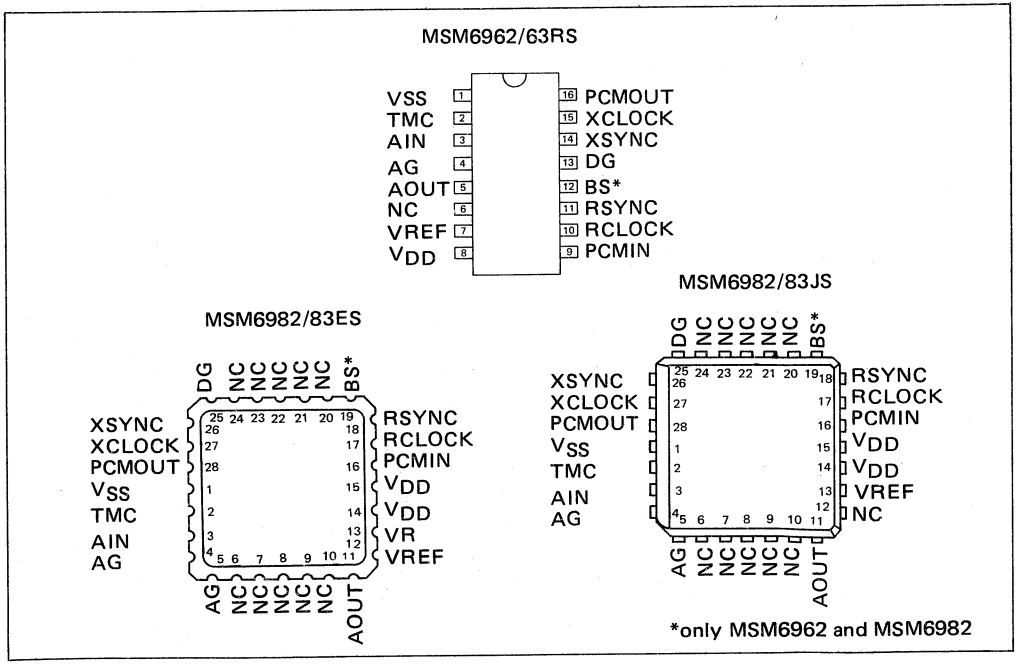
PACKAGE VARIETY

μ-Law	A-Law	Package	No. of Pin
MSM6962RS	MSM6963RS	Plastic DIP	16
MSM6982JS	MSM6983JS	PLCC	28
MSM6982ES	MSM6983ES	LCC	28

BLOCK DIAGRAM



PIN CONFIGURATION



ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{DD}	-0.3 ~ +7	V
	V_{SS}	+0.3 ~ -7	V
Reference Voltage	V_{REF}	0 ~ V_{DD}	V
Analog Input Voltage	V_{AIN}	V_{SS} - 0.3 ~ V_{DD} + 0.3	V
Digital Input Voltage	V_{DIN}	-0.3 ~ V_{DD} + 0.3	V
Operating Temperature	T_{OP}	-10 ~ 80	°C
Storage Temperature	T_{stg}	-55 ~ 150	°C

Recommended Operating Conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{DD}		4.75	5	5.25	V
	V_{SS}		-5.25	-5	-4.75	V
Reference Voltage	V_{REF}		—	2.5	—	V
Analog Input Voltage	V_{AIN}		$-V_{REF}$	—	$+V_{REF}$	V
Input High Voltage	V_{IH}	XSYNC, XCLOCK, PCM IN, RSYNC, RCLOCK, TMC, BS	2.0	—	V_{DD}	V
Input Low Voltage	V_{IL}		0	—	0.8	V
Clock Frequency	f_c	XCLOCK, RCLOCK	512, 1024 1536, 1544, 2048			kHz
Sync Pulse Frequency	f_s	XCLOCK, RSYNC	—	8	—	kHz
Clock Duty Ratio	D_R	XCLOCK, RCLOCK	40	50	60	%
Digital Input Rise Time	t_{lr}	XSYNC, XCLOCK, PCM IN RSYNC, RCLOCK (Fig. 2)	—	—	50	ns
Digital Input Fall Time	t_{lr}	XSYNC, XCLOCK, PCM IN RSYNC, RCLOCK (Fig. 2)	—	—	50	ns
XMIT. Sync Timing	t_{XS}	XCLOCK → XSYNC (Fig. 3)	50	—	—	ns
	t_{SX}	XSYNC → XCLOCK (Fig. 3)	150	—	—	ns
RCV. Sync Timing	t_{RS}	RCLOCK → RSYNC (Fig. 3)	50	—	—	ns
	t_{SR}	RSYNC → RCLOCK (Fig. 3)	100	—	—	ns
XMIT. Sync Pulse Width	t_{WX}	(Fig. 3)	1/fc	—	117	μs
RCV. Sync Pulse Width	t_{WR}	(Fig. 3)	1/fc	—	117	μs
PCM IN Set-up Time	t_{DS}	(Fig. 3)	100	—	—	ns
PCM IN Hold Time	t_{DH}	(Fig. 3)	100	—	—	ns
Analog Output Allowable Load	R_{AL}		10	—	—	kΩ
	C_{AL}		—	—	100	PF
Digital Output Allowable Load	R_{DL}		1	—	—	kΩ
	C_{DL}		—	—	100	PF
Operating Temperature	T_{OP}		0	—	70	°C

DC Characteristics

Parameter	Symbol	Condition		Min	Typ	Max	Unit
Supply Current (Operating)	I_{DD1}	V_{DD} = +5.25 V, V_{SS} = -5.25 V		–	5.5	11	mA
	I_{SS1}			–	5.0	11	mA
Supply Current (Stand-by)	I_{DD2}			–	1.0	3	mA
	I_{SS2}			–	0.3	1.5	mA
Reference Current	I_{REF}			–	5	100	μA
Input High Voltage	V_{IH}	V_{DD} = +5.25 V, V_{SS} = -5.25 V		2.0	1.7	–	V
Input Low Voltage	V_{IL}	V_{DD} = +4.75 V, V_{SS} = -4.75 V		–	1.6	0.8	V
Input Leakage Current	I_{IH}	V_{DD} = +5.25 V, V_{SS} = -5.25 V	V_I = 5 V	–	< 0.5	2.0	μA
	I_{IL}		V_I = 0 V	–	< 0.5	0.5	μA
Output Low Voltage	V_{OL}	V_{DD} = +4.75 V, V_{SS} = -4.75 V		–	< 0.2	0.4	V
Output Leakage Current	I_{OH}	V_{DD} = +5.25 V, V_{SS} = -5.25 V		–	< 5	10	μA
Input Capacitance	C_{IN}	Except for AIN		–	5	–	PF
		AIN		–	5	–	PF
Analog Input Resistance	R_{IN}	f_{IN} < 3.4 kHz		–	1	–	MΩ

AC Characteristics

V_{DD} = +5 V ±5%, V_{SS} = -5 V ±5%, V_R = 0 V

Parameter	Symbol	Condition f (Hz)	Condition Level (dBmO)		Min	Typ	Max	Unit
Transmit Frequency Response	Loss T1	60	0		20	26	—	dB
	Loss T2	300			-0.1	-0.03	0.2	
	Loss T3	820			Reference Value			
	Loss T4	2020			-0.1	0.0	0.2	
	Loss T5	3000			-0.1	0.10	0.2	
	Loss T6	3400			0	0.45	0.8	
	Loss T7	3980			14	16	—	
Receive Frequency Response	Loss R1	300	0		-0.1	-0.02	0.2	dB
	Loss R2	820			Reference Value			
	Loss R3	2020			-0.1	0.0	0.2	
	Loss R4	3000			-0.1	0.10	0.2	
	Loss R5	3400			0	0.65	0.8	
	Loss R6	3980			14	16	—	
Transmit Signal to Distortion Ratio (*1)	SD T1	1020	3		36	43	—	dB
	SD T2		0		36	41	—	
	SD T3		-30		36	40	—	
	SD T4		-40	*2	31	34.5 / 33	—	
	SD T5		-45	*2	26	31 / 28.5	—	
Receive Signal to Distortion Ratio (*1)	SD R1	1020	3		36	44	—	dB
	SD R2		0		36	41	—	
	SD R3		-30		36	41	—	
	SD R4		-40	*2	31	35.5 / 35	—	
	SD R5		-45	*2	26	34 / 28.5	—	

*1 : The measurement is taken with P-message filter.

*2 : MSM6962 MSM6982 / MSM6963 MSM6983

Parameter		Symbol	Condition f (Hz)	Condition Level (dBmO)	Min	Typ	Max	Unit
Transmit Gain Tracking		GT T1	1020	3	-0.2	-0.01	0.2	dB
		GT T2		-10	Reference Value			
		GT T3		-40	-0.2	0.05	0.2	
		GT T4		-50	-0.4	0.25	0.4	
		GT T5		-55	-0.8	0.10	0.8	
Receive Gain Tracking		GT R1	1020	3	-0.2	0.02	0.2	
		GT R2		-10	Reference Value			
		GT R3		-40	-0.2	-0.05	0.2	
		GT R4		-50	-0.4	-0.16	0.4	
		GT R5		-55	-0.8	-0.13	0.8	
Idle Channel Noise *3	Transmit	N_{IDL} T		—	—	-89	-75	dBmOp
	Receive	N_{IDL} R	—	—	—	-89	-75	
Analog Input Level		V_{IN}	1020	0	1,182	1,252	1,326	Vrms
Analog Output Level		V_{OUT}	1020	0	1,182	1,252	1,326	Vrms
Absolute Delay Time		t_D	—	—	—	0.47	0.5	ms
Transmit Group Delay Time		t_{GD} T1	500	0	—	0.2	0.75	ms
		t_{GD} T2	600		—	0.1	0.35	
		t_{GD} T3	1000		—	0	0.125	
		t_{GD} T4	1800		Reference Value			
		t_{GD} T5	2600		—	0.05	0.125	
		t_{GD} T6	2800		—	0.07	0.75	
Receive Group Delay Time		t_{GD} R1	500	0	—	-0.02	0.75	ms
		t_{GD} R2	600		—	-0.02	0.35	
		t_{GD} R3	1000		—	0.03	0.125	
		t_{GD} R4	1800		Reference Value			
		t_{GD} R5	2600		—	0.07	0.125	
		t_{GD} R6	2800		—	0.10	0.75	

*3 : The measurement is taken with P-message filter.

Parameter		Symbol	Condition f (Hz)	Condition Level (dBmO)	Min	Typ	Max	Unit
Crosstalk	T to R	C_R T	1020	0	–	-90	-66	dBmO
	R to T	C_R R	1020		–	-78	-66	
Discrimination Against Out-of-Band Input Signals		DIS	4.6K ~ 72K	-25	30	32	–	dB
Spurious Out-of-band Signals at the Output		SO	300 ~ 3400	0	–	-33	-30	dBmO
Intermodulation		IMD 1	fa=470 fb=320	-4	–	-40	-38	dB
Spurious In-band Signals at the Output		SI	1020	0	–	-45	-40	dBmO
Single Frequency Noise		N_S	–	–	–	-60	-50	dBmO
V_{DD} PSRR	Transmit	PPSR T	0 ~ 300K	200 mVp-p	–	30	–	dB
	Receive	PPSR R			–	30	–	
V_{SS} PSRR	Transmit	NPSR T			–	30	–	dB
	Receive	NPSR R			–	30	–	
Digital Output Delay Time		t_{SD}	R pull = 1 kΩ C_L = 100 pF		50	150	200	ns
		t_{XD_1}			50	100	200	
		t_{XD_2}			50	100	200	
		t_{XD_3}			50	180	200	
Digital Output Fall Time		t_{DDf}			–	20	100	ns

PIN DESCRIPTION

<table>
<tr><th rowspan="2">Pin Name</th><th colspan="2">Pin No.</th><th rowspan="2">Function</th></tr>
<tr><th>RS</th><th>ES, JS</th></tr>
<tr><td>V_{SS}</td><td>1</td><td>1</td><td>V_{SS} is a negative supply pin. The voltage supplied to this pin should be -5 V ±5%.</td></tr>
<tr><td>TMC</td><td>2</td><td>2</td><td>Test mode control input pin.
TMC is a control input for operating mode selection, such as normal operating mode and analog loop-back mode.
The operating modes are listed in the following table.
<table>
<tr><th>"TMC</th><th>Mode</th><th>"AOUT"</th><th>AIN"</th></tr>
<tr><td>V_{IH} (2.0V ~ V_{DD})</td><td>Operating</td><td>Receive signal output Connected to to RCVFLI output</td><td>Xmit signal input</td></tr>
<tr><td>V_{IL} (0 ~ 0.8V)</td><td>Analog Loop back (Refer to Fig. 1)</td><td>ov</td><td>Disconnected</td></tr>
</table></td></tr>
<tr><td>AIN</td><td>3</td><td>3</td><td>AIN is a analog signal input pin and is normally connected to the transmit filter input. The input analog signal is bandwidth-limited to 3.4 kHz and is converted to the 8 bits PCM signal.
The input analog signal must remain between + VREF and - VREF for accurate conversion.
In the analog loop-back mode, this pin is disconnected from any other circuits.</td></tr>
<tr><td>AG</td><td>4</td><td>4, 5</td><td>Analog ground pin.
AG is connected to the analog system ground.</td></tr>
<tr><td>A_{OUT}</td><td>5</td><td>11</td><td>A_{OUT} is a analog signal output pin and is connected to the receive filter output.
The output voltage range is ±2.5 V.</td></tr>
<tr><td>V_{REF}</td><td>7</td><td>13</td><td>V_{REF} is an input pin of the external voltage reference. This pin is left in open or connected to AG to activate the internal voltage reference.</td></tr>
<tr><td>V_{DD}</td><td>8</td><td>14, 15</td><td>V_{DD} is a positive supply pin. The voltage supplied to this pin should be +5 ±5%.</td></tr>
<tr><td>PCM_{IN}</td><td>9</td><td>16</td><td>PCM_{IN} is an input pin of the PCM signal. This signal is serial data and is converted to the analog signal under control of R_{SYNC} and R_{CLOCK}. The input PCM data rates are 512KBPS, 1024KBPS, 1536KBPS, 1544KBPS or 2048KBPS.</td></tr>
</table>

Pin Name	Pin No.		Function
	RS	ES, JS	
R_{CLOCK}	10	17	R_{CLOCK} is an input pin of the clock that provides the basic timing and control signals required for the input of the PCM signal. The frequency of this clock must be coincident with the input PCM data rate.
R_{SYNC}	11	18	R_{SYNC} is an input pin of the pulse signal that is synchronized with R_{CLOCK} and is used for taking out the required signal from the input serial PCM data. This signal makes the whole operation in the receive section synchronized. When R_{SYNC} is connected continuously low or continuously high, the receive section is powered down. The frequency of this signal is 8 kHz ±50 ppm.
BS	12	19	7 bits control input pin. In the normal mode and the analog loop back mode, a positive or negative transient of BS signal provides a 7 bits decode operation with MSM6962 and MSM6982. (Refer to Fig. 4)
DG	13	25	Digital ground pin. DG is connected to the digital system ground.
X_{SYNC}	14	26	X_{SYNC} is an input pin of the pulse signal that is synchronized with X_{CLOCK} and makes the whole operation in the transmit section synchronized. The output signal from the PCM_{OUT} pin is naturally synchronized with this signal. When X_{SYNC} is connected continuously low or continuously high, the transmit section is powered down. The frequency of this signal is 8 kHz ±50 ppm.
X_{CLOCK}	15	27	X_{CLOCK} is an input pin of the clock that provides the basic timing and control signals required for the output of PCM signal. Clock rates of 512KBPS, 1024KBPS, 1536KBPS, 1544KBPS or 2048KBPS can be used for X_{CLOCK}.
PCM_{OUT}	16	28	PCM_{OUT} is an output pin of the PCM signal. The result of conversion from analog to digital is output from this pin as 8 bits serial data. This data is shifted out under control of X_{SYNC} and X_{CLOCK}. Because of an open-drain output, wired-OR connections are easily performed.

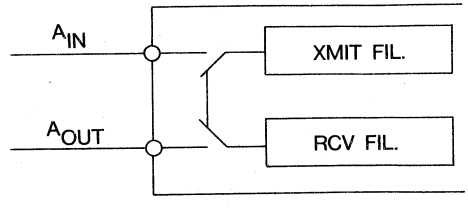
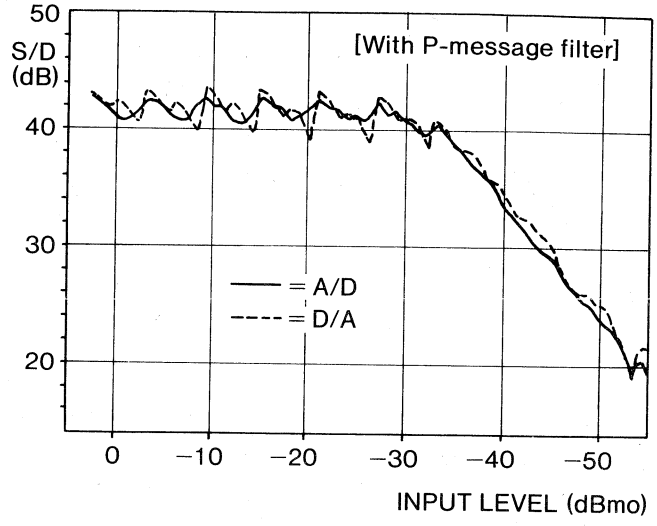


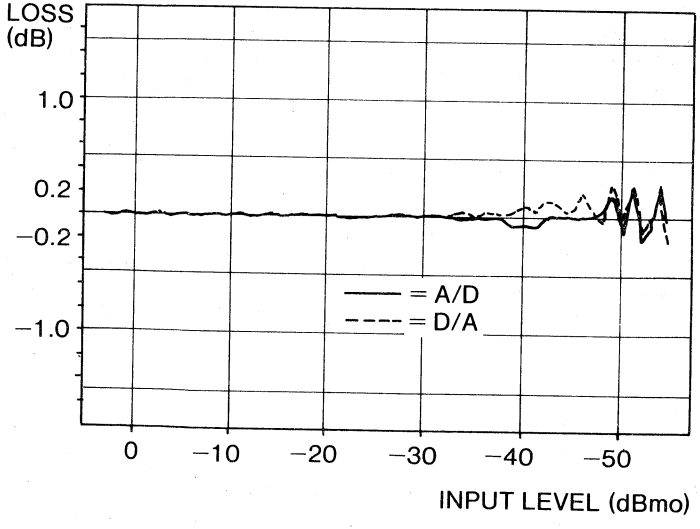
Figure 1

SIGNAL TO DISTORTION RATIO

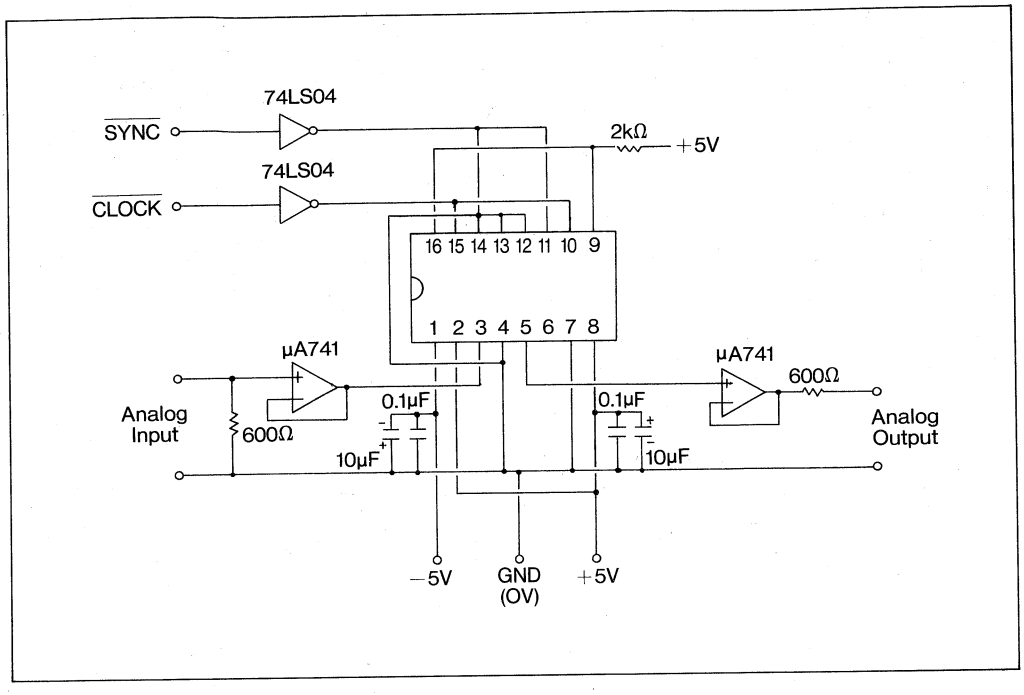


III

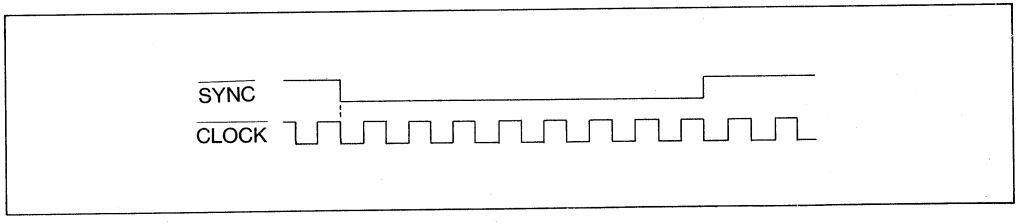
GAIN TRACKING CHARACTERISTICS



TEST CIRCUIT FOR MSM6962 AND MSM6963



Note 1: SYNC and CLOCK timing.



Note 2: Make the connection wire between AG and DG as short as possible.
Note 3: Use a test socket with short leads.

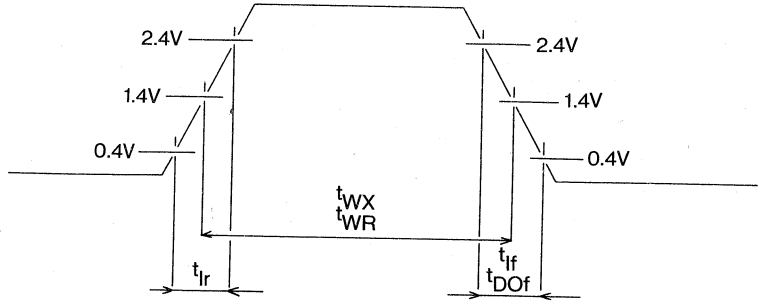


Figure 2 Definitions of Rise Time and Fall Time

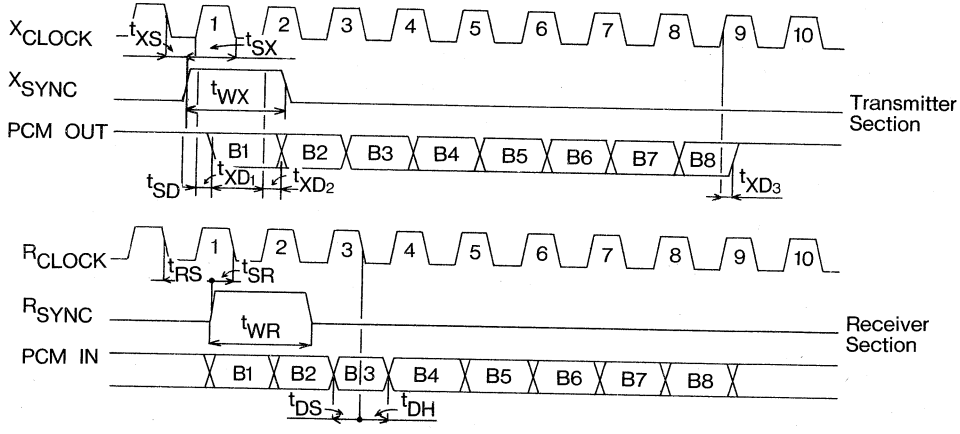


Figure 3 Basic Time Chart

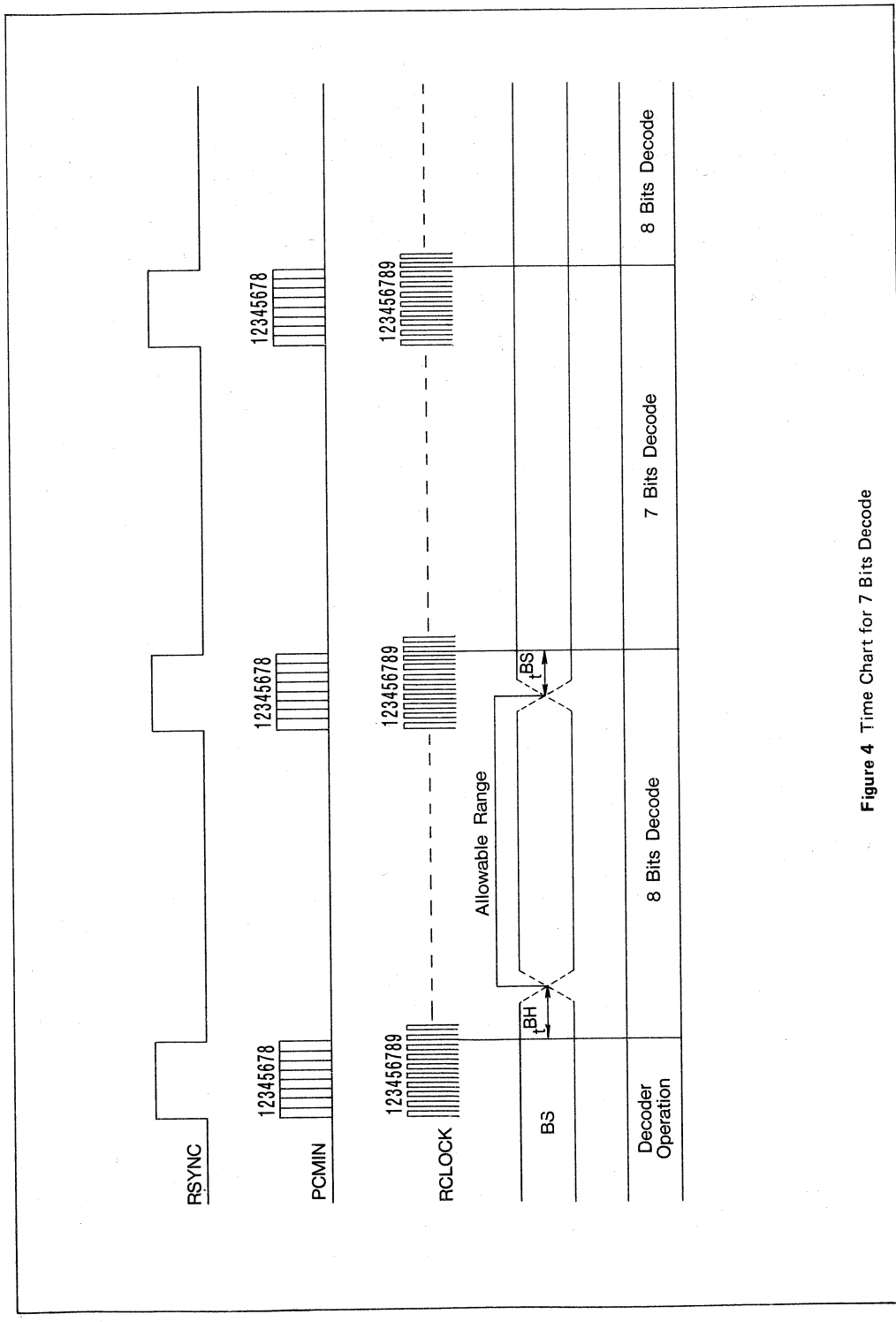


Figure 4 Time Chart for 7 Bits Decode

OKI semiconductor

MSM6996H/6996V/6998(A-Law)
MSM6997H/6997V/6999(μ-Law)

SINGLE CHIP CODEC WITH FILTER (COMBO)

GENERAL DESCRIPTION

MSM6996, MSM6997, MSM6998, MSM6999 are CMOS devices containing a companding CODEC and PCM filters on a single chip. It converts voice signals to PCM signals (μ-law or A-law) and vice versa. It contains analog pre-filter, transmit switched capacitor filter (SCF), receive SCF, analog post-filter and CODEC.

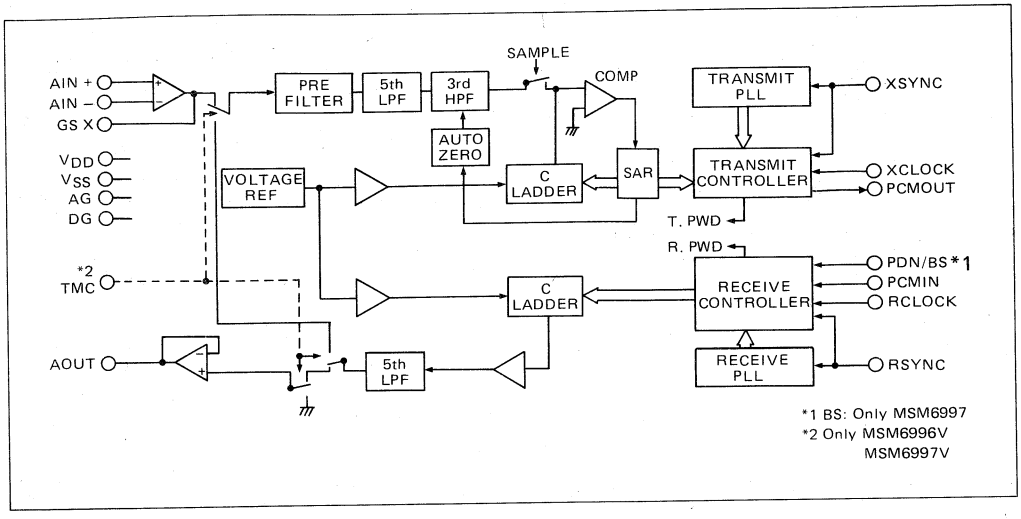
The transmit section and the receive section are designed to operate in both synchronous and asynchronous applications.

Each section requires sampling clock (8 kHz) and data clock (64 ~ 2048 kHz) respectively.

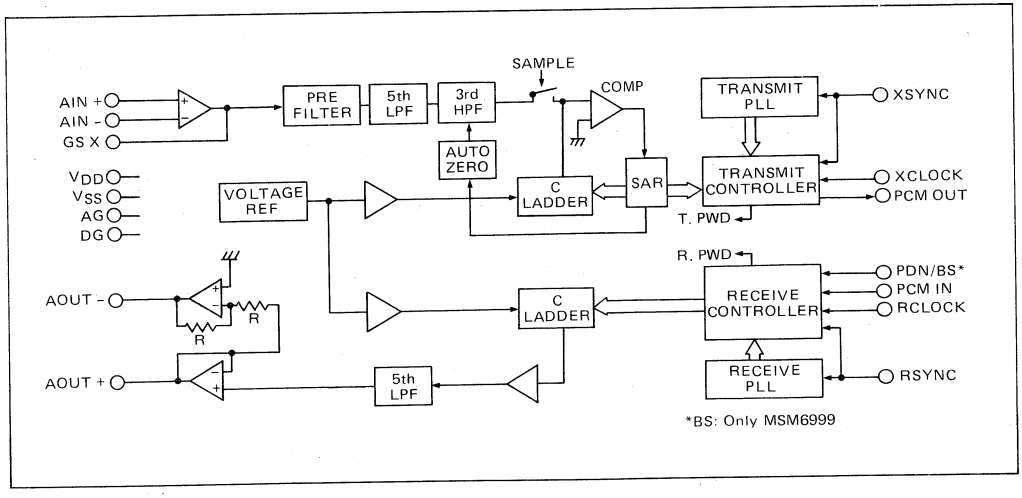
FEATURES

- Per-channel Single Chip CODEC with Filters.
- ±5 V Power Supplies.
- Low Power Dissipation.
  70 mW operating (TYP)
  5 mW standby (TYP)
- Follows the A-companding Law (MSM-6996, MSM6998)
- Follows the μ-companding Law (MSM-6997, MSM6999)
- Synchronous or Asynchronous Operation.
- 600 Ω drive (MSM6996, MSM6997)
- 600 Ω push-pull drive (MSM6998, MSM-6999)
- Serial Data Rate Range: 64K BPS ~ 2048 K BPS.
- On-chip Full Auto-ZERO Circuits and PLLs.
- On-chip Analog Pre-Filter and Post-Filter.
- Excellent Power Supply Rejection Ratio 30 dB (from 300 Hz to 300 kHz)
- On-chip Precision Voltage reference.
- Transmit level adjust.
- Standard 16 pin Package (ceramic or plastic)

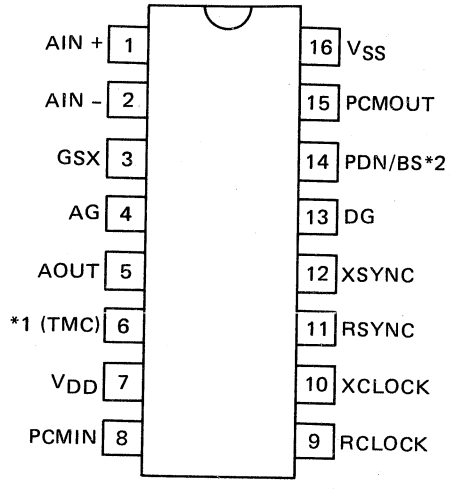
BLOCK DIAGRAM (MSM6996H/MSM6996V/MSM6997H/MSM6997V)



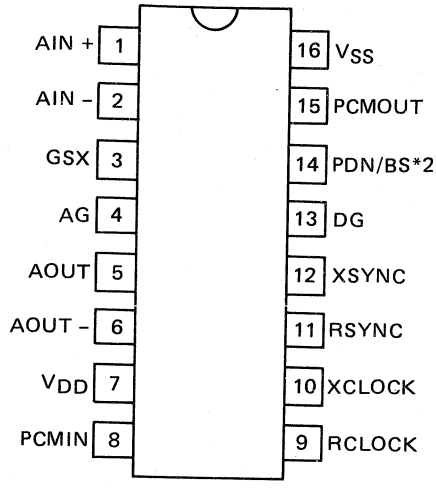
BLOCK DIAGRAM (MSM6998/MSM6999)



PIN CONFIGURATION



MSM6996H/MSM6996V
MSM6997H/MSM6997V



MSM6998
MSM6999

*1. Only MSM6996V/MSM6997V
*2. BS: Only MSM6997/MSM6999

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{DD}	− 0.3 ~ + 7	V
	V_{SS}	+ 0.3 ~ − 7	V
Analog Input Voltage	V_{AIN}	V_{SS} − 0.3 ~ V_{DD} + 0.3	V
Digital Input Voltage	V_{DIN}	− 0.3 ~ V_{DD} + 0.3	V
Operating Temperature	T_{OP}	− 10 ~ + 80	°C
Storage Temperature	T_{stg}	− 55 ~ 150	°C

Recommended Operating Conditions

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	–	4.75	5	5.25	V
	V_{SS}	–	-5.25	-5	-4.75	V
Analog Input Voltage	V_{AIN}	–	-2.5	–	+2.5	V
Input High Voltage	V_{IH}	XSYNC, XCLOCK, PCM IN, RSYNC, RCLOCK, TMC, BS	2.0	–	V_{DD}	V
Input Low Voltage	V_{IL}		0	–	0.8	V
Clock Frequency	f_c	XCLOCK, RCLOCK	64	–	2048	kHz
Sync Pulse Frequency	f_s	XSYNC, RSYNC	–	8	–	kHz
Clock Duty Ratio	D_R	XCLOCK, RCLOCK	40	50	60	%
Digital Input Rise Time	t_{lr}	XSYNC, XCLOCK, PCM IN RSYNC, RCLOCK (Fig. 2)	–	–	50	ns
Digital Input Fall Time	t_{lf}	XSYNC, XCLOCK, PCM IN RSYNC, RCLOCK (Fig. 2)	–	–	50	ns
XMIT. Sync Timing	t_{XS}	XCLOCK → XSYNC (Fig. 3)	50	–	–	ns
	t_{SX}	XSYNC → XCLOCK (Fig. 3)	150	–	–	ns
RCV. Sync Timing	t_{RS}	RCLOCK → RSYNC (Fig. 3)	50	–	–	ns
	t_{SR}	RSYNC →RCLOCK (Fig. 3)	100	–	–	ns
XMIT. Sync Pulse Width	t_{WX}	(Fig. 3)	1/fc	–	117	μs
PCV. Sync Pulse Width	t_{WR}	(Fig. 3)	1/fc	–	117	μs
PCM IN Set-up Time	t_{DS}	(Fig. 3)	100	–	–	ns
PCM IN Hold Time	t_{DH}	(Fig. 3)	100	–	–	ns
Analog Output Allowable Load	R_{AL}	–	600	–	–	Ω
	C_{AL}	–	–	–	100	pF
Digital Output Allowable Load	R_{DL}	–	1	–	–	kΩ
	C_{DL}	–	–	–	100	pF
Operating Temperature	T_{OP}	–	0	–	70	°C

DC Characteristics

Parameter	Symbol	Condition		Min	Typ	Max	Unit
Supply Current (Operating)	I_{DD1}	V_{DD} = +5.25 V, V_{SS} = -5.25 V		–	–	11	mA
	I_{SS1}			–	–	11	mA
Supply Current (Stand-by)	I_{DD2}			–	1.3	3	mA
	I_{SS2}			–	0.3	1.5	mA
Input High Voltage	V_{IH}	V_{DD} = +5.25V, V_{SS} = -5.25 V		2.0	–	–	V
Input Low Voltage	V_{IL}	V_{DD} = +4.75 V, V_{SS} = -4.75 V		–	–	0.8	V
Input Leakage Current	I_{IH}	V_{DD} = +5.25 V, V_{SS} = -5.25 V	V_I = 5 V	–	–	2.0	μA
	I_{IL}		V_I = 0 V	–	–	0.5	μA
Output Low Voltage	V_{OL}	V_{DD} = +4.75 V, V_{SS} = -4.75 V		–	–	0.4	V
Output Leakage Current	I_{OH}	V_{DD} = +5.25 V, V_{SS} = -5.25 V		–	–	10	μA
Input Capacitance	C_{IN}	Except for AIN		–	5	–	pF
		AIN		–	5	–	pF
Analog Input Resistance	R_{IN}	–		–	1	–	MΩ

AC Characteristics

Parameter	Symbol	Condition f (Hz)	Condition Level (dBmO)	Min	Typ	Max	Unit
Transmit Frequency Response	Loss T_1	60	0	20	–	–	dB
	Loss T_2	300		-0.1	–	0.2	
	Loss T_3	820		Reference Value			
	Loss T_4	2020		-0.1	–	0.2	
	Loss T_5	3000		-0.1	–	0.2	
	Loss T_6	3400		0	–	0.8	
	Loss T_7	3980		14	–	–	
Receive Frequency Response	Loss R_1	300	0	-0.1	–	0.2	dB
	Loss R_2	820		Reference Value			
	Loss R_3	2020		-0.1	–	0.2	
	Loss R_4	3000		-0.1	–	0.2	
	Loss R_5	3400		0	–	0.8	
	Loss R_6	3980		14	–	–	
Transmit Signal to Distortion Ratio (*1)	SD T_1	1020	3	36	–	–	dB
	SD T_2		0	36	–	–	
	SD T_3		-30	36	–	–	
	SD T_4		-40	31	–	–	
	SD T_5		-45	26	–	–	
Receive Signal to Distortion Ratio (*1)	SD R_1	1020	3	36	–	–	dB
	SD R_2		0	36	–	–	
	SD R_3		-30	36	–	–	
	SD R_4		-40	31	–	–	
	SD R_5		-45	26	–	–	

*1: The measurement is taken with P-message filter.

Parameter		Symbol	Condition f (Hz)	Condition Level (dBmO)	Min	Typ	Max	Unit
Transmit Gain Tracking		GT T_1	1020	3	-0.2	–	0.2	dB
		GT T_2		-10	Reference Value			
		GT T_3		-40	-0.2	–	0.2	
		GT T_4		-50	-0.4	–	0.4	
		GT T_5		-55	-0.8	–	0.8	
Receive Gain Tracking		GT R_1	1020	3	-0.2	–	0.2	dB
		GT R_2		-10	Reference Value			
		GT R_3		-40	-0.2	–	0.2	
		GT R_4		-50	-0.4	–	0.4	
		GT R_5		-55	-0.8	–	0.8	
Idle Channel Noise *2	Transmit	N_{IDL} T	–	–	–	–	-75	dBmOp
	Receive	N_{IDL} R	–	–	–	–	-75	
Analog Input Level *3		V_{IN}	1020	0	1,189/1,185	1,231/1,227	1,274/1,270	Vrms
Analog Output Level *3		V_{OUT}	1020	0	1,189/1,185	1,231/1,227	1,274/1,270	Vrms
Absolute Delay Time		tD	–	–	–	–	0.5	ms
Transmit Group Delay Time		tGD T_1	500	0	–	–	0.75	ms
		tGD T_2	600		–	–	0.35	
		tGD T_3	1000		–	–	0.125	
		tGD T_4	1800		Reference Value			
		tGD T_5	2600		–	–	0.125	
		tGD T_6	2800		–	–	0.75	
Receive Group Delay Time		tGD R_1	500	0	–	–	0.75	ms
		tGD R_2	600		–	–	0.35	
		tGD R_3	1000		–	–	0.125	
		tGD R_4	1800		Reference Value			
		tGD R_5	2600		–	–	0.125	
		tGD R_6	2800		–	–	0.75	

*2: The measurement is taken with P-message filter.

*3: MSM6996 MSM6998 / MSM6997 MSM6999

III

Parameter		Symbol	Condition f (Hz)	Condition Level (dBmO)	Min	Typ	Max	Unit
Crosstalk	T to R	C_R T	1020	0	–	–	-66	dBmO
	R to T	C_R R	1020		–	–	-66	
Discrimination Against Out-of-band Input Signals		DIS	4.6K ~ 72K	-25	30	–	–	dB
Spurious Out-of-band Signals at the Output		SO	300 ~ 3400	0	–	–	-30	dBmO
Intermodulation		IMD 1	fa = 470 fb = 320	-4	–	–	-38	dB
Spurious In-band Signals at the Output		SI	1020	0	–	–	-40	dBmO
Single Frequency Noise		Ns	–	–	–	–	-50	dBmO
V_{DD} PSRR	Transmit	PPSR T	0 ~ 300K	200 mV_{p-p}	–	30	–	dB
	Receive	PPSR R			–	30	–	
V_{SS} PSRR	Transmit	NPSR T			–	30	–	dB
	Receive	NPSR R			–	30	–	
Digital Output Delay Time		t_{SD}	R pull = 1 KΩ C_L = 100 pF		50	–	200	ns
		t_{XD_1}			50	–	200	
		t_{XD_2}			50	–	200	
		t_{XD_3}			50	–	200	
Digital Output Fall Time		t_{DDf}			–	–	100	ns

PIN DESCRIPTION

<table>
<tr><th>Pin Name</th><th>Pin No.</th><th>Function</th></tr>
<tr><td>AIN +</td><td>1</td><td rowspan="3">These three pins are used for the transmit level adjustment. AIN+ is a Non-inverting Analog Input pin which is connected to the non-inverting input of a transmit amplifier.
AIN– is a Inverting Analog Input pin which is connected to the inverting input of the transmit amplifier.
GSX is a Tramsmit Amplifier Output Pin.</td></tr>
<tr><td>AIN –</td><td>2</td></tr>
<tr><td>GSX</td><td>3</td></tr>
<tr><td>AG</td><td>4</td><td>AG is a analog ground pin.
AG is connected to the analog system ground.</td></tr>
<tr><td>AOUT</td><td>5</td><td>AOUT is the analog signal output pin and is connected to the receive filter output. The output voltage range is ±2.5 V. This output can drive the impedance of 600 Ω.</td></tr>
<tr><td>TMC-
(MSM6996V
MSM6997V
only)</td><td>6</td><td>Test mode control input pin.
This is a control input pin for operating mode selection, such as normal operating mode and analog loop-back mode.
The operating modes are as follows.
<table>
<tr><th>"TMC"</th><th>Mode</th><th>"AOUT"</th><th>"AIN"</th></tr>
<tr><td>V_{IH}
(2.0 V ~ V_{DD})</td><td>Operating</td><td>Receive Signal Output Connected to RCV_{FIL} Output</td><td>Xmit Signal Input</td></tr>
<tr><td>V_{IL}
(0 ~ 0.8 V)</td><td>Analog Loop Back (Refer to Fig. 1)</td><td>0 V</td><td>Disconnected</td></tr>
</table></td></tr>
<tr><td>AOUT-
(MSM6998
MSM6999
only)</td><td>6</td><td>This is the inverting analog output pin. This output can drive the impedance of 600 Ω.</td></tr>
<tr><td>NC
(MSM6996H
MSM6997H
only)</td><td>6</td><td>As for MSM6996H and MSM6997H, this pin should be left open.</td></tr>
<tr><td>VDD</td><td>7</td><td>VDD is the positive power supply pin. The voltage supplied to this pin should be +5 V ±5%.</td></tr>
<tr><td>PCMIN</td><td>8</td><td>PCM signal input pin. This signal is serial data and is converted to the analog signal under control of RSYNC and RCLOCk. The input PCM data rate range is from 64KBPS to 2048KBPS.</td></tr>
</table>

III

<table>
<tr><th>Pin Name</th><th>Pin No.</th><th>Function</th></tr>
<tr><td>RCLOCK</td><td>9</td><td>Receive Clock Input pin. The clock that provides the basic timing and control signals required for the input of the PCM signal is input to this pin. The frequency of this clock must be coincident with the input PCM data rate.</td></tr>
<tr><td>XCLOCK</td><td>10</td><td>Transmit Clock Input pin. The clock that provides the basic timing and control required for the output of the PCM signal is input to this pin. The clock frequencies are from 64 kHz to 2048 kHz.</td></tr>
<tr><td>RSYNC</td><td>11</td><td>Receive Synchronous Signal Input pin. The pulse signal that is synchronized with RCLOCK and is used for taking out the required signal from the input serial PCM data is input to this pin. The signal makes the whole operation in the receive section synchronized. When RSYNC is connected continuously low or continuously high, the receive section is powered down.
The frequency of this signal is 8 kHz ±50 ppm.</td></tr>
<tr><td>XSYNC</td><td>12</td><td>Transmit Synchronous Signal Input pin. The pulse signal that is synchronized with XCLOCK and makes the whole operation in the transmit section synchronized, is input to this pin.
The output signal from the PCMOUT pin is naturally synchronized with this signal. When XSYNC is connected continuously low or continuously high, the transmit section is powered down. The frequency of this signal is 8 kHz ±50 ppm.</td></tr>
<tr><td>DG</td><td>13</td><td>Digital Ground level pin.
DG is connected to the digital system ground.</td></tr>
<tr><td>PDN/BS</td><td>14</td><td>Power Down Signal Input pin.
This is an input of the power-down control signal. When this input is held at low level more than 1 ms, the chip is put into the power-down mode. For the μ-law devices (MSM6997 and MSM6999), this pin also provides the half-bit decoder shift for the 7 bit decode operation according to alternating the state of the pin. Refer to Fig. 4.</td></tr>
<tr><td>PCMOUT</td><td>15</td><td>PCM Signal Output pin. Open-drain output of the PCM signal is output from this pin. The result of conversion from analog to digital is output from this pin as 8 bit serial data is shifted out under control of XSYNC and XCLOCK.
ENCODING FORMAT
<table>
<tr><th></th><th colspan="8">MSM6996, MSM6998</th><th colspan="8">MSM6997, MSM6999</th></tr>
<tr><th></th><th>B1</th><th>B2</th><th>B3</th><th>B4</th><th>B5</th><th>B6</th><th>B7</th><th>B8</th><th>B1</th><th>B2</th><th>B3</th><th>B4</th><th>B5</th><th>B6</th><th>B7</th><th>B8</th></tr>
<tr><td>VIN = +Full Scale</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>VIN = +0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>VIN = -0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>VIN = -Full Scale</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
</table></td></tr>
<tr><td>VSS</td><td>16</td><td>This is the negative power supply pin. The voltage supplied to this pin should be -5 V ±5%.</td></tr>
</table>

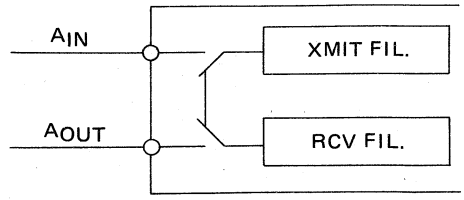
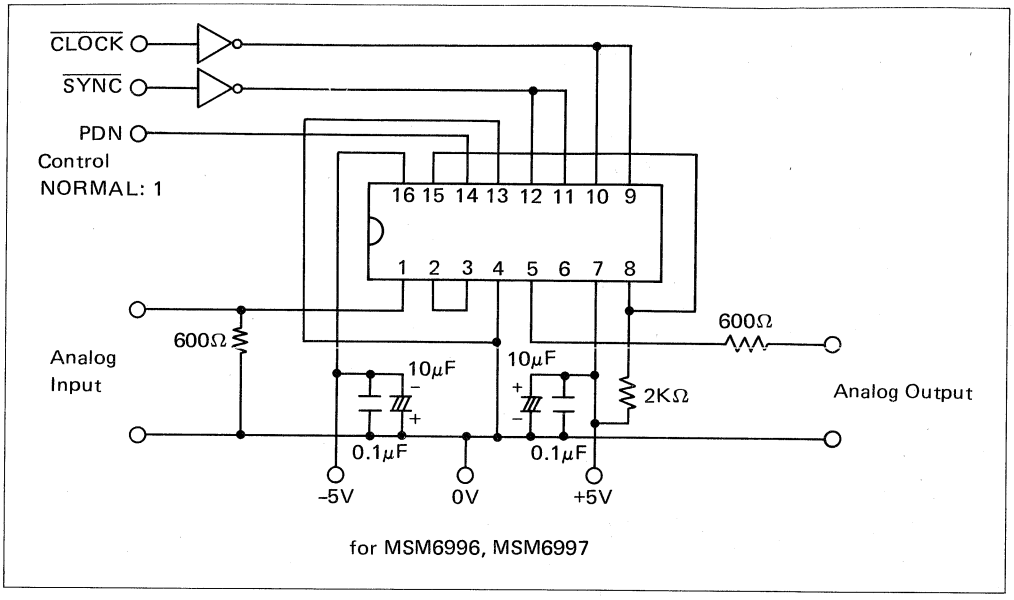
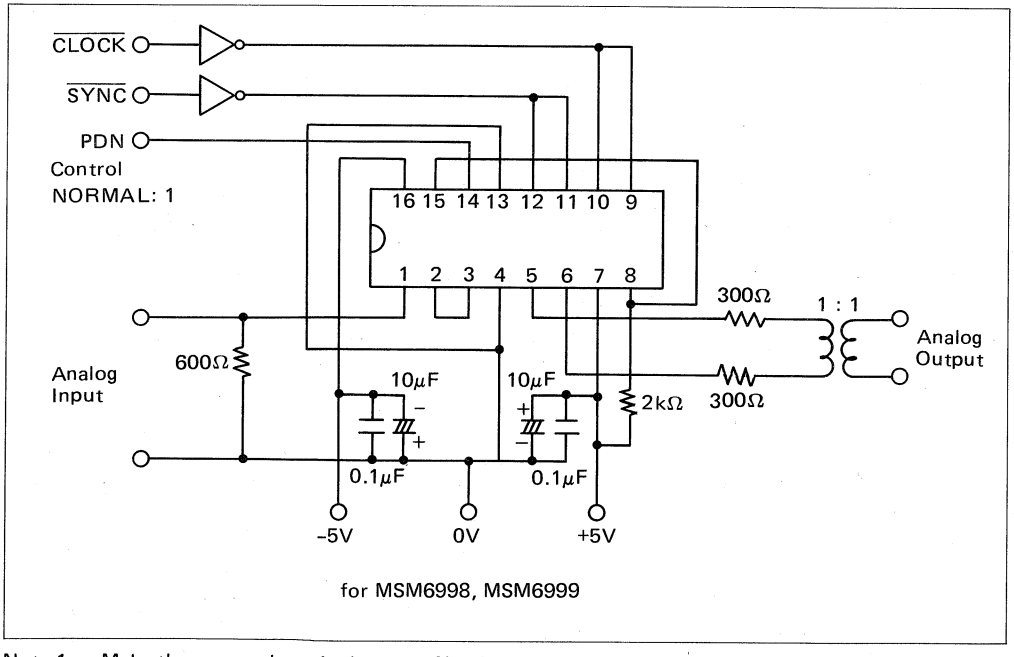


Figure 1

TEST CIRCUIT



for MSM6996, MSM6997



for MSM6998, MSM6999

Note 1 : Make the connection wire between No. 4 pin and No. 13 pin as short as possible.

Note 2 : Use a test socket with shor leads.

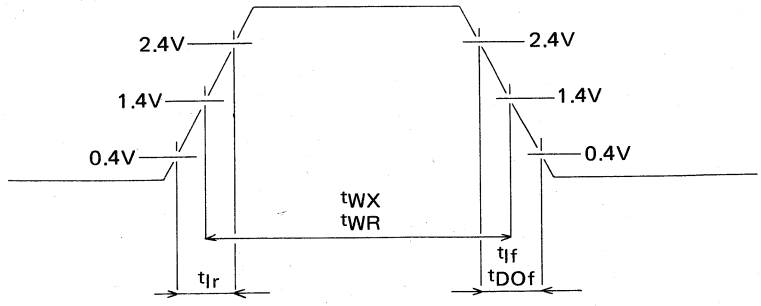


Figure 2 Definitions of Rise Time and Fall Time

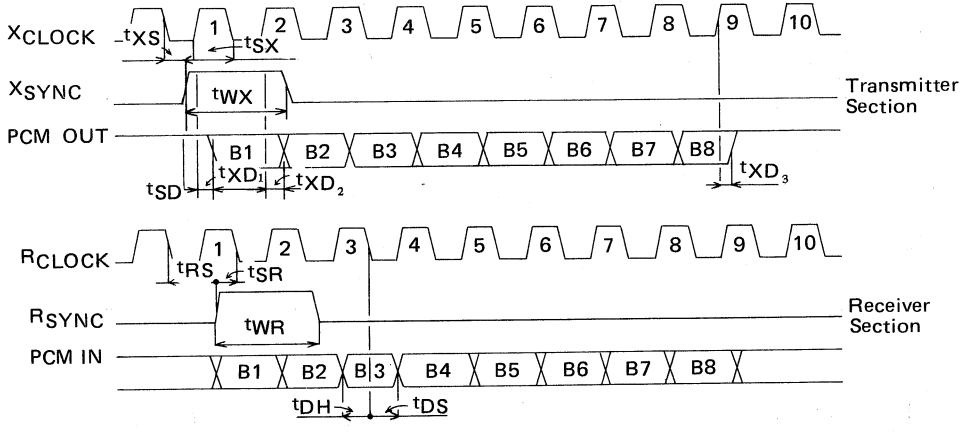


Figure 3 Basic Time Chart

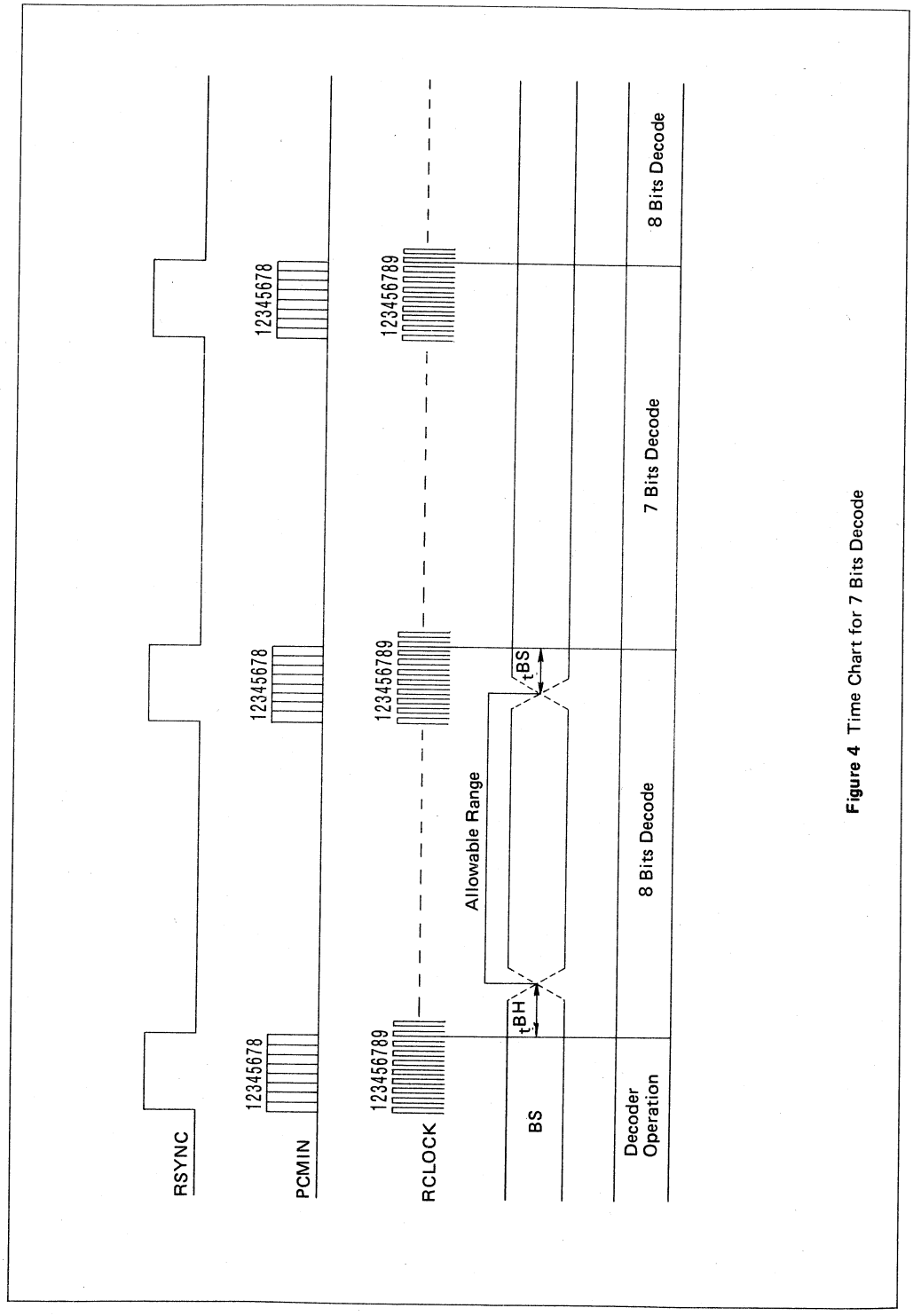
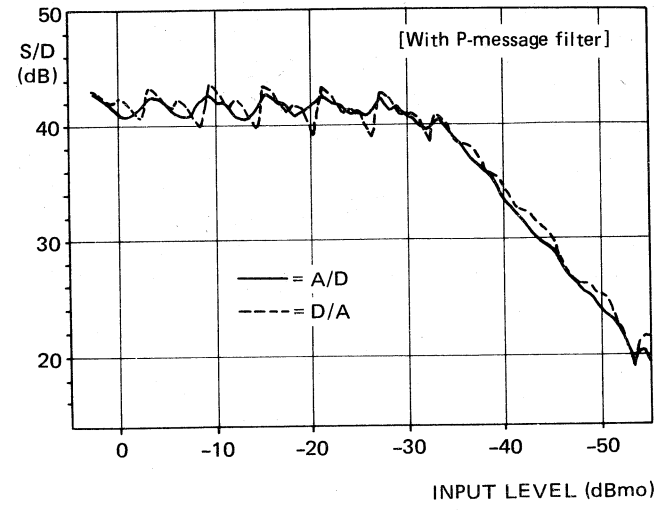
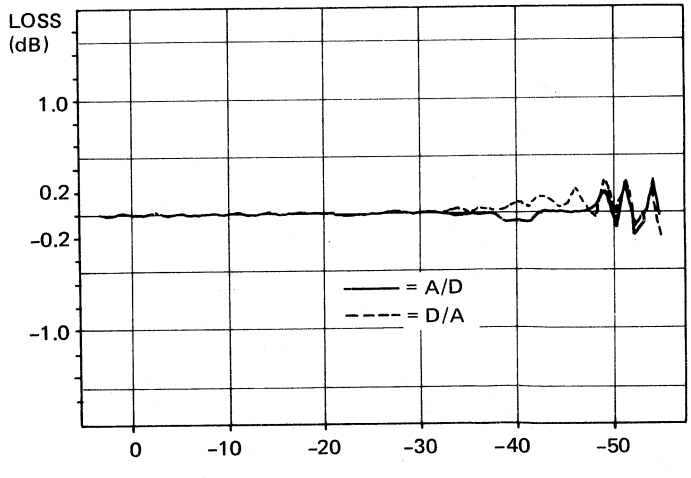


Figure 4 Time Chart for 7 Bits Decode

Signal to Distortion Ratio



Gain Tracking Characteristics



Preliminary

OKI semiconductor

MSM6814 (μ-Law)
MSM6815 (A-Law)

SINGLE CHIP COMBO CODEC WITH TIME SLOT ASSIGNMENT

GENERAL DESCRIPTION

The MSM6814 and MSM6815 are single chip COMBO CODEC with time slot assignment (TACO-DEC) which are fabricated by OKI's low power consumption CMOS silicon gate technology.

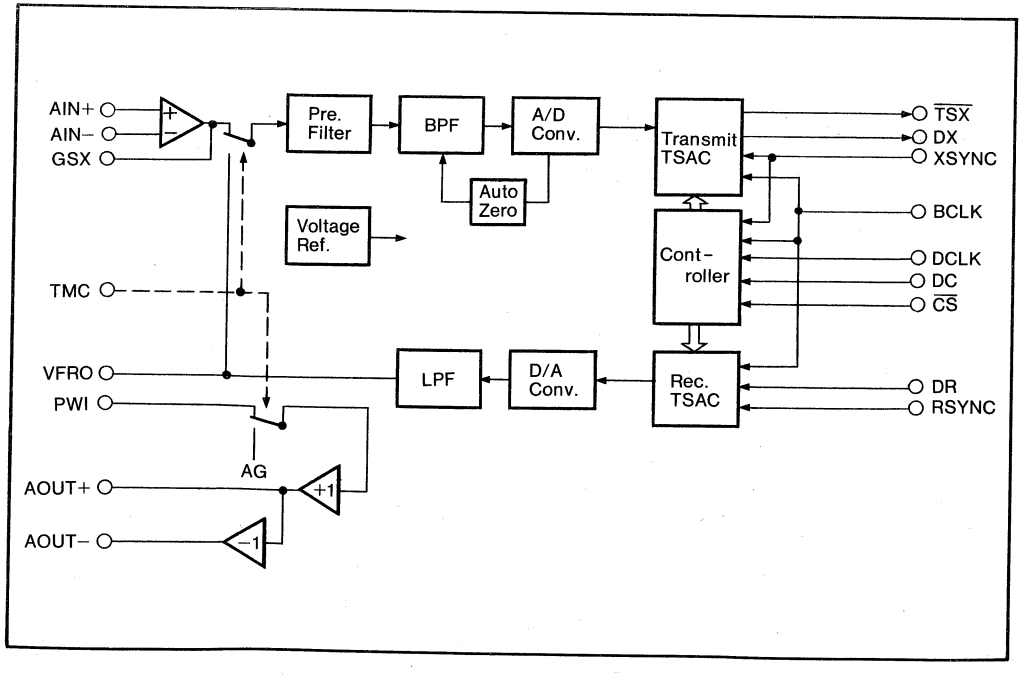
The MSM6814 and MSM6815 can control the time slot of the PCM data externally. It consists of analog pre-filters, A/D converter, D/A converter, transmit time slot assignment circuit and receive time slot assignment circuit.

FEATURES

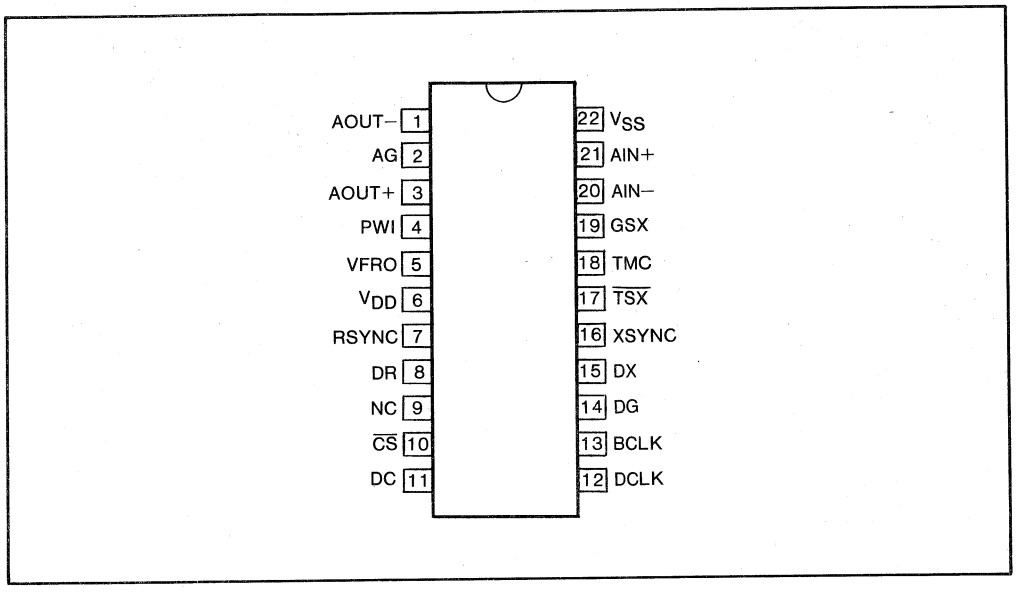
- Independant transmit and receive time slot assignment
- 32 time slot per frame maximum
- Clock rate selectable (512 KHz, 1024 KHz, 1536 KHz, 1544 KHz, 2048 KHz)
- Time slot control by serial interface
- Follows the μ-companding Law (MSM6814)
- Follows the A-companding Law (MSM6815)
- On-chip voltage reference
- On-chip full auto zero circuit
- ±5 V power supplies
- Low power dissipation
  60 mW operating (TYP)
  5 mW standby (TYP)
- 22 pin plastic DIP package

III

BLOCK DIAGRAM



PIN CONFIGURATION



ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Condition	Ratings	Unit
Supply voltage	V_{DD}	Ta = 25°C	−0.3 ~ +7	V
	V_{SS}		−7 ~ +0.3	
Analog input voltage	V_{IA}		V_{SS} − 0.3 ~ V_{DD} + 0.3	
Digital input voltage	V_{ID}		−0.3 ~ V_{DD} + 0.3	
Operating temperature	T_{OP}	−	−10 ~ +80	°C
Storage temperature	T_{stg}	−	−55 ~ +150	

Recommended Operating Conditions

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Supply voltage	V_{DD}		4.75	5.0	5.25	V
	V_{SS}		−5.25	−5.0	−4.75	
Analog input voltage	V_{AIN}		−	−	5	V_{P-P}
High input voltage	V_{IH}	XSYNC, RSYNC, BCLK, D_R, DCLK, DC, $\overline{CS}$, TMC	2.0	2.4	V_{DD}	V
Low input voltage	V_{IL}	XSYNC, RSYNC, BCLK, D_R, DCLK, DC, $\overline{CS}$, TMC	0	0	0.8	V
Clock frequency	fc	BCLK	−	512 1024 1536 1544 2048	−	KHz
Synclonizing signal frequency	fs	XSYNC, RSYNC	−	8	−	KHz
Clock duty cycle	D_L	BCLK	40	50	60	%
Digital input rise time	tr	XSYNC, RSYNC, BCLK, D_R, DCLK, DC, $\overline{CS}$ (Refer to Figure 1)	−	−	50	ns
Digital input fall time	tf	XSYNC, RSYNC, BCLK, D_R, DCLK, DC, $\overline{CS}$ (Refer to Figure 1)	−	−	50	ns
Synclonize signal timing	T_{BS}	BCLK to SYNC (Refer to Figure 2)	0			ns
	T_{SB}	SYNC to BCLK (Refer to Figure 2)	50			

Recommended Operating Conditions (Cont.)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Synclonize signal width	T_{WS}	XSYNC, RSYNC (Refer to Figure 2)	400			ns
D_R set-up time	T_{DRS}	(Refer to Figure 4)	100			ns
D_R hold time	T_{DRH}	(Refer to Figure 4)	100			ns
Data clock width	T_{WCH}	DCLK (Refer to Figure 5)	244			ns
	T_{WCL}	DCLK (Refer to Figure 5)	244			ns
$\overline{CS}$ signal timing	T_{CS1}	DCLK to $\overline{CS}$ (Refer to Figure 5)	50			ns
	T_{CS2}	$\overline{CS}$ to DCLK (Refer to Figure 5)	100			ns
	T_{CS3}	(Refer to Figure 5)	50			ns
	T_{CS4}	(Refer to Figure 5)	50			ns
DC set-up time	T_{DCS}	(Refer to Figure 5)	100			ns
DC hold time	T_{DCH}	(Refer to Figure 5)	100			ns

TIMING CHART

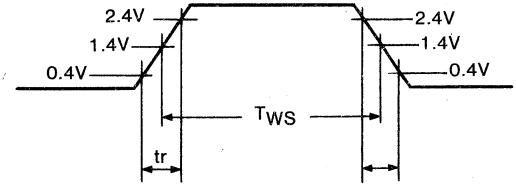


Figure 1 Definition of Rise Time and Fall Time

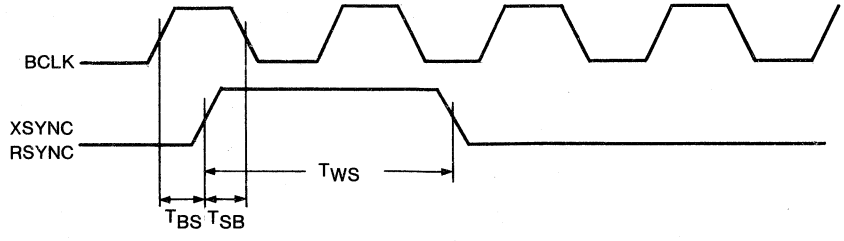


Figure 2 Synclonizing Signal Time Chart

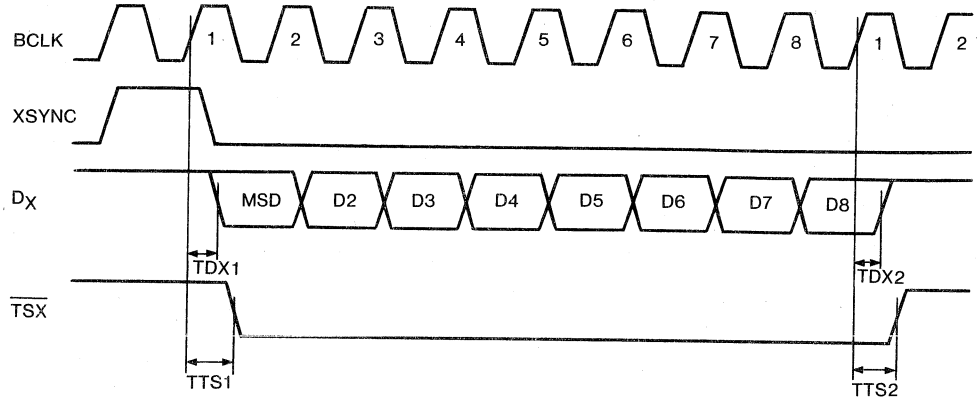


Figure 3 Transmit Signal Basic Time Chart (Time Slot 1 is selected)

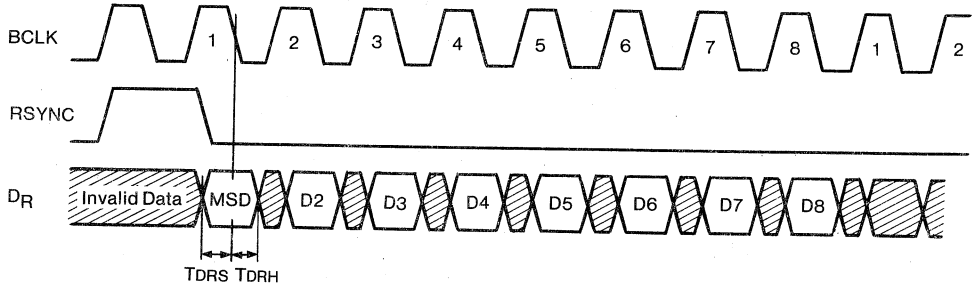
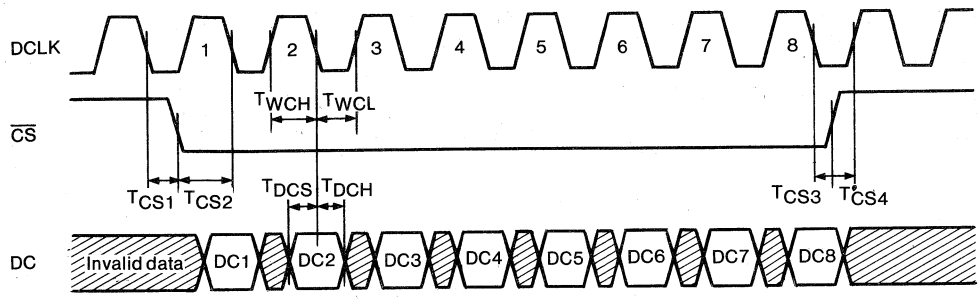
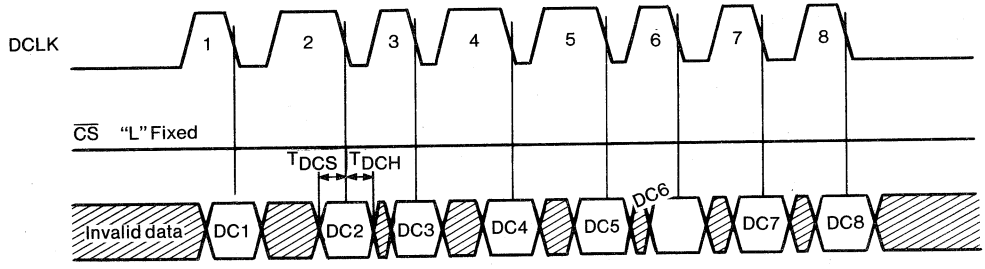


Figure 4 Receive Signal Basic Time Chart (Time Slot 1 is selected)



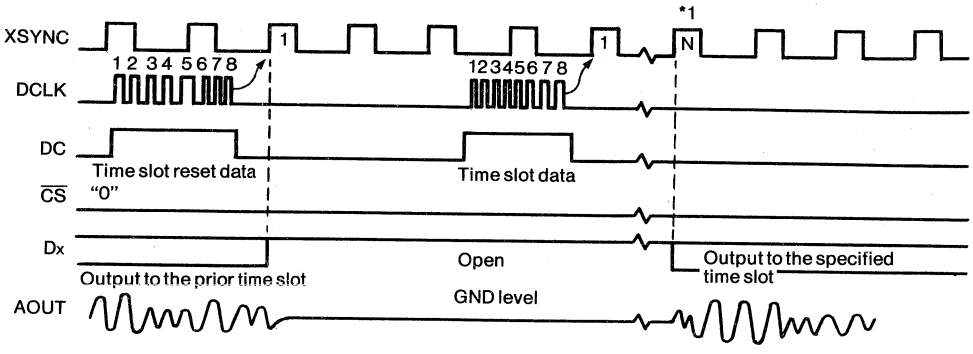
(a) When DCLK is continued



(b) DCLK is Burst CLOCK and , CS is Fixed at "L"

Figure 5 Time Slot Data Timing

Both of above operations are controlled by XSYNC signal



Note*1 : Maximum number for N is 5.

Figure 6

When the time slot is fixed, data on D_x is output on the 1st time slot 4 frames' after the internal power-on reset has been reset. Time required for power on reset is max 1 ms.

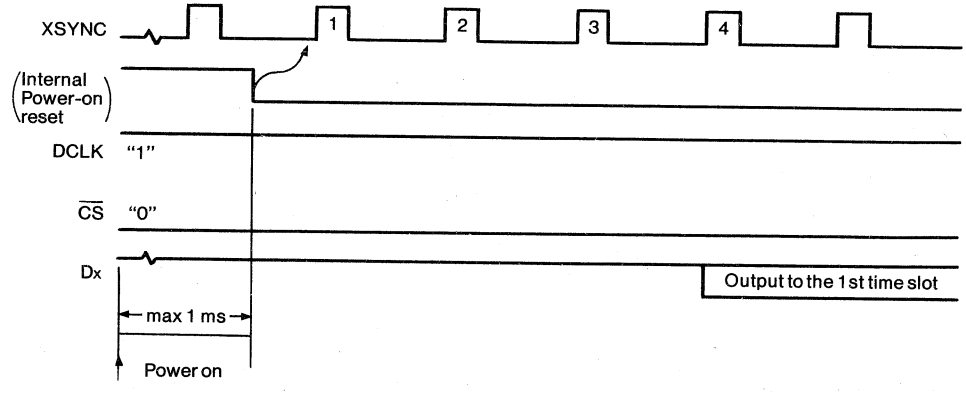


Figure 7

DC Characteristics

Parameter	Symbol	Condition		Min	Typ	Max	Unit
Supply current (Operating)	I_{DD1}	V_{DD} = +5.25 V, V_{SS} = −5.25 V		–	–	14	mA
	I_{SS1}			–	–	14	mA
Supply current (Stand-by)	I_{DD2}			–	1.0	3	mA
	I_{SS2}			–	0.3	1.5	mA
Input high voltage	V_{IH}	V_{DD} = +5.25 V, V_{SS} = −5.25 V		2.0	1.7	–	V
Input low voltage	V_{IL}	V_{DD} = +4.75 V, V_{SS} = −4.75 V		–	1.6	0.8	V
Input leakage current	I_{IH}	V_{DD} = +5.25 V, V_{SS} = −5.25 V	V_I = 5 V	–	<0.5	2.0	μA
	I_{IL}		V_I = 0 V	–	<0.5	0.5	μA
Output low voltage	V_{OL}	V_{DD} = +4.75 V, V_{SS} = −4.75 V		–	<0.2	0.4	V
Output leakage current	I_{OH}	V_{DD} = +5.25 V, V_{SS} = −5.25 V		–	<5	10	μA
Input capacitance	C_{IN}			–	5	–	PF

TRANSMIT Analog Interface

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input resistance	R_{INX}	AIN+, AIN−	1	–	–	MΩ
Load resistance	R_{LGX}	GSX	10	–	–	KΩ
Load capacitance	C_{LGX}	GSX	–	–	100	PF
Output level	V_{OGX}	GSX, R_L = 10 KΩ	−2.5	–	2.5	V
Offset voltage	V_{OSGX}	Gain = 10	−20	–	20	mV

RECEIVE Analog Interface

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input resistance	R_{INPW}	PWI	1	–	–	MΩ
Load resistance	R_{LVF}	VFRO	10	–	–	KΩ
	R_{LAO}	AOUT+, AOUT−	600	–	–	Ω
Load capacitance	C_{LVF}	VFRO	–	–	100	PF
	C_{LAO}	AOUT+, AOUT−	–	–	100	PF
Output level	V_{OVF}	VFRO, R_L = 10 KΩ	−2.5	–	2.5	V
	V_{OAO}	AOUT+, AOUT−, R_L = 600 Ω	−2.5	–	2.5	V
Offset voltage	V_{OSVF}	VFRO	−150	–	150	mV
	V_{OSAO}	AOUT+, AOUT−, PWI = 0 V	−20	–	20	mV

A.C. Characteristics

V_{DD} = +5 V ±5%, V_{SS} = −5 V ±5%

Parameter	Symbol	Condition f (Hz)	Condition Level (dBmO)		Min	Typ	Max	Unit
Transmit frequency response	Loss T1	60	0		20	26	–	dB
	Loss T2	300			−0.1	−0.03	0.2	
	Loss T3	820			Reference Value			
	Loss T4	2020			−0.1	0.0	0.2	
	Loss T5	3000			−0.1	0.10	0.2	
	Loss T6	3400			0	0.45	0.8	
	Loss T7	3980			14	16	–	
Receive frequency response	Loss R1	300	0		−0.1	−0.02	0.2	dB
	Loss R2	820			Reference Value			
	Loss R3	2020			−0.1	0.0	0.2	
	Loss R4	3000			−0.1	0.10	0.2	
	Loss R5	3400			0.0	0.65	0.8	
	Loss R6	3980			14	16	–	
Transmit signal to distortion Ratio (*1)	SD T1	1020	3		36	43	–	dB
	SD T2		0		36	41	–	
	SD T3		−30		36	40	–	
	SD T4		−40	*2	31	34.5 / 33	–	
	SD T5		−45	*2	26	31 / 28.5	–	
Receive signal to disortion ratio (*1)	SD R1	1020	3		36	44	–	dB
	SD R2		0		36	41	–	
	SD R3		−30		36	41	–	
	SD R4		−40	*2	31	35.5 / 35	–	
	SD R5		−45	*2	26	34 / 28.5	–	

*1: The measurement is taken with P-message filter.

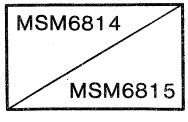
*2:

MSM6814 / MSM6815

Parameter		Symbol	Condition f (Hz)	Condition Level (dBmO)		Min	Typ	Max	Unit
Transmit gain tracking		GT T1	1020	3		−0.2	−0.01	0.2	dB
		GT T2		−10		Reference Value			
		GT T3		−40		−0.2	0.05	0.2	
		GT T4		−50		−0.4	0.25	0.4	
		GT T5		−55		−0.8	0.10	0.8	
Receive gain tracking		GT R1	1020	3		−0.2	0.02	0.2	
		GT R2		−10		Reference Value			
		GT R3		−40		−0.2	−0.5	0.2	
		GT R4		−50		−0.4	−0.16	0.4	
		GT R5		−55		−0.8	−0.13	0.8	
Idle channel noise *3	Transmit	NIDL T	−	−		−	−89	−75	dBmOp
	Receive	NIDLR	−	−		−	−89	−75	
Analog input level		VIN	1020	0	*4	1.185 / 1.189	1.227 / 1.231	1.270 / 1.274	Vrms
Analog output level		VOUT	1020	0	*4	1.185 / 1.189	1.227 / 1.231	1.270 / 1.274	Vrms
Absolute delay time		tD	−	−		−	0.47	0.5	ms
Transmit Group delay time		tGD T1	500	0		−	0.2	0.75	ms
		tGD T2	600			−	0.1	0.35	
		tGD T3	1000			−	0	0.125	
		tGD T4	1800			Reference Value			
		tGD T5	2600			−	0.05	0.125	
		tGD T6	2800			−	0.07	0.75	
Receive Group delay time		tGD R1	500	0		−	−0.02	0.75	ms
		tGD R2	600			−	−0.02	0.35	
		tGD R3	1000			−	0.03	0.125	
		tGD R4	1800			Reference Value			
		tGD R5	2600			−	0.07	0.125	
		tGD R6	2800			−	0.10	0.75	

*3: The measurement is taken with P-message filter.

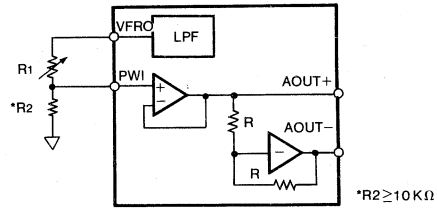
*4:



III

Parameter		Symbol	Condition f (Hz)	Condition Level (dBmO)	Min	Typ	Max	Unit
Crosstalk	T to R	CR T	1020	0	–	−90	−66	dBmO
	R to T	CR R	1020		–	−78	−66	
Discrimination against out-of-band input signals		DIS	4.6K ~ 72K	−25	30	32	–	dB
Spurious out-of-band signals at the output		SO	300 ~ 3400	0	–	−33	−30	dBmO
Intermodulation		IMD 1	fa = 470 fb = 320	−4	–	−40	−38	dB
Spurious in-band signals at the output		S1	1020	0	–	−45	−40	dBmO
Single frequency noise		NS	–	–	–	−60	−50	dBmO
VDD PSRR	Transmit	PPSR T	0 ~ 300K	200 mVp-p	–	30	–	dB
	Receive	PPSR R			–	30	–	
VSS PSRR	Transmit	NPSR T			–	30	–	dB
	Receive	NPSR R			–	30	–	
Digital output delay time		TDX1	R pull = 1 kΩ CL = 100 pF Refer to Figure 3		50	–	200	ns
		TDX2			50	–	200	
		TTS1			50	–	300	
		TTS2			50	–	300	
Digital output fall time		tDDf			–	20	100	ns

PIN DESCRIPTION

Pin No.	Pin Name	Function
1	AOUT−	Receive analog signal output pins. The maximum output signal swing is 5 Vp-p. These output can drive the impedance of 600Ω.
3	AOUT+	The output level of AOUT− is a reversed output level of AOUT+. These output levels are fixed at 0V in the power down mode.
2	AG	Analog ground level.
4	PWI	Input pin for the receive buffer amplifier. Receive level can be adjusted by using VFRO pin and PWI. 
5	VFRO	Output pin for receive filter. Voltage swing of output signal is 5Vp-p. So, it can drive a resistor of 10 KΩ or more.
6	V_{DD}	Positive power supply pin. +5 V ±5% has to be applied.
7	RSYNC	Input pin for the receive synchronous signal. This signal is the base signal for the time slot of the receive PCM signal (DR). Rising edge of BCLK signal followed by the rising edge of this signal becomes the first clock. (Refer to Figure 4)
8	DR	PCM signal input pin. PCM signal is written at the falling edge of BCLK signal. It is latched into the internal resistor when the 8-bit data is written. Time slot, to which the data is written, can be control by following two methods. 1) Fix the time slot Time slot 1 is selected by fixing the DCLK at "H" when the power is turned on. 2) Variable time slot Time slot can be selected out of 1 ~ 32 according to the time slot data (DC). Refer to the description about DC, DCLK, CS. The method for AD/DA conversion and coding method of input/output is conformed to CCITT's recommendation G711. MSM6815 is also provided with the even number's reverse function.

Input/ output level	Dx/DR	
	MSM6814	MSM6815
+FS	1 0 0 0 0 0 0 0	1 0 1 0 1 0 1 0
+ 0	1 1 1 1 1 1 1 1	1 1 0 1 0 1 0 1
− 0	0 1 1 1 1 1 1 1	0 1 0 1 0 1 0 1
−FS	0 0 0 0 0 0 0 0	0 0 1 0 1 0 1 0

III

PIN DESCRIPTION (CONT.)

Pin No.	Pin Name	Function
10	$\overline{CS}$	Time slot control signal input pin for receiving and transmitting of data.
11	DC	DCLK ..... A clock which enables to write a time slot data. 8-bit burst clock or a continuous clock. Cycyle of the clock is 488 ns minimum.
12	DCLK	$\overline{CS}$ ..... Chip select signal input pin. When this pin is at "L" level, DCLK signal becomes valid.
		DC ..... Time slot data input pin. It consists of $DC_1 \sim DC_8$ and the data is written at the falling edge of DCLK signal.

DC_1	DC_2	DC_3	Operation
0	0	X	Specify the time slot of Transmit or Receive
0	1	X	Specify the time slot of Transmit
1	0	X	Specify the time slot of Receive
1	1	X	Reset for time slot function, power down mode.

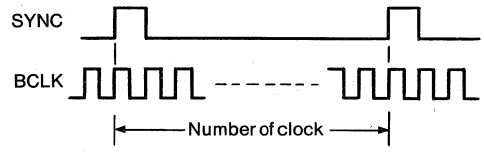
DC_4	DC_5	DC_6	DC_7	DC_8	Time Slot
0	0	0	0	0	1
0	0	0	0	1	2
0	0	0	1	0	3
.	.	.	.	.	.
.	.	.	.	.	.
1	1	1	0	1	30
1	1	1	1	0	31
1	1	1	1	1	32

Time slot can be specified out of $1 \sim 32$.
When the frequency of BCLK is lower than 2048 KHz, maximum number of the time slot is specified as follows. In this use, however, no time slot is chosen when 17th time slot is specified when BCLK is operated at 1024 KHz.

BCLK	Variable time slot
512 KHz	$1 \sim 8$
1024 KHz	$1 \sim 16$
1536 KHz	$1 \sim 24$
1544 KHz	$1 \sim 24$
2048 KHz	$1 \sim 32$

In the variable time slot mode, the relation between the time slot data input and output data D_X is described in figure 6 below.
(The specified time slot appears from the Nth frame followed by the falling edge of 8th bit of DCLK.)
To have the time slot assignment function reset, disable the D_X output in the first frame followed by the falling edge of 8th bit of DCLK.
In this case, AOUT is also fixed at GND level.

PIN DESCRIPTION (CONT.)

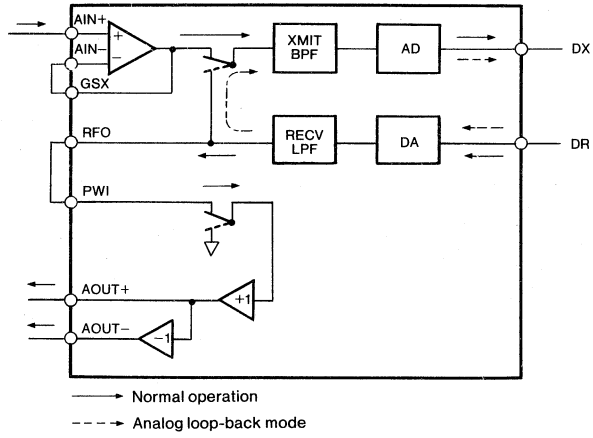
<table>
<tr><th>Pin No.</th><th>Pin Name</th><th>Function</th></tr>
<tr><td>13</td><td>BCLK</td><td>Shift clock input pin to write/read the PCM data (Dx or DR). This signal has to be a continuous clock signal as it is counted down and is used as the clock signal for SCF filter and timing signal for AD/DA conversion.
To guarantee the frequency characteristics of the filter, diviation of the input clock frequency has to be ±50 PPM.
If the frequency characteristics of the equipment is not specified strictly, MSM6814 and MSM6815 operate normally if the clock signal and SYNC are within the range of the figure described in following table. (In this case, however, electrical characteristics of MSM6814 and MSM6815 cannot be guaranteed.)
<table>
<tr><th rowspan="2">Nominal data rate of DX and DR</th><th colspan="3">Number of clock between SYNC signal</th></tr>
<tr><th>Main value</th><th>Minimum</th><th>Maximum</th></tr>
<tr><td>512 Kb/s</td><td>64</td><td>64</td><td>65</td></tr>
<tr><td>1024 Kb/s</td><td>128</td><td>127</td><td>130</td></tr>
<tr><td>1536 Kb/s</td><td>192</td><td>190</td><td>195</td></tr>
<tr><td>1544 Kb/s</td><td>193</td><td>190</td><td>195</td></tr>
<tr><td>2048 Kb/s</td><td>256</td><td>253</td><td>257</td></tr>
</table>

</td></tr>
<tr><td>14</td><td>DG</td><td>Digital ground pin.</td></tr>
<tr><td>15</td><td>DX</td><td>PCM signal output pin.
This signal is synchronized with the rising edge of BCLK signal. The time slot, output from Dx, can be controlled by following two methods.
1) Fix the time slot
Time slot 1 is selected by fixing the DCLK at "H" when the power is turned on.
2) Variable time slot
Time slot can be selected out of 1 ~ 32 according to the time slot data (Dc). Refer to the description about Dc, DCLK, $\overline{CS}$.
The output of this pin is a open drain output and is at "open" except when time slot is output. A pull-up resistor of more than 1 KΩ has to be connected between V_{DD} and Dx.</td></tr>
<tr><td>16</td><td>XSYNC</td><td>Input pin for the transmit synchronous signal.
This signal is the base signal for the time slot of the transmit PCM signal (Dx).
Rising edge of BCLK signal followed by the rising edge of this signal becomes the first clock (Refer to Figure 3). XSYNC is not necessary to be synchronized with the RSYNC, but it has to be synchronized with BCLK. Frequency of this signal is 8 KHz. By fixing this synchronizing signal at either "H" or "L", power down function can be realized.</td></tr>
</table>

III

PIN DESCRIPTION (CONT.)

Pin No.	Pin Name	Function
17	$\overline{TSX}$	Output pin for transmit time slot signal. The selected time slot is output when this signal is at "L" level. This pin has to be pulled-up by a resistor with more than 2 KΩ as it is open drain output.
18	TMC	Mode switching signal input pin. Operation mode or analog loop-back mode can be selected.

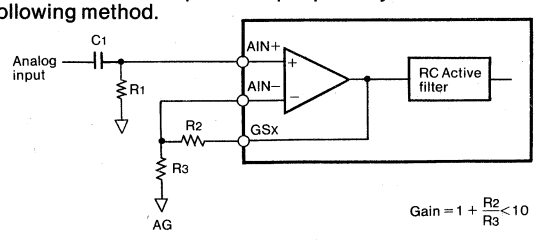
TMC input	Mode
> 2.0 V	Normal
< 0.8 V	Analog loop-back



——→ Normal operation

- - - → Analog loop-back mode

19	GSX	These three pins are used for the transmit level adjustment. AIN+ is a non-inverting analog input pin which is connected to the non-inverting input of a transmit amplifier.
20	AIN−	AIN− is a inverting analog input pin which is connected to the inverting input of the transmit amplifier.
21	AIN+	GS_X is a transmit amplifier output pin. Adjustment can be done by following method.



Note:
1. $R_2 + R_3 > 10K\Omega$
2. When the DC off-set voltage of analog input is more than 20 mV, C_1 and R_1 should provide for DC blocking. In this case, cut-off frequency of HPF, composed by R_1 and C_1, should be less than 30 Hz
3. R_1 should be less than 20 KΩ.

22	V_{SS}	Negative power supply pin. −5 V ±5% has to be applied.

D. PABX APPLICATION

III

OKI semiconductor

MSA4710

SUBSCRIBER LINE INTERFACE CIRCUIT

GENERAL DESCRIPTION

The MSA4710 is designed to provide BSH functions and to meet PABX transmission performance requirements.

This device can replace the hybrid transformer circuit.

FEATURES

- B (Batteryfeed), S (Supervision), and H (Hybrid) functions integrated on chip
- Design to meet Central Office and PABX quality transmission requirements
- All transmission performance parameters can be externally programable
- Free from parastic SCR's using dielectric isolation technology
- Size and weight reduction over conventional approaches
- 28 pin plastic DIP package, 28 pin PLCC package

III

BLOCK DIAGRAM

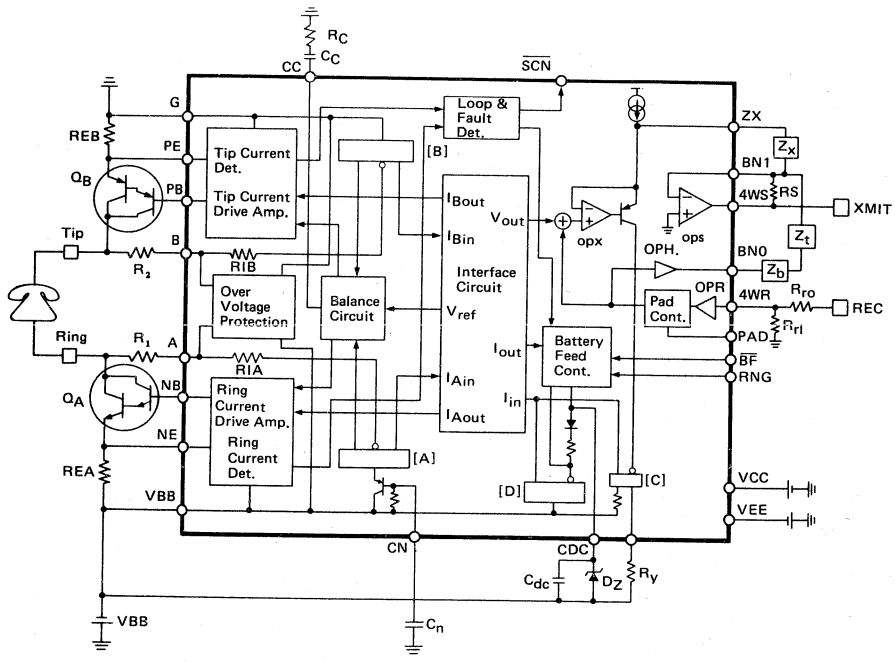
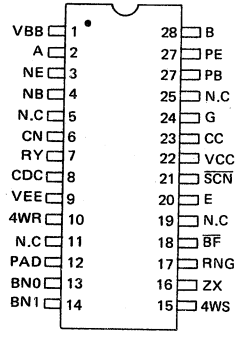


Figure 1 OKI SLIC functional block diagram

PIN CONFIGURATION

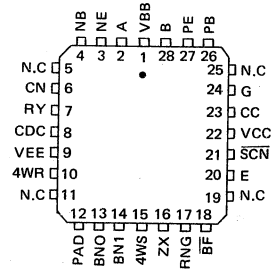
Top View

28 pin Plastic Dip Package



MSA4710RS

28 pin Plastic Leaded Chip Carrier Package



MSA4710JS

PIN DESCRIPTION

Name	Pin No.	Function
VBB	1	Battery supply, -48V input.
A	2	The Ring voltage sensing input. This input is high impedance (apr. 38 kΩ), and is connected to the built-in over voltage protection circuit.
NE	3	The Ring current sensing input and is connected to the emitter of NPN Darlington transister and the power resistor REA.
NB	4	The base drive output for the NPN Darlington transister.
N. C.	5	No connection
CN	6	Battery noise rejection capacitor input. This capacitor value is 60 V 1 μF.
RY	7	AC performance adjusting resistor Ry input.
CDC	8	AC high impedance providing capacitor Cdc input and constant current feed at the short line adjusting zener diode input. This capacitor value is 15 V 4.7 μF.
VEE	9	–5 V input.
4WR	10	Receive input and is connected to the positive input of the built-in buffer operational amplifier.
N. C.	11	No connection
PAD	12	Pad control input. A logic level "H" makes the transmission level of 4WR to 2 Wire be 4dB lower.
BN0	13	The balancing network drive output.
BN1	14	2 wire terminating impedance compornent Zx input, transhybrid impedance Zt or Zb input and 2 wire to XMIT transmission gain adjusting resistor Rs input. This input sumes the current from the BN0 through Zb, Zt, the ZX through Zx and the 4WS through Rs.
4WS	15	Transmit output.
ZX	16	2 wire terminating impedance compornent Zx input. This pin has a low input impedance.
RNG	17	Ringing mode control input. A logic level "H" enables either the Tip or Ring power Darlington transister to source the half of return current of the Ringing signal, changes the threshold of the fault current detector and inhibits the loop current detector from operating.
$\overline{BF}$	18	Battery-feed mode control input. A logic level "H" switches off both the Ring and Tip current drive amp. and presents a high impedance to the line. (apr. 80 kΩ).
N. C.	19	No connection
E	20	Should be connected to G.

Name	Pin No.	Function
$\overline{SCN}$	21	Output of both the fault current detector and loop current detector. A logic level "H" indicates Off-hook or line fault condition. This output is open-collector with a built-in pull-up resistor. (apr. 10 kΩ)
VCC	22	+5V input.
CC	23	Compensation capacitor Cc, in series with Rc, input. These capacitor and resistor are 4700 pF (30 V) and 2 kΩ, respectively.
G	24	Ground input.
N. C.	25	No Connection
PB	26	The base drive output for the PNP Darlington power transistor.
PE	27	The Tip current sensing input and is connected to the emitter of the PNP Darlington power transister and the power resistor REB.
B	28	The Tip voltage sensing input. This input is high impedance (apr. 38 kΩ) and is connected to the built-in over voltage protection circuit.

ABSOLUTE MAXIMUM RATINGS

Ta = 25°C

Rating	Symbol	Value	Unit
Supply voltage	V_{BB}	−60 ~ +0.3	V
	V_{CC}	−0.3 ~ +7.0	
	V_{EE}	−7.0 ~ +0.3	
Tip and Ring voltage sensing terminals A and B input current	I_A, I_B	±200	mA
Receive signal input voltage	V_{4WR}	V_{EE}−0.5 ~ V_{CC}+0.5	V
Operating junction temperature	T_j	125	°C
Storage temperature range	T_{stg}	−55 ~ 150	°C

RECOMMENDED OPERATING CONDITIONS

Rating	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{BB}	−53	−48	−43	V_{dc}
	V_{CC}	+4.75	+5	+5.25	
	V_{EE}	−5.25	−5	−4.75	
Operating ambient temperature	T_a	0	–	70	°C
Loop current	I_L	20	–	80	mA
Longitudinal induced current	I_{AC}	–	–	10	mArms / conductor

III

ELECTRICAL CHARACTERISTICS

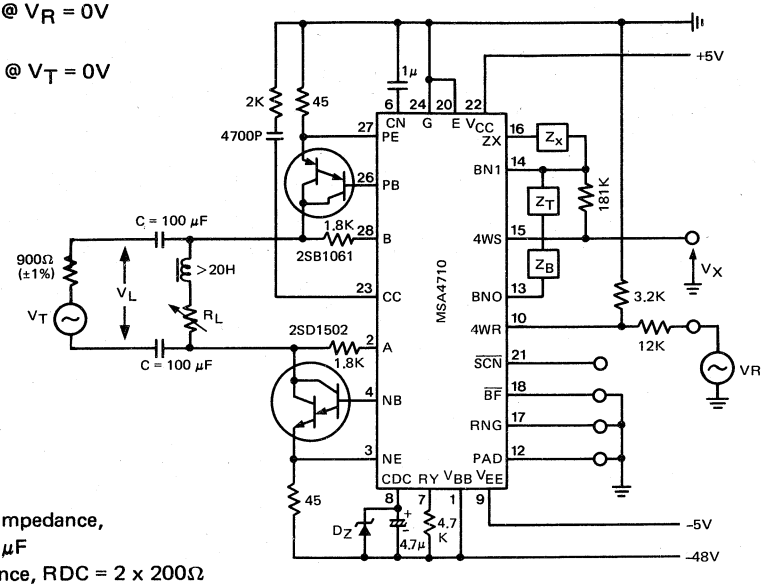
Ta = 0°C ~ 70°C, V_{BB} = –48 V ±5 V, V_{CC} = +5V ±5%
V_{EE} = –5V ±5%

- REA = REB = 45Ω, Ry = 4.7 KΩ
- 2 wire terminating impedance = 900 Ω +2.16 μF
- Balancing network = 800 Ω//(100 Ω + 50μF)

Parameters		Symbol	Conditions		Min.	Max.	Unit
Minimum battery feed current		I_{LM}	V_{BB} = –48 V R_L = 1900 Ω		20	–	mA
Power dissipation	ON-Hook	P_{S0}	V_{BB} = –53 V R_L = open V_{CC} = +5.25 V, V_{EE} = –5.25 V		–	170	mW
	OFF-Hook	P_{S1}	V_{BB} = –53 V R_L = 50 Ω V_{CC} = +5.25 V, V_{EE} = –5.25 V		–	700	mW
ON-Hook supply current		I_{BB}	V_{BB} = –53 V R_L = open V_{CC} = +5.25 V V_{EE} = –5.25 V		–	2.4	mA
		I_{CC}			–	7.8	
		I_{EE}			–	5.4	
2-wire leak current		I_{LEAK}	V_{BB} = –53 V R_L = 0 Ω $\overline{BF}$ = H		–	1.0	mA
2-wire return loss		R_L	Fig. 3	0.2 KHz ~ 0.5 KHz	23	–	dB
				0.5 KHz ~ 3.4 KHz	29	–	
Frequency response		F_R	Fig. 2	f = 0.3 KHz ~ 3.4 KHz	–0.1	+0.1	dB
Insertion loss variety		ΔL_I	Fig. 2	f = 1004 Hz I_L = 20 mA ~ 80 mA	–0.1	+0.1	dB
Idle channel noise		N_I	C-message Fig. 5		–	10	dBrnc
Transhybrid loss		T_{HL}	Fig. 4	0.2 KHz ~ 0.5 KHz	23	–	dB
				0.5 KHz ~ 2.5 KHz	28	–	
				2.5 KHz ~ 3.4 KHz	23	–	
Longitudinal balance		L_B	Fig. 6 0.2 KHz ~ 3.4 KHz The matchig of REA and REB is ±0.1%		46	–	dB
Power supply noise rejection ratio		P_{SR}	Fig. 7 0.2 KHz ~ 3.4 KHz V_{in} = 100 mVp-p		30	–	dB

$$G_{24} = 20 \log \left| \frac{V_X}{V_L} \right| @ V_R = 0V$$

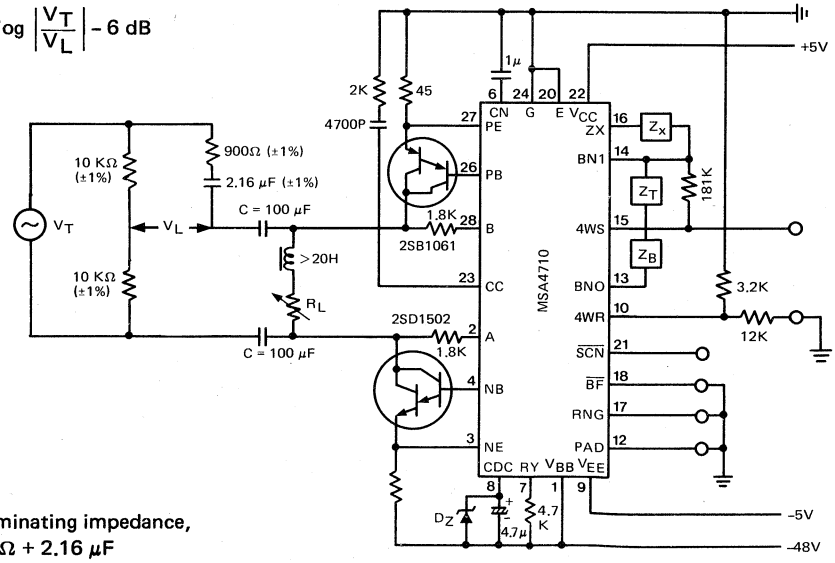
$$G_{42} = 20 \log \left| \frac{V_L}{V_R} \right| @ V_T = 0V$$



- 2-wire terminating impedance, $Z_{to} = 900\Omega + 2.16\ \mu F$
- Battery feed resistance, RDC = 2 x 200Ω
- Transmit and receive gain, $G_{24} = G_{42} = 0$ dB
- Balancing network, $Z_L = 800\Omega // (100\Omega + 50\ nF)$ (See APPLICATIONS INFORMATION)

Figure 2 Transmit & Receive Gain Test Circuit

$$R_L = 20 \log \left| \frac{V_T}{V_L} \right| - 6\ dB$$

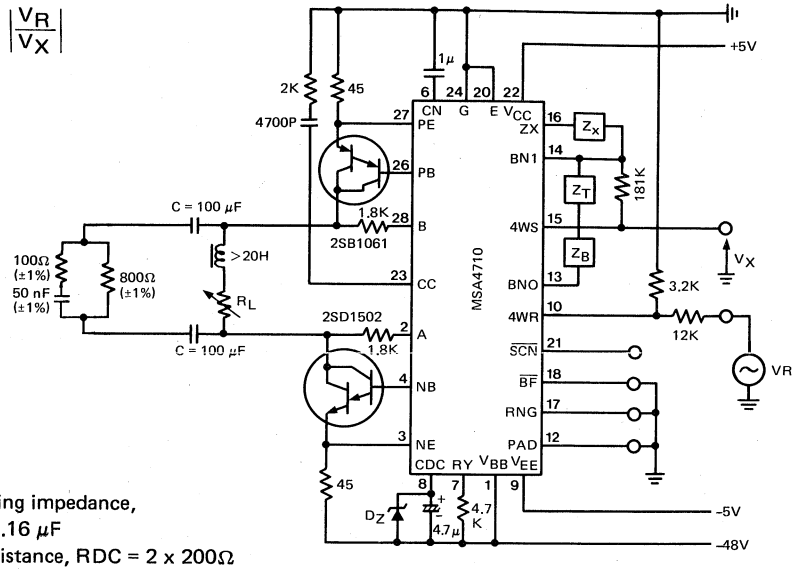


- 2-wire terminating impedance, $Z_{to} = 900\Omega + 2.16\ \mu F$
- Battery feed resistance, RDC = 2 x 200Ω
- Transmit and receive gain, $G_{24} = G_{42} = 0$ dB
- Balancing network, $Z_L = 800\Omega // (100\Omega + 50\ nF)$ (See APPLICATIONS INFORMATION)

Figure 3 2-wire Return Loss Test Circuit

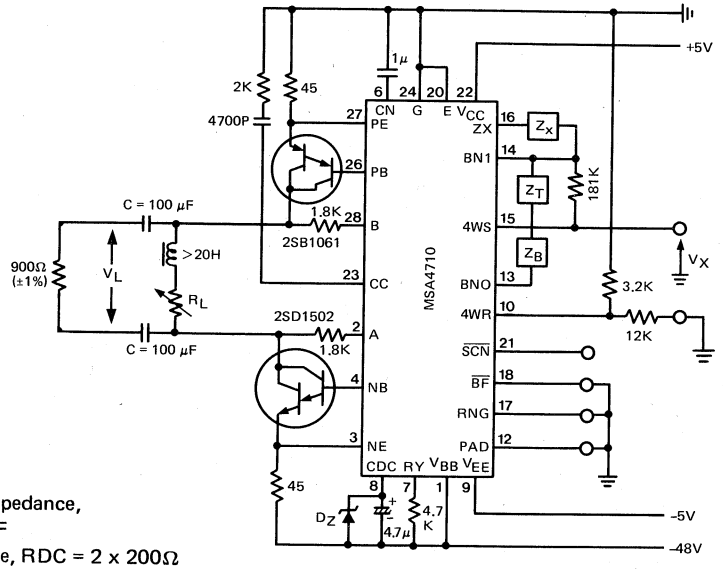
III

$$T_{HL} = 20 \log \left| \frac{V_R}{V_X} \right|$$



- 2-wire terminating impedance, $Z_{to} = 900\Omega + 2.16\ \mu F$
- Battery feed resistance, RDC = 2 x 200Ω
- Transmit and receive gain, $G_{24} = G_{42} = 0$ dB
- Balancing network, $Z_L = 800\Omega // (100\Omega + 50\ nF)$ (See APPLICATIONS INFORMATION)

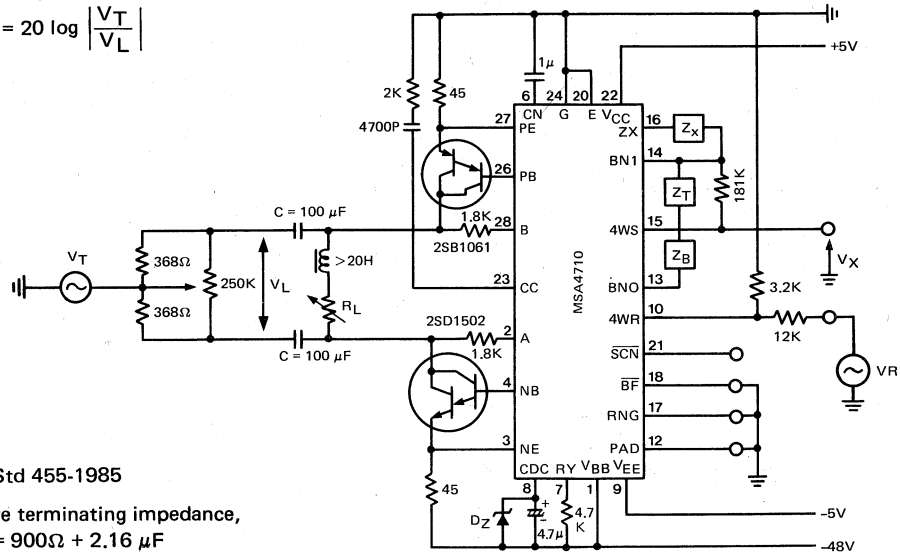
Figure 4 Transhybrid Loss Test Circuit



- 2-wire terminating impedance, $Z_{to} = 900\Omega + 2.16\ \mu F$
- Battery feed resistance, RDC = 2 x 200Ω
- Transmit and receive gain, $G_{24} = G_{42} = 0$ dB
- Balancing network, $Z_L = 800\Omega // (100\Omega + 50\ nF)$ (See APPLICATIONS INFORMATION)

Figure 5 Idel Channel Noise Test Circuit

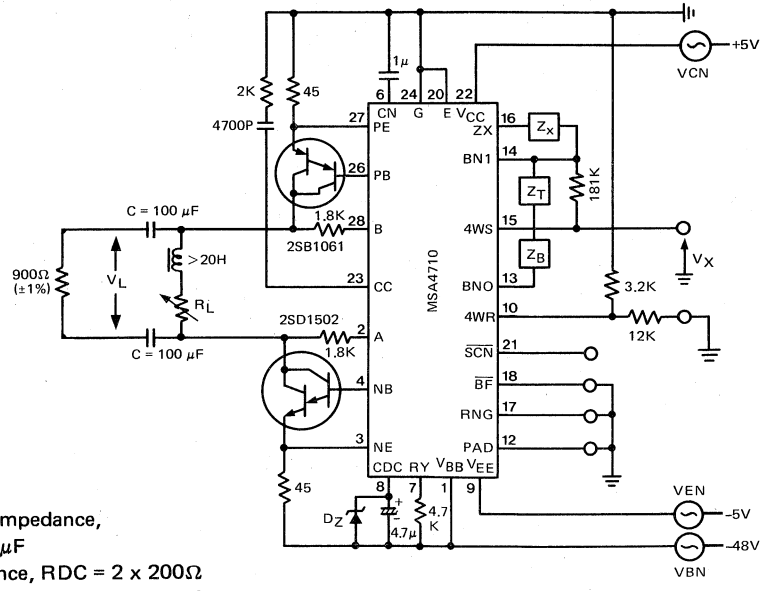
$$L_B = 20 \log \left| \frac{V_T}{V_L} \right|$$



IEEE Std 455-1985

- 2-wire terminating impedance, $Z_{to} = 900\Omega + 2.16\ \mu F$
- Battery feed resistance, RDC = 2 x 200Ω
- Transmit and receive gain, $G_{24} = G_{42} = 0$ dB
- Balancing network, $Z_L = 800\Omega // (100\Omega + 50\ nF)$ (See APPLICATIONS INFORMATION)

Figure 6 Longitudinal Balance Test Circuit



- 2-wire terminating impedance, $Z_{to} = 900\Omega + 2.16\ \mu F$
- Battery feed resistance, RDC = 2 x 200Ω
- Transmit and receive gain, $G_{24} = G_{42} = 0$ dB
- Balancing network, $Z_L = 800\Omega // (100\Omega + 50\ nF)$ (See APPLICATIONS INFORMATION)

Figure 7 Supply Noise Rejection Test Circuit

III

APPLICATIONS INFORMATION

The OKI SLIC is comprised of a bipolar dielectric isolated integrated circuit. MSA4710, two compremementary Darlinton power transisters, a 2-wire terminating compornents, Z_x, two transhybrid rejection impedances Z_t, Z_b nine resistors and three capacitors as shown in Figure 1.

The circuit of Figure 1 will provide:

Adjustable resistive battery feed
Adjustable maximum loop current at the short line
Adjustable 2-wire terminating impedance
Adjustable transmit and receive gain
2-wire balancing to 4-wire single ended conversion
Adjustable balancing network
Hook-state output
Line fault current limiting (apr. 50 mA)
Rejection of longitudinal induced current (10 mArms/conductor)
Adjustable longitudinal balance.

1) DC CHARACTERISTICS

a) Battery feed

In the Off-hook state the equivalent battery feed resistance RDC is given by

$$RDC = (REA + REB) \times 4.44 \quad \ldots\ldots\ldots\ldots \quad (1)$$

Examples

RDC = 2x200Ω REA = REB = 45Ω
RDC = 2x220Ω REA = REB = 50Ω

The matching of REA and REB is critical to a number of AC performance parameters.

b) Maximum loop current limiting

The constant current feed at the short line is acheived by connecting a zener diode between the terminal CDC and VBB.

The constant current value is given by:

$$Icl = 0.9 \times (V_Z - 2)/REA \quad \ldots (2)$$

V_Z: Zener voltage

Typical Battery feed characteristics is shown in Figure 8.

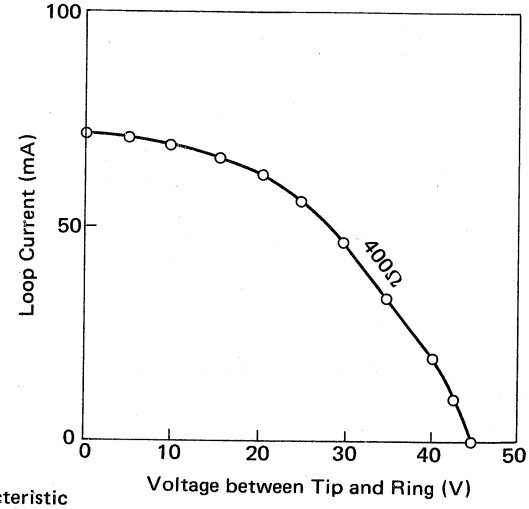


Figure 8 Typical Batteryfeed Characteristic

2) SUPERVISION

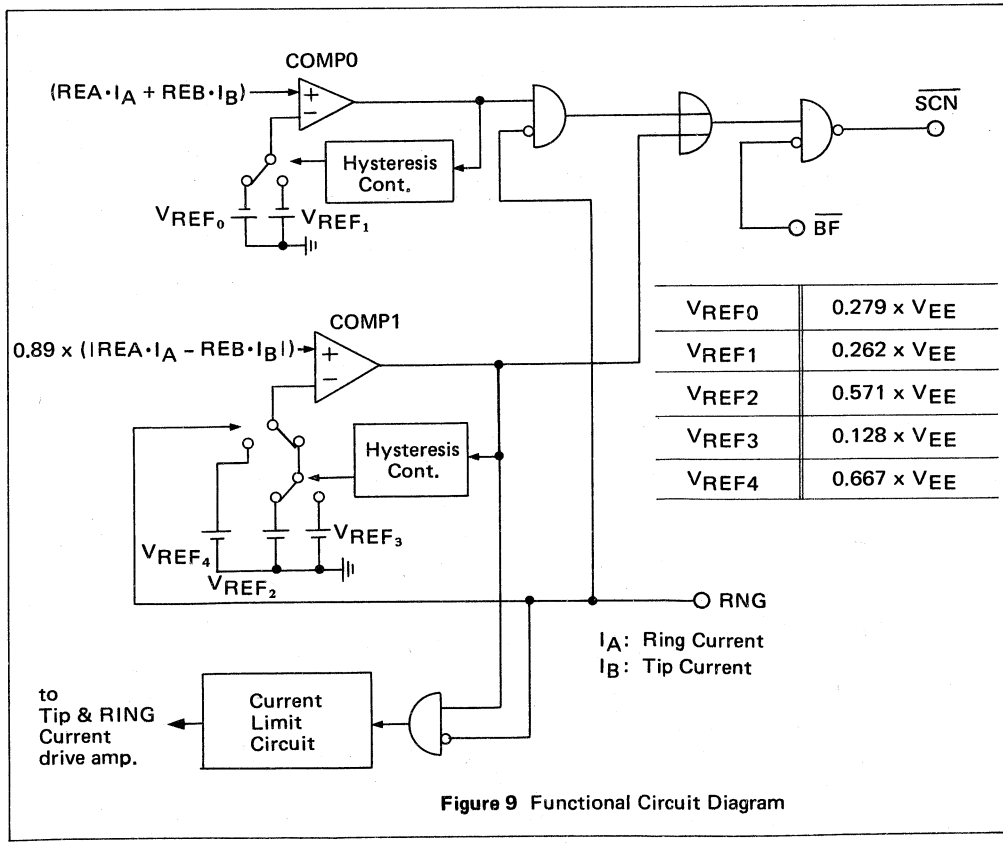
The OKI SLIC has two comparators, Comp0 and Comp1, to supervise the subscriber line conditions. The Comp0 can detect the sum current of the Ring and Tip through the power resistors REA, REB, and the Comp1 can detect the absolute differential current between the Ring and Tip through REA and REB. Thereby, the subscriber's On-hook or Off-hook and Dialing pulses can be detected by Comp0, and subscriber line's troubles such as Ring-to-ground or Tip-to-battery fault can be detected by Comp1.

The Current-limit-circuit can make the fault current limiting at apr. 50 mA when the Comp1 detects the fault current.

Functional circuit diagram of supervision is shown in Figure 9, and the threshold current value is shown in table 1.

The RNG function can be used to send the Ringing signal. (see Figure 11)

When RNG is logic level "H", to prevent the two comparators from detecting the ringing signal current which flowes into the short line in the On-hook state, the detecting threshold of Comp1 is become higher than that of the detecting line fault, and output of the Comp0 is inhibited from making the $\overline{SCN}$ low, and at the same time, to prevent the Current-limit-circuit which causes the Ringing signal current to distort from operting, the output of the Comp 1 is inhibited from driving the Current-limit-circuit.



V_{REF0}	0.279 x V_{EE}
V_{REF1}	0.262 x V_{EE}
V_{REF2}	0.571 x V_{EE}
V_{REF3}	0.128 x V_{EE}
V_{REF4}	0.667 x V_{EE}

Figure 9 Functional Circuit Diagram

Table 1

V_{REF} VOLTAGE (V_{EE} = 5 V)	$(I_A + I_B)$ OR $\|I_A - I_B\|$ CURRENT DETECTION – THRESHOLD [mA]			
	$R_{EA} = R_{EB} = 45\ \Omega$		$R_{EA} = R_{EB} = 50\ \Omega$	
	$I_A + I_B$	$\|I_A - I_B\|$	$I_A + I_B$	$\|I_A - I_B\|$
V_{REF0} = 1.395 V	2 x 15.5	–	2 x 14.0	–
V_{REF1} = 1.310 V	2 x 14.6	–	2 x 13.1	–
V_{REF2} = 2.855 V	–	71.2	–	64.2
V_{REF3} = 0.640 V	–	16.0	–	14.4
V_{REF4} = 3.335 V	–	83.4	–	75.1

3) AC CHARACTERISTICS

The AC functional circuit diagram of the OKI SLIC is shown in Figure 10.

a) 2-wire terminating impedance

2-wire terminating impedance Z_{to} is given by eq. (3)

$$Z_{to} = (V_L/I_L) = Z_X/(K_i \times K_{V0}) \quad \ldots\ldots\ldots \quad (3)$$

The value of Z_X can be derived from eq. (3) to provide the desired 2-wire terminating impedance.

$$Z_X = Z_{to} \times (K_i \times K_{V0}) \quad \ldots\ldots\ldots\ldots\ldots \quad (4)$$

Both the value of the current gain Ki and the voltage gain K_{V0} are given by table 2.

b) Transmit and receive gain

2-wire to XMIT and REC to 2-wire transmission gain G_{24}, G_{42} are given by eq. (5) and eq. (6) respectively.

$$G_{24} = |V_X/V_L| = |R_s \times K_{V0}/Z_X| \quad \ldots\ldots\ldots \quad (5)$$

$$G_{42} = |V_L/V_R| = \left|\frac{K_{V1} \times K_{V3} \times Z_I}{K_{V0}}\right| \Big/ [Z_I + Z_X/(K_{V0} \times K_i)] \quad \ldots\ldots\ldots\ldots \quad (6)$$

The impedance ZI may be chosen a general transmission impedance 600Ω or 900Ω. The value of R_S may be calculated to provide the disired G_{24} for given Z_X by eq. (4) and K_{V0} by table 2.

$$R_s = |Z_X \times G_{24}/K_{V0}| \quad \ldots\ldots\ldots\ldots\ldots \quad (7)$$

The value of the receive attnuator K_{V3} may be desired from eq. (6) and (4) once ZI is known.

$$K_{V3} = G_{24} \times |(Z_I + Z_{to})/(Z_I \times K_{V1}/K_{V0})| \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (8)$$

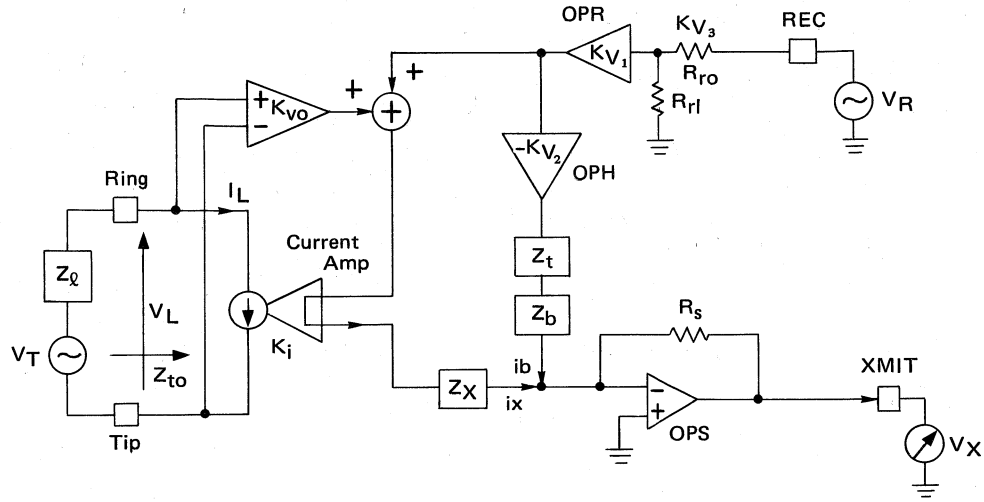


Figure 10 AC Functional Circuit Diagram

c) Transhybrid rejection

Transhybrid rejection is acheived with OKI SLIC by taking advantage of the 180° phase reversal of the current ix at the negative input of OPS amp with respect to receive signal V_R. When the receive signal V_R transmits to 2-wire, the return current ix from 2-wire and the cancel current is apear at the negative input of OPS amp.

These ix and ib are given by eq. (9) and (10).

$$ix = \frac{VR \times K_{V1} \times K_{V3}}{(K_i \times K_{V0})} \times \frac{1}{(Z_l + \frac{Z_x}{K_i \times K_{V0}})} \quad \ldots\ldots\ldots (9)$$

$$ib = -V_R \times K_{V1} \times K_{V2} \times K_{V3}/(Z_b + Z_t) \quad \ldots (10)$$

The value of the impedance Z_b and Z_t are selected to exactly cancel out the return current ix and are determined by eq. (11) and (12).

$$Z_b = K_i \times K_{V0} \times K_{V2} \times Z\ell \ldots\ldots\ldots\ldots (11)$$

$$Z_t = K_{V2} \times Z_X = K_i \times K_{V0} \times K_{V2} \times Z_{to} \ldots (12)$$

The impedance $Z\ell$ may be an actual subscriber line loop impedance, including phone set. The value of K_{V2} is shown table 2.

d) Longitudinal balance

The longitudinal balance is determined by the matching both the gain of the Tip and Ring current drive amp.

The longitudinal balance may be improved by making a little adjustment of either power resistor REA and REB because the gain of the Tip and Ring current drive amp are determined by the ratio of the power resistors and the built-in resistors respectively.

Table 2

Symbol of gain	Actual gain of OKI SLIC	Example gain @ Ry = 4.7 K @ $R_{EA} = R_{EB} = 45\ \Omega$
K_i	$\frac{Ry}{R_{EA} + R_{EB}} \cdot 3.858$	201
K_{V0}	0.167	0.167
K_{V1}	1.60	1.60
K_{V2}	1.517	1.517
$K_i \cdot K_{V0}$	$0.644 \cdot \frac{Ry}{(R_{EA} + R_{EB})}$	33.6
$K_i \cdot K_{V0} \cdot K_{V2}$	$0.977 \cdot \frac{Ry}{R_{EA} + R_{EB}}$	51.0

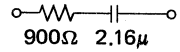
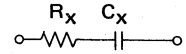
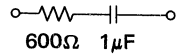
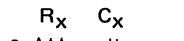
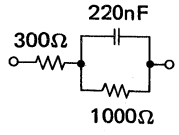
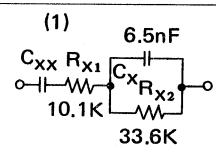
DESIGN EXAMPLES

Table 3 and Table 4 are shown the design examples of the 2 wire terminating impedance component Zx and the two transhybrid rejection impedances Zt, Zb, in the case of $R_{EA} = R_{EB} = 45\ \Omega$ and Ry = 4.7 KΩ.

III

(1) 2-wire terminating impedance Zx.

Table 3

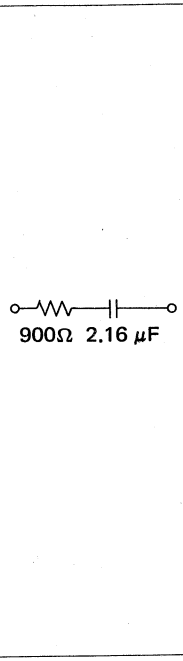
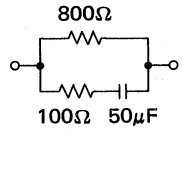
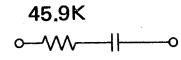
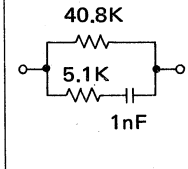
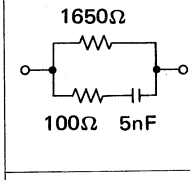
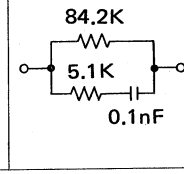
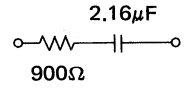
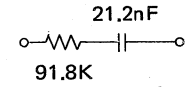
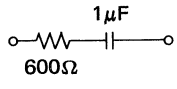
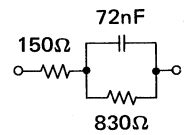
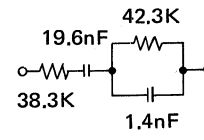
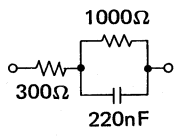
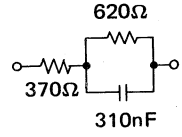
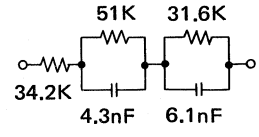
No.	Required 2 wire terminating impedance Zto	Determined impedance from table 2 Zx. (Rx. Cx)	Remark
1			Apply to North America (AT&T) (See CCITT rec. Q517)
2			Apply to NTT (See CCITT rec. Q517)
3			Apply to BT (See CCITT rec. Q517)

Note (1) C_{xx}: needed to be provided to block the DC ($\simeq 0.68\mu F \pm 50\%$)

(2) When a required 2-wire return loss cannot be obtained even when an externaly impedance Z_x is selected, it is possible to improve the characteristic merely by adjusting the externally resistor R_y.

(2) Transhybrid rejection impedances Zt and Zb.

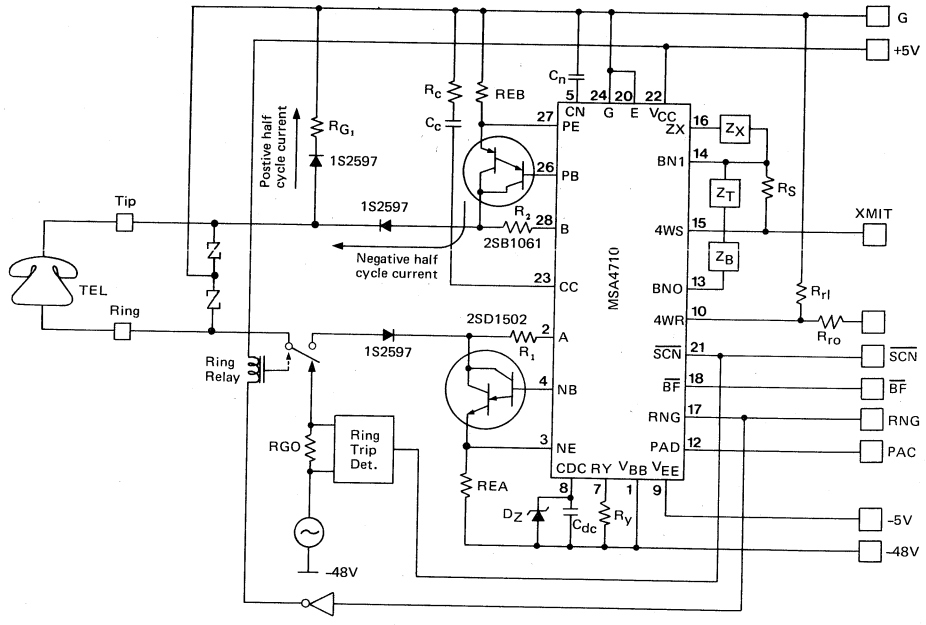
Table 4

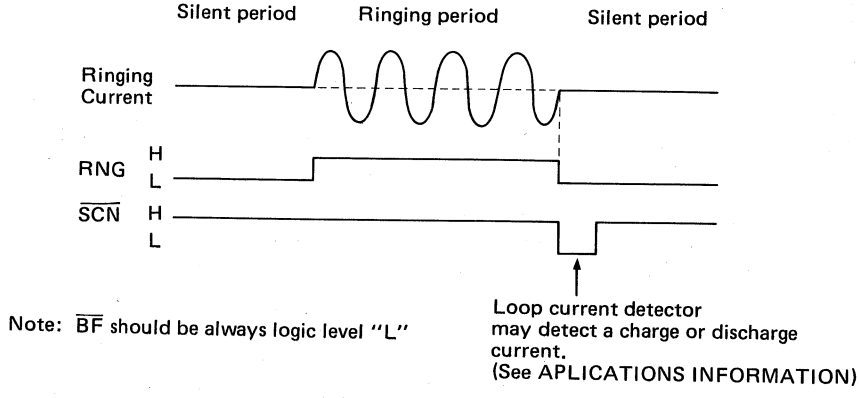
No.	2-wire terminating impdeance Zto (1)	2-wire subscriber line loop impedance (1)	Determined impedances from table 2		Remark
			Zt	Zb	
1					North America nonloaded line
2					North America loaded line
3			 $(Z_t + Z_b)$		North America special service line
4			 $(Z_t + Z_b)$		NTT
5					BT

Note (1): See LSSGR and CCITT redbook Rec. Q517.

III

RINGING SIGNAL INSERTION





Note: $\overline{BF}$ should be always logic level "L"

Figure 11 Signal Insertion Circuit Diagram

MSA4722-1

SOLID-STATE RELAYS FOR SLIC IN THE PABX

GENERAL DESCRIPTION

The MSA4722-1 is a solid-state relay function LSI for SLIC in the PABX and it consists of eight high-voltage PNPN Switches. The MSA4722-1 is designed to provide R.T functions for SLIC.

This device can replace conventional electromagnetic relays.

FEATURES

- R (Ringing signal sending & Ring trip interface), T (Network test switch) and Cutoff (Separate the Battery-Feed circuit from subscriber line) functions on chip.
- High voltage functions integrated in dielectric isolation technology.
- Low ON-Resistance & High OFF-Resistance.
- Size and Weight reduction over electro-magnetic relays.
- 22 pin plastic DIP package.

III

FUNCTIONAL BLOCK DIAGRAM

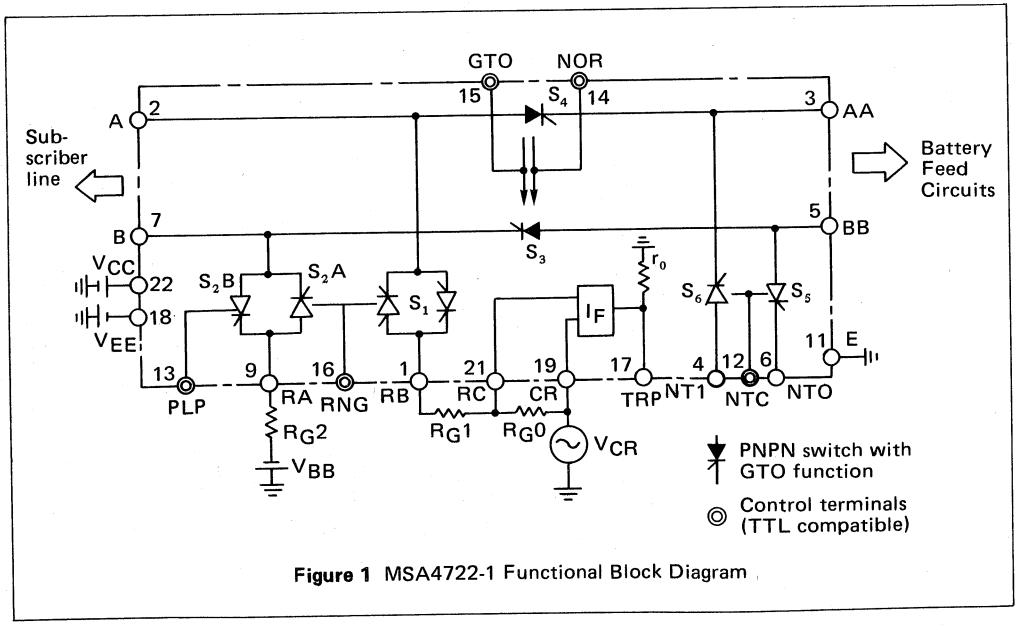
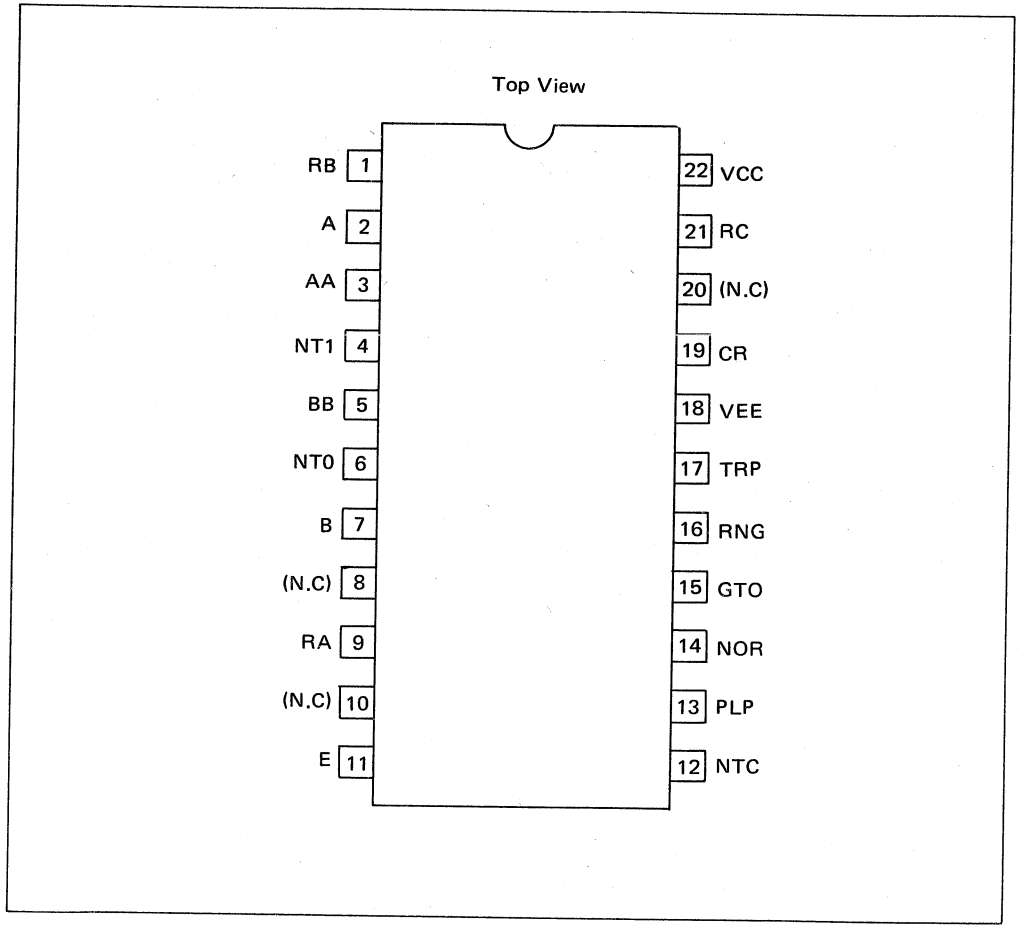


Figure 1 MSA4722-1 Functional Block Diagram

PIN CONFIGURATION



PIN DESCRIPTION

Name	Pin No.	Function
RB	1	Ringing signal sending power resistor RG1 input and connected to Ring line through the switch S1. The resistor value is 510 Ω, 1 W.
A	2	Connected to Ring line.
AA	3	Connected to the poled negative terminal of the Battery-feed circuit.
NT1	4	Connected to the Network test equipment.
BB	5	Connected to the poled positive terminal of the Battery-feed circuit.
NT0	6	Connected to the Network test equipment.
B	7	Connected to Tip line.
N.C.	8	Unused.
RA	9	Connected to the power resistor RG2 which supply the battery for Tip line in order to feed the DC current for detecting the customer's off-hook. The value of the resistor RG2 is 220 Ω, 0.25 W.
N.C.	10	Unused.
E	11	Connected to ground.
NTC	12	Network test switches S5, S6 control input. A logic level "H" connects the Battery-feed circuit to the Network test equipment through S5 and S6.
PLP	13	Superimposing VBB switches S2B control input. A logic level "H" superimposes VBB during the Ringing signal is sent.
NOR	14	Line cutoff switches S3, S4 control input. A logic level "H" turns on both S3 and S4.
GT0	15	The gate turn-off function of the PNPN switches S3, S4 control input. A logic level "H" gets the loop current interrupted by these switches.
RNG	16	Ringing signal sending switches S1, S2A control input. A logic level "H" sends ringing signal to the customer.
TRP	17	The ringing voltage output. This voltage is proportional to the voltage between the terminals RC and CR. The output impedance is apr. 10 kΩ.
VEE	18	-5 V input.
CR	19	Ringing signal generator input and connected to the ringing signal feed resistor RG0. The resistor value is 220 Ω, 0.5 W.
N.C.	20	Unused.
RC	21	Ringing signal feed resistors RG0 and RG1 input. The voltage between RC and CR applies to the Ring trip interface circuit (IF).
VCC	22	+5V input.

ABSOLUTE MAXIMUM RATING

$T_a = 25°C$

Rating		Symbol	Value	Unit
Supply Voltage		V_{CC}	−0.5 ~ +7	V
		V_{EE}	−7 ~ +0.5	
Anode-cathode Current Continuous	S_1, $S_{2A, B}$	I_{AK}	±180	mA
	S_3, S_4		170	
	S_5, S_6		120	
Operating Ambient Temperature Range		T_a	0 ~ +70	°C
Storage Temperature Range		T_{stg}	−55 ~ +125	°C
Junction Temperature Range		T_j	+125	°C

RECOMMENDED OPERATING CONDITIONS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	+4.75 ~ +5.25	V
	V_{EE}	−5.25 ~ −4.75	
Ringing Signal Voltage	V_{CR}	69 ~ 83	V_{rms}

ELECTRICAL CHARACTERISTICS

(Unless otherwise noted T_A = 0 to 70°C)

Parameters		Symbol	Conditions		Min	Max	Unit
Supply current — OFF Hook		I_{VCC}	Figure 2		—	15	mA
Logic input voltage	High level	V_{IH}	—	NOR(1) GTO PLP RNG NTC	2.0	—	V
	Low level	V_{IL}			—	0.5	
Logic input current per one fan-in	High level	I_{IH}	$V_{IH} = V_{CC}$		—	0.1	mA
	Low level	I_{IL}	V_{IL} = 0V		-1.2	—	
Cross point ON drive current	P-Gate	I_{PG}	Figure 3	$S_1 \sim S_6$	—	1.2	mA
	N-Gate	I_{NG}		S_1	—	1.5	
Crosspoint off drive current		I_{GOFF}	Figure 3	S_3, S_4	—	3	mA
Breakdown voltage		V_{BO}	—	S_1	-320	320	V
				$S_2 \sim S_6$	-260	260	
Minimum voltage ramp Which could fire the SCR under transient conditions		dv/dt			200/0.8	—	V/μs
Interrupt DC current capability		I_{OFF}	GTO = "H"	S_3, S_4	5	—	mA
Holding current		I_H		S_5, S_6	0.1	—	mA
ON voltage		V_F	I_F = 30 mA	$S_1 \sim S_6$	—	1.4	V
Dynamic ON resistance		R_{ON}	Center current I_F = 30 mA	S_3, S_4	—	10	Ω
Relative ON resistance error		ΔR_{ON}	$S_3 \sim S_4$		—	1	Ω
OFF state resistance		R_{OFF}	V_{AK} = 50V		150	—	MΩ
Ringtrip interface circuit transfer ratio		K	Figure 4 V_{in} = ±8V		0.305	0.439	—
TRP output resistance		R_{out}			6.2	13.8	kΩ

Note (1) The fan-in of GTO, RNG and PLP is two, respectively.
Other logic fan-in is one.

III

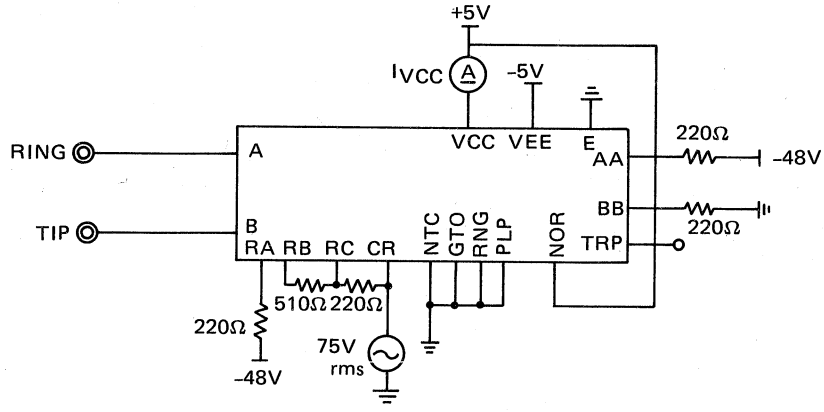


Figure 2 Supply Current Test Circuit

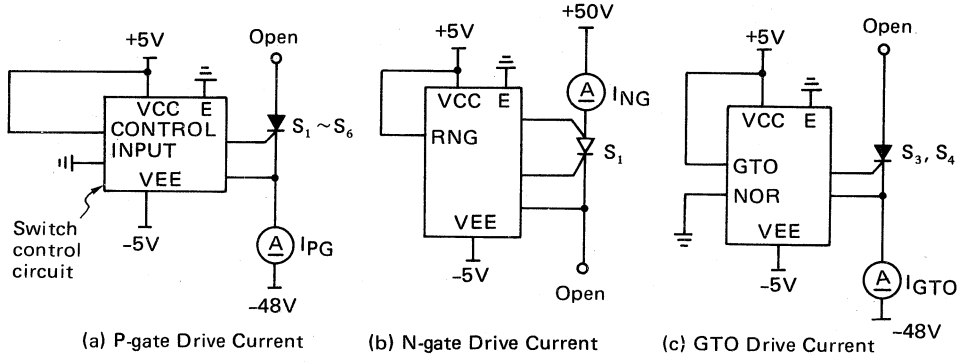


Figure 3 Switch Drive Current Test Circuit

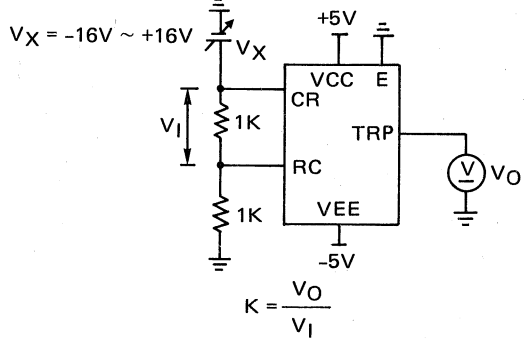


Figure 4 Ring Trip Interface Circuit Transfer Ratio Test Circuit

APPLICATIONS INFORMATION

1) Overvoltage Protection

The MSM4722-1 consists of 8 high voltage withstanding PNPN switches.

But overvoltage protection circuit is required and it must keep the voltage at the line interface terminals A and B the value indicated eq. (1) during lightning or transient high voltage strikes.

$$Vclp = Vbo - \sqrt{2} \times Vcr \quad \ldots\ldots\ldots (1)$$

Vclp : 2nd arrestor clamping voltage.
Vcr : Ringing signal voltage [r.m.s].
Vbo : Breakdown voltage of S1.

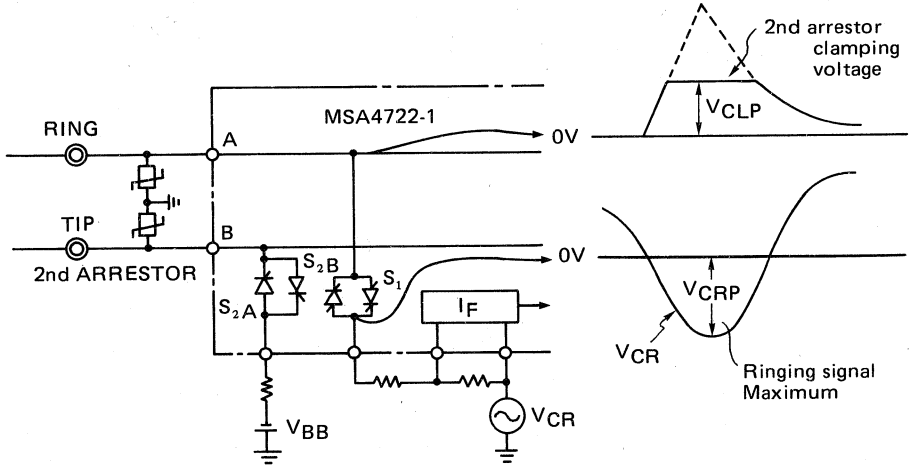


Figure 5 Overvoltage Protection Diagram

2) Ringing Signal Sending Time Chart

The OKI RT-LSI can send the ringing and silent signal to the customer and these signal sending method is shown below and in Figure 6.

The ringing signal can be sent to the customer through the switches S1, $S2_A$, $S2_B$, during the RNG and PLP are logic level "H".

The silent signal can be sent by the Battery-feed circuit through the Cutoff switches S_3, S_4 during NOR is a logic level "H".

Some guard timing are required when ringing and silent signal are sent, because RT consists of the self-holding PNPN switches and the holding-current of these switches is very small.

The ringing and silent signal sending time chart is shown in Figure 7.

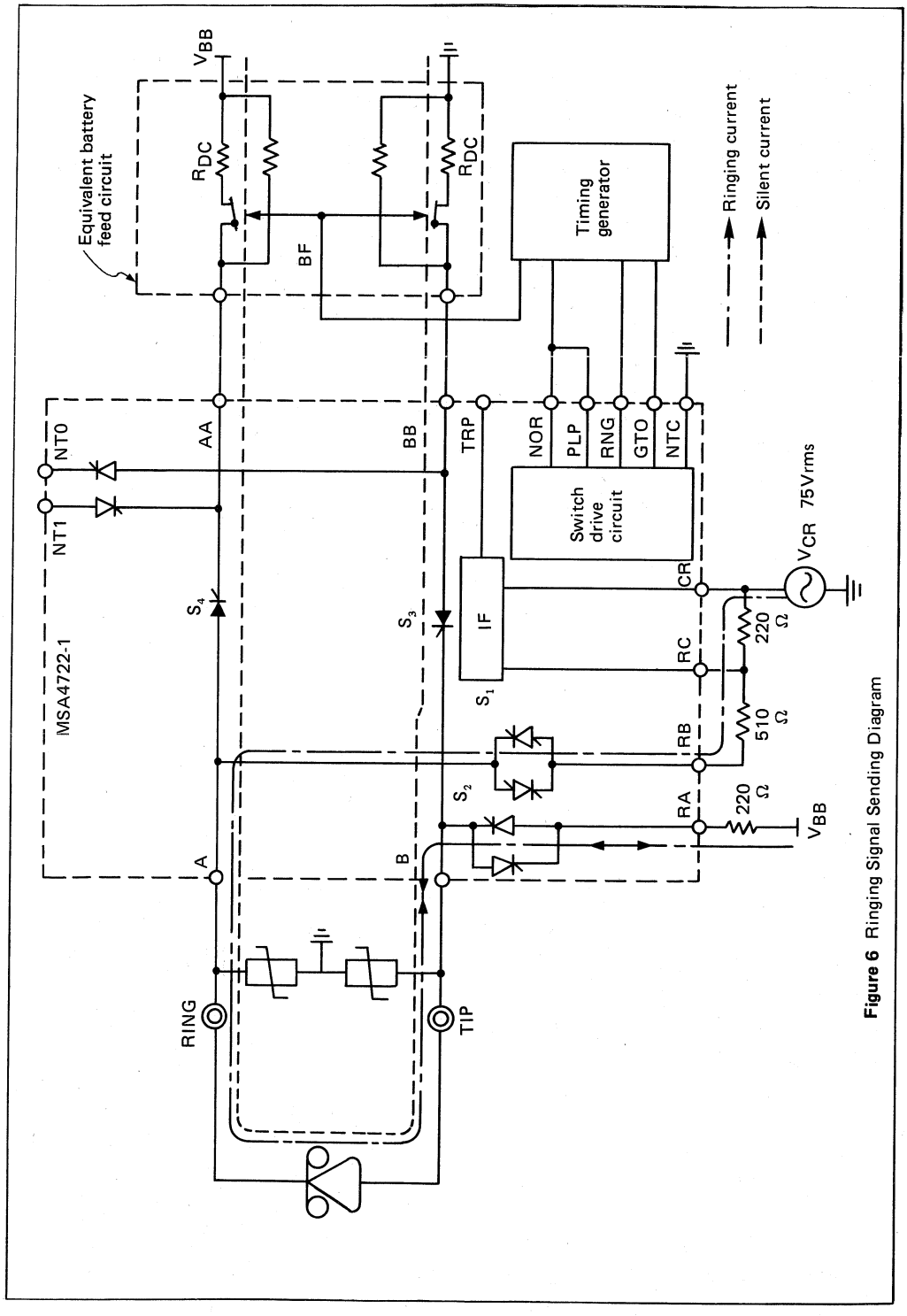
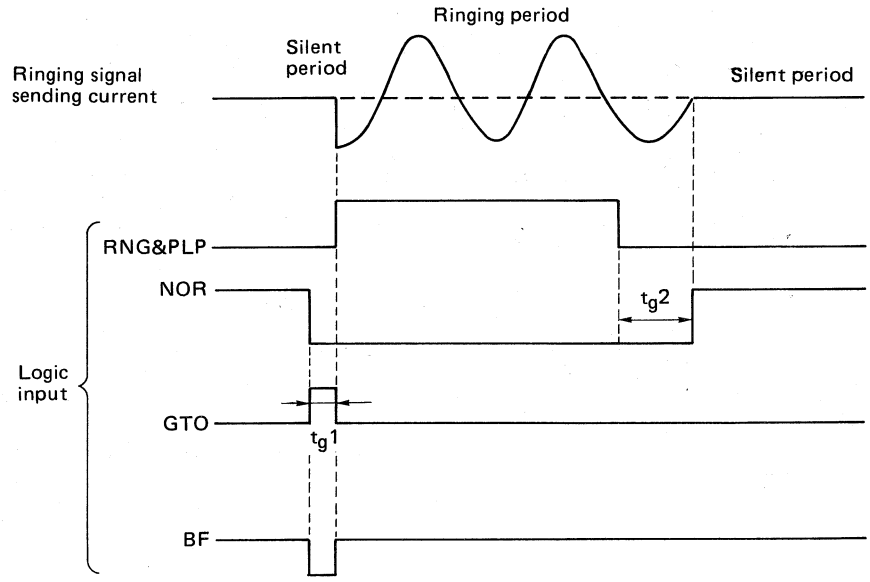


Figure 6 Ringing Signal Sending Diagram



t_g1 : prevents the switches S_3 and S_4 from holding by flowing current through a line leakage resistance. ($\geqq$1 ms)

t_g2 : needs to be not shorter than the half cycle time of ringing signal frequency.
(ex. $\geqq \frac{1}{2 \times 16\ Hz} = 32$ ms)

Figure 7 Ringing/Silent Signal Sending Time Chart

III

3) Cut-off from the Battery-feed Circuit Method

As the gate turn-off capability of the battery polarity reverse switches S_3, S_4 is not greater than the loop current, line cut-off from the SLIC must be performed by the following sequence.

a) The Battery-feed circuit is turned off in order to reduce the loop current to be interrupted by gate turn-off function of the switches S_3 and S_4.
b) The logic input NOR is turned "L" and the GTO is turned "H" in order to interrupt the leakage current flowing from the Battery-feed circuit to the line.
c) GTO input is turned "H" 1 ms after the cutoff swithes S_3, S_4 are completely turned off, in order to prevent the GTO driving current from flowing in the line.

The line cut-off time chart is shown in Figure 8.

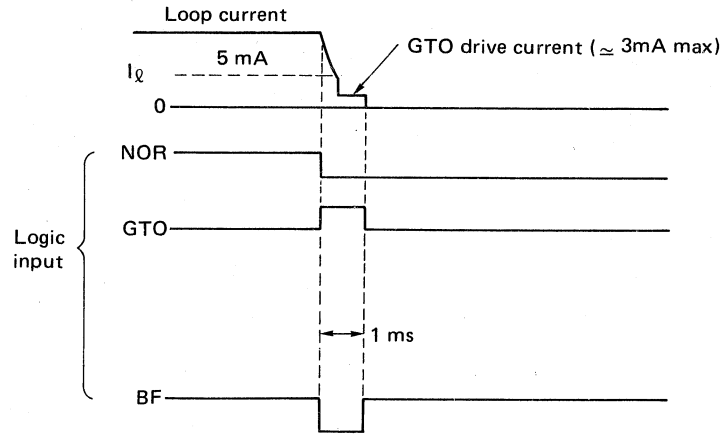


Figure 8 Line Cut-off Time Chart

4) Ring Trip Interface Circuit Characteristics

The Ring trip interface circuit (IF) attenuates the voltage generated on between terminals CR and RC, and transmits to the TRP terminal.

The IF circuit diagram is shown in Figure 9.

As the level shift transistors' collectors are connected to the ground through the output resistor, the phase difference between ringing generator voltage and ringing signal current distorts the output wave-form of the TRP.

Figure 10 shows this case. The IF transmission characteristics is shown in Figure 10 and Figure 11. The ring trip detection may be possible by connecting an appropriate low-pass filter and comparator to the TRP terminal.

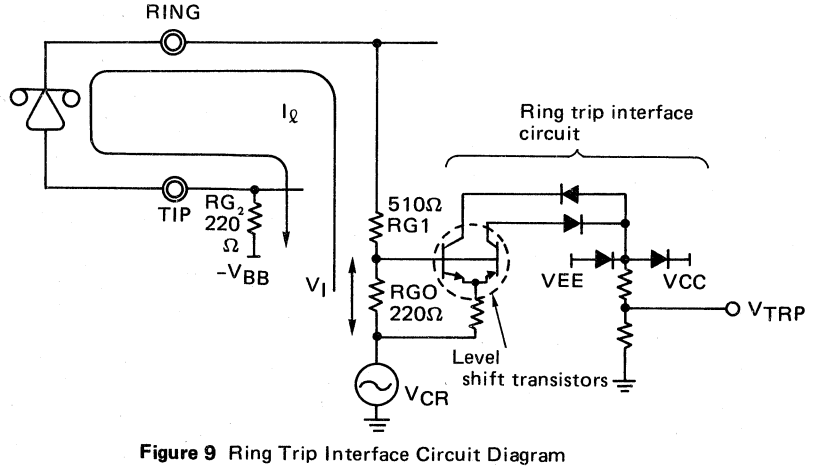


Figure 9 Ring Trip Interface Circuit Diagram

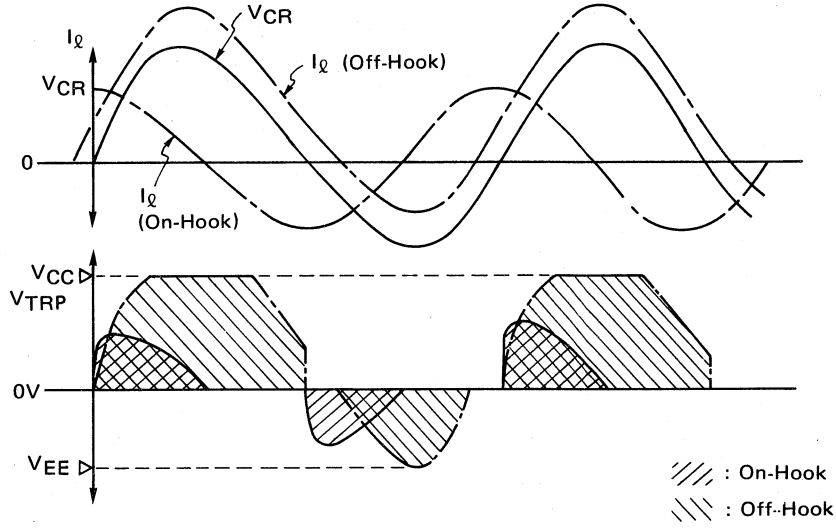


Figure 10 Ring Trip Interface Dynamic Characteristic

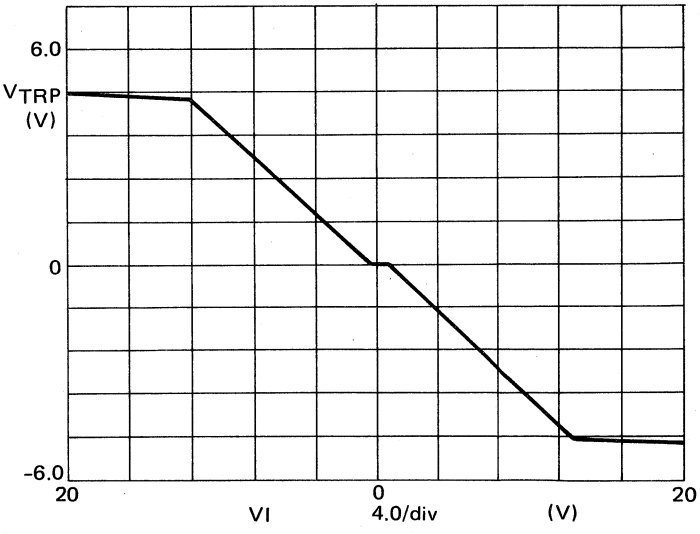


Figure 11 Ring Trip Interface Static Characteristic

III

MSM6912

PCM CHANNEL FILTER

GENERAL DESCRIPTION

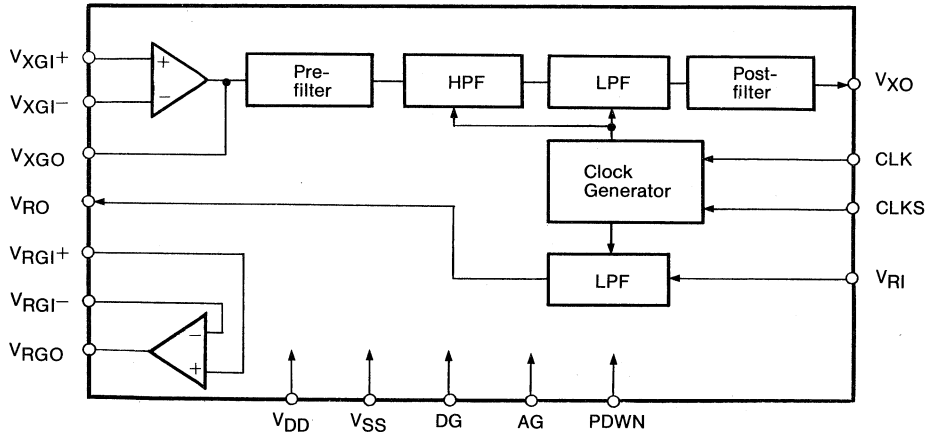
The MSM6912 is a PCM channel filter LSI which is fabricated by OKI's low power consumption CMOS silicon gate technology.

It consists of pre-filter, HPF, post filter and two LPF's.

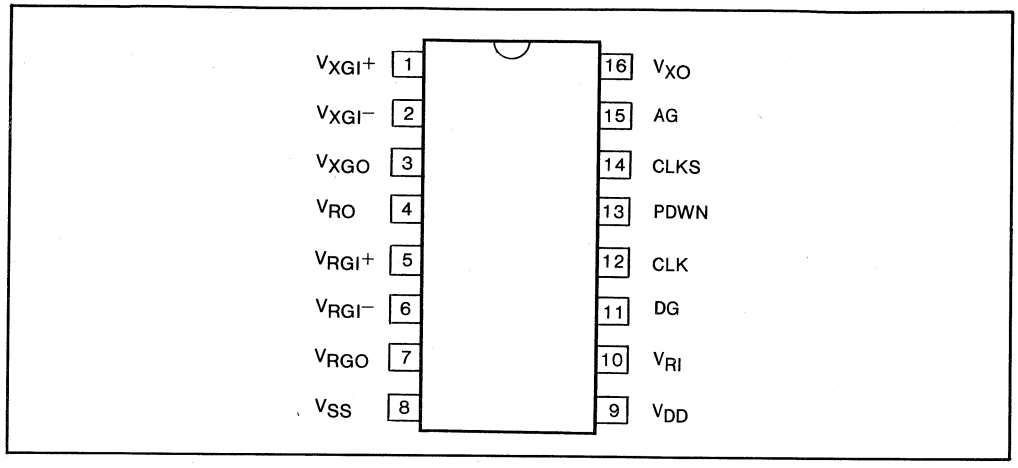
FEATURES

- CCITT G.712 standard
- 50/60 Hz rejection filter on-chip
- SIN x/x compensation filter on-chip
- External gain adjustment, both transmit and receive filters
- Power-down mode available
- 128 KHz or 2048 KHz external clock for operation
- Power supply, ±5 V
- 16-pin ceramic DIP package

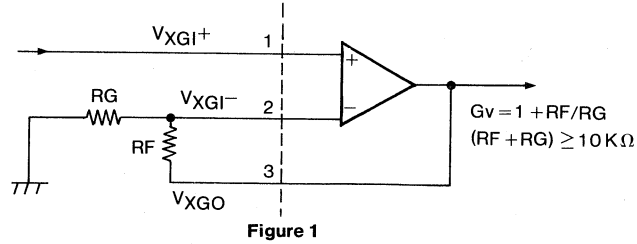
BLOCK DIAGRAM



PIN CONFIGURATION



PIN DESCRIPTION

Pin No.	Pin Name	Function
1	$V_{XGI}+$	$V_{XGI}+$ is the non-inverting input of the gain-setting Op Amp in the transmit filter section. The input analog signal is typically applied to this pin.
2	$V_{XGI}-$	$V_{XGI}-$ is the inverting input of the gain-setting Op Amp in the transmit filter section.
3	V_{XGO}	V_{XGO} is connected to the output of the gain-setting Op Amp in the transmit filter section. An appropriate voltage gain can be set as shown in Figure 1 below.  **Figure 1** As the transmit filter section has a gain of approx. +3 dB excluding this amplifier, a suitable level diagram has to be selected. The DC offset voltage of V_{XGO} becomes 50·Gv (mV) in the worst case. The load resistance connected to V_{XGO} should be greater than 10 KΩ.
4	V_{RO}	V_{RO} is the analog output of the receive filter. Because the output impedance is not so low, it is better to use the gain setting OP Amp as a output buffer. The resistive loads connected to V_{RO} should be greater than 10 KΩ.
5	$V_{RGI}+$	$V_{RGI}+$ is the non-inverting input of the gain setting Op Amp in the receive filter section.
6	$V_{RGI}-$	$V_{RGI}-$ is the inverting input of the gain setting Op Amp in the receive filter section.

III

Pin No.	Pin Name	Function
7	V_{RGO}	V_{RGO} is the output of the gain setting Op Amp in the receive filter section. An appropriate voltage gain can be set as shown in Figure 2 and 3.

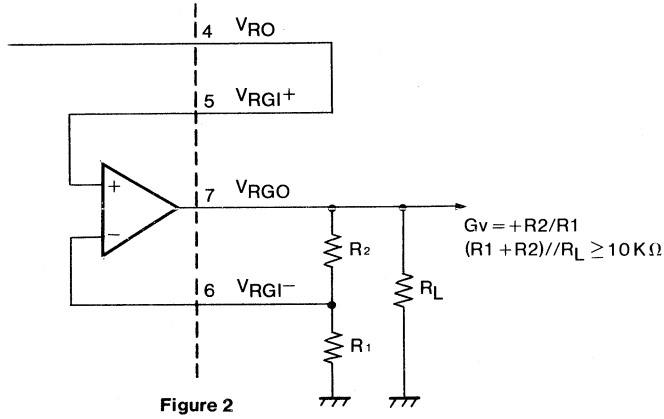


Figure 2

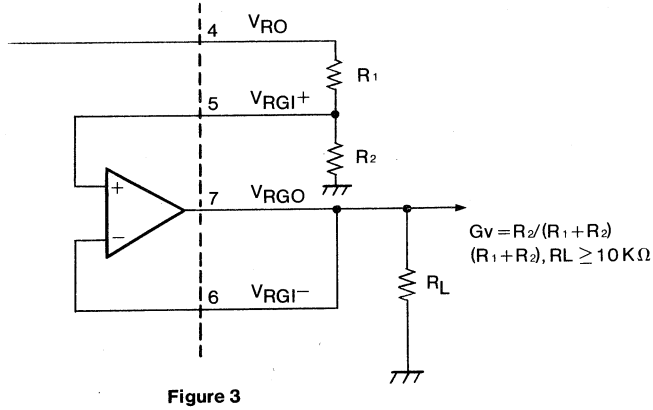


Figure 3

Use Figure 2 for amplification and Figure 3 for attenuation. As the receive filter section has a gain of approx. 0 dB excluding this amplifier, a suitable level diagram has to be calculated.
The DC offset voltage of V_{RGO} becomes as follows in the worst case;

Figure 2 ... (200 + 50) · Gv = 250 · Gv (mV)
Figure 3 ... 200 · Gv + 50 (mV)

The resistive loads connected to V_{RGO} should be greater than 10 KΩ.

Pin No.	Pin Name	Function
8	V_{SS}	V_{SS} is the negative supply pin. The voltage supplied to this pin should be $-5V \pm 5\%$.
9	V_{DD}	V_{DD} is the positive supply pin. The voltage supplied to this pin should be $+5V \pm 5\%$.
10	V_{RI}	V_{RI} is the analog input to the receive filter. The receive signal is typically generated by the decoder section of a companding CODEC (ex. MSM6917AS). The receive filter provides the sin x/x correction over the passband.
11	DG	This pin is connected to the digital system ground.
12	CLK	CLK is the digital clock signal input. Two clock frequency (128 KHz, 2,048 KHz) can be applied. The desired clock frequency is selected by the CLKS input. For proper operation, this clock should be tied to the receive clock of the CODEC.
13	PDWN	This control input enables MSM6912AS in the powerdown mode. Power down occurs when the signal of this input is pulled high.
14	CLKS	This control pin is used to select the desired clock frequency.
15	AG	This pin is connected to the analog system ground.
16	V_{XO}	V_{XO} is the analog output of the transmit filter. The output voltage range is ± 2.5 V and the output DC offset voltage is less than 200 mV. This output should be AC-coupled to the encoder section of the CODEC. The resistive load connected to V_{XO} should be greater than 5 KΩ.

CLK (Pin 12)	CLKS (Pin 14)
128 KHz	Digital "L"
2,048 KHz	Digital "H"

III

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD}	Ta=25°C with respect to DG and AG	−0.3 ~ 7	V
	V_{SS}		+0.3 ~ −7	
Digital input voltage	V_{DIN}		−0.3 ~ V_{DD} +0.3	V
Analog input voltage	V_{AIN}		V_{SS}−0.3 ~ V_{DD}+0.3	V
Operating temperature	T_{OP}		0 ~ 70	°C
Storage temperature	T_{ST}		−55 ~ 150	°C

Recommended Operating Conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply voltage	V_{DD}	With respect to DG and AG	4.75	5	5.25	V
	V_{SS}		−4.75	−5	−5.25	V
Operating temperature	T_{OP}		0		70	°C

DC and Digital Interface Characteristics

(V_{DD} = +5V ± 5%, V_{SS} = −5V ± 5%, Ta = 0 ~ 70°C)

Parameter	Symbol	Conditions	Limits			Unit
			Min	Typ	Max	
Standby supply current	I_{DDS}	PDWN = V_{IH}	–	0.01	1	mA
	I_{SSS}		–	0.01	1	mA
Operating supply current	I_{DDO}	PDWN = V_{IL}	–	5	10	mA
	I_{SSO}		–	5	10	mA
Input leakage current	I_{IL}	V_I = 0V	–	–	10	μA
	I_{IH}	V_I = 5V	–	–	10	μA
Input voltage	V_{IL}	With respect to DG	–	–	0.8	V
	V_{IH}		2.4	–	–	V

Analog Interface, Gain Setting Amplifier and Transmit Filter

(V_{DD} = +5V ± 5%, V_{SS} = −5V ± 5%, Ta = 0 ~ 70°C)

	Parameter	Symbol	Conditions	Limits			Unit
				Min	Typ	Max	
Gain setting amplifier	Input leakage current $V_{XGI}+$ $V_{XGI}-$	I_{BX}	$-3.2V \leq V_{IN} \leq +3.2V$	–	–	10	μA
	Input resistance $V_{XGI}+$ $V_{XGI}-$	R_{IX}		2	–	–	MΩ
	Input offset voltage	V_{OSXI}	$-3.2V \leq V_{IN} \leq +3.2V$	–	–	50	mV
	DC open loop voltage gain	A_{VX}		66	–	–	dB
	Open loop unity gain bandwidth	fcx		–	2	–	MHz
	Load capacitance	C_{LX1}		–	–	200	PF
	Load resistance	R_{LX1}		10	–	–	KΩ
	Output voltage swing	V_{OX1}	$RL \geq 10K\Omega$	±2.5	–	–	V
Filter	Output resistance	R_{OX1}		–	–	100	Ω
	Output offset voltage	V_{OSX}	$V_{XGI}+ = AG$ Input OP Amp at Unity gain	–	–	200	mV
	Load capacitance	C_{LX2}		–	–	200	PF
	Load resistance	R_{LX2}		5	–	–	KΩ
	Output voltage swing	V_{OX2}	$R_L \geq 5K\Omega$	±2.5	–	–	V

Analog Interface, Receive Filter and Gain Setting Amplifier

(V_{DD} = +5V ± 5%, V_{SS} = −5V ± 5%, Ta = 0 ~ 70°C)

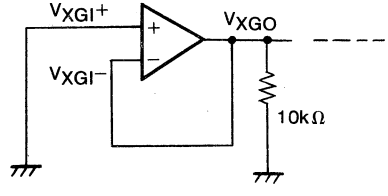
	Parameter	Symbol	Conditions	Limits			Unit
				Min	Typ	Max	
Filter	Input leakage current	I_{BR1}	$-3.2V \leq V_{IN} \leq +3.2V$	–	–	10	μA
	Input resistance	R_{IR1}		2	–	–	MΩ
	Output resistance	R_{OR1}		–	–	200	Ω
	Output offset voltage	V_{OSR}	$V_{RI} = AG$	–	–	200	mV
	Load capacitance	C_{LR1}		–	–	200	PF
	Load resistance	R_{LR1}		10	–	–	KΩ
	Output voltage swing	V_{OR1}	$R_L \geq 10K\Omega$	±2.5	–	–	V
Gain setting amplifier	Input leakage current $V_{RGI}+$, $V_{RGI}-$	I_{BR2}	$-3.2V \leq V_{IN} \leq +3.2V$	–	–	10	μA
	Input resistance $V_{RGI}+$, $V_{RGI}-$	R_{IR2}		2	–	–	MΩ
	Input offset voltage	V_{OSRI}	$-3.2V \leq V_{IN} \leq +3.2V$	–	–	50	mV
	DC open loop voltage gain	A_{VR}		66	–	–	dB
	Open loop unity gain bandwidth	f_{CR}		–	2	–	MHz
	Output resistance	R_{OR2}	At unity gain	–	–	20	Ω
	Load capacitance	C_{LR2}		–	–	200	PF
	Load resistance	R_{LR2}		10	–	–	KΩ
	Output voltage swing	V_{OR2}	$RL \geq 10K\Omega$	±2.5	–	–	V

Transmit Filter Transfer Characteristics

(V_{DD} = +5V ± 5%, V_{SS} = −5V ± 5%, Ta = 0 ~ 70°C)

Parameter		Symbol	Conditions	Limits				Unit
				Amp	Min	Typ	Max	
Absolute passband gain (900 Hz)		G_{AX}	Input = 0 dBmo ≅1.25 Vrms Output = +3 dBmo ≅1.77 Vrms	–	2.8	3.0	3.2	dB
Relative gain (to GAX)	Below 60 Hz	G_{RX}			–	−20		
	300~3000 Hz				−0.25	–	+0.1	
	3300 Hz				−0.35	–	+0.1	
	3400 Hz			0 dB	−0.85	–	+0.1	
	4000 Hz				–	–	−14	
	4600 Hz and above				–	–	−28	
Gain variation with temperature		G_{AXT}	Input = 0 dBmo 900 Hz		–	0.0005	–	dB/°C
Gain variation with supplies		G_{AXS}	Input = 0 dBmo 900 Hz Supplies: ±5%		–	0.05	–	dB/V
Crosstalk, Receive to Transmit		CT_{RX}	*1		–	–	−60	dB
Total C message noise at output		N_{CX1}			–	8	–	dBrnco
Total C message noise at output		N_{CX2}		20 dB	–	10	–	
Differential envelope delay		D_{DX}	0.9 ~ 2.6 KHz	0 dB	–	–	60	μS
Absolute delay		D_{AX}	900 Hz		–	200	–	
Single frequency distortion products		D_{PX}	V_{XO} = +3 dBmo 900 Hz	20 dB	–	–	−45	dB
Positive power supply rejection ratio		P_{SRR1}	V_{XO}, 900 Hz V_{DD}	0 dB	25	30	–	
Negative power supply rejection ratio		P_{SRR2}	V_{XO}, 900 Hz V_{SS}		23	28	–	

*1 V_{RI} = 0 dBmo, 900 Hz



Receive Filter Transfer Characteristics

(V_{DD} = +5V ± 5%, V_{SS} = −5V ± 5%, Ta = 0 ~ 70°C)

Parameter		Symbol	Conditions	Limits				Unit
				Amp	Min	Typ	Max	
Absolute passband gain (900 Hz)		G_{AR}	Input = 0 dBmo = 1.25 Vrms	0 dB	−0.25	−0.1	0	dB
Relative gain (to GAR)	Below 300 Hz	G_{RR}	Output = +3 dBmo = 1.77 Vrms With sin x/x correction where x = πf/8000		−0.25	–	+0.1	
	300~3000 Hz				−0.25	–	+0.1	
	3300 Hz				−0.35	–	+0.1	
	3400 Hz				−0.85	–	+0.1	
	4000 Hz				–	–	−14	
	4600 Hz and above				–	–	−28	
Gain variation with temperature		G_{ART}	Input = 0 dBmo 900 Hz		–	0.0005	–	dB/°C
Gain variation with supplies		G_{AXS}	Input = 0 dBmo 900 Hz Supplies: ±5%		–	0.05	–	dB/V
Crosstalk, transmit to receive		CT_{XR}	*1		–	–	−60	dB
Total C message noise at output		N_{CR}			–	7	–	dBrnco
Differential envelope delay		D_{DR}	0.9 ~ 2.6 KHz		–	–	120	μs
Absolute delay		D_{AR}	900 Hz		–	120	–	
Single frequency distortion products		D_{PR}	V_{RGO} = +3 dBmo 900 Hz *2		–	–	−50	dB
Positive power supply rejection ratio		P_{SRR3}	V_{RGO}, 900 Hz V_{DD}		30	35	–	
Negative power supply rejection ratio		P_{SRR4}	V_{RGO}, 900 Hz V_{SS}		30	35	–	

*1 V_{XO} = +3 dBmo, 900 Hz
V_{RI} = AG

*2 Removing the component of 128 KHz

MSM6913

SERIAL PARALLEL CONVERTER

GENERAL DESCRIPTION

The MSM6913 is a serial-parallel converter LSI which is fabricated by OKI's low power consumption CMOS silicon gate technology. The MSM6913 has 8 data signal input pins and 8 data signal output pins, and also has the row-column converting function to replace rows with columns on a matrix with 8 rows and 8 columns considering the 8 data signal pins as the row and the 8 bits, the depth of data, as the column. This function realizes the parallel-serial conversion to convert the input data with 8 cycles of 8-bit parallel data into 8 output data of 8-bit serial data, and the serial-parallel conversion to convert 8 input data of 8-bit serial data into the output data with 8 cycles of 8-bit parallel data.

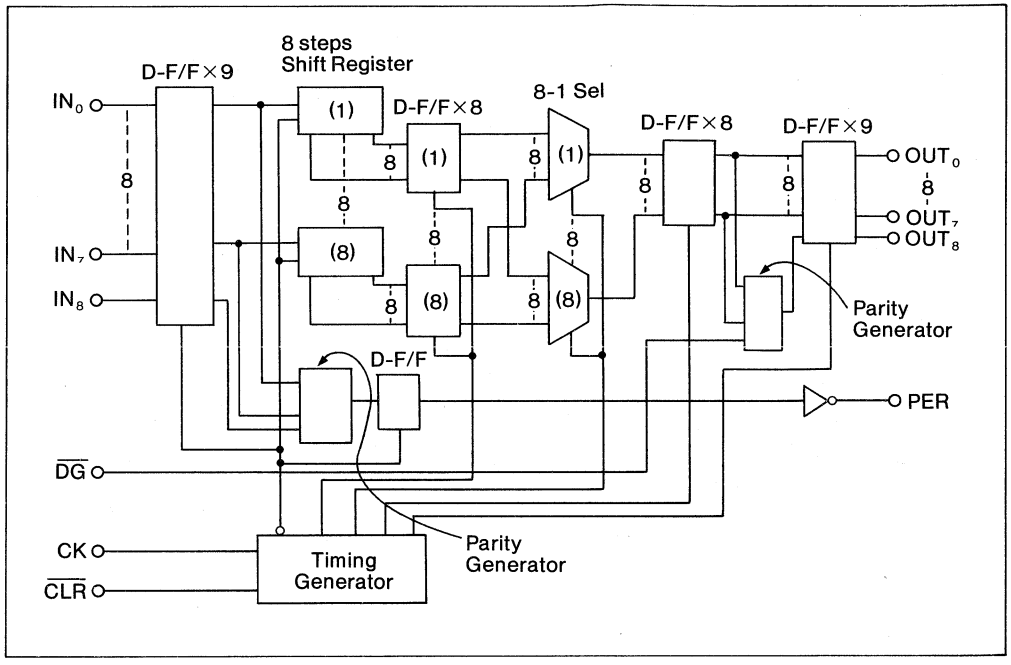
The MSM6913 is also provided with functions to perform the parity check for 8-bit data input signal + parity bit and the parity generation for 8-bit data output signal.

All data except that on the $\overline{DG}$ pin are synchronized with the clock. 9MHz clock can be used for its operation.

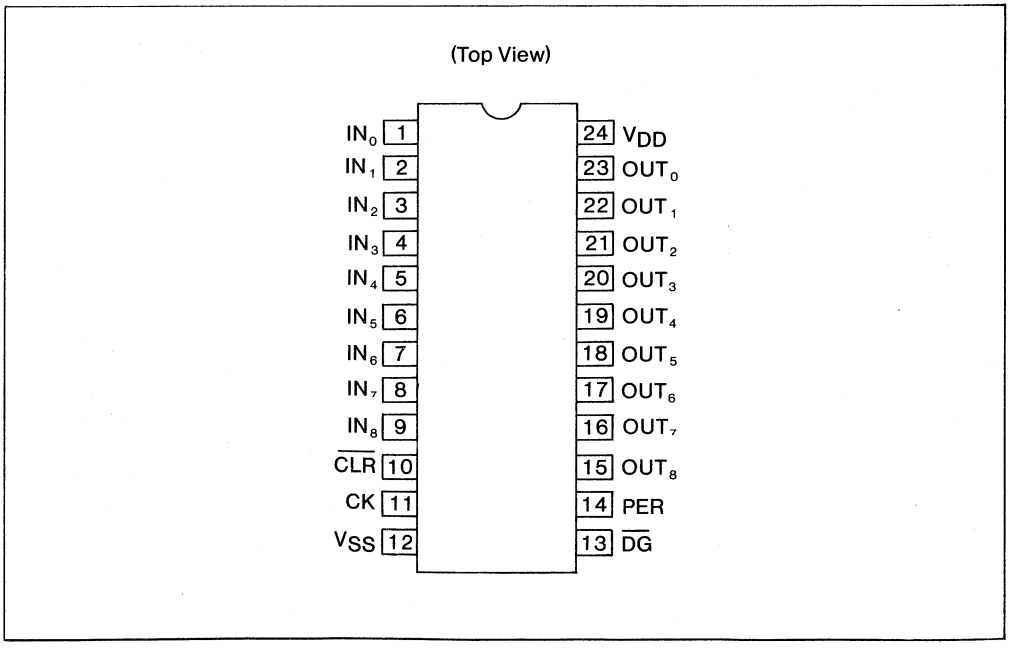
FEATURES

- Serial conversion for 8-bit parallel signal and parallel conversion for 8-bit serial signal
- 9MHz high-speed switching
- Built-in parity-check circuit for data input signal
- Built-in parity-generation circuit for data output signal
- 5V single power supply
- 24-pin plastic DIP package, 24-pin ceramic DIP package

BLOCK DIAGRAM



PIN CONFIGURATION



PIN DESCRIPTION

Pin Name	Pin No.	Function
$IN_0 \sim IN_8$	1 ~ 9	1) Octet interleave serial HW input pin In this case, 8-bit data + parity (serial-parallel conversion) 2) 8-bit data + parity parallel HW input pin Has the parity check function for input data and the output is the octet interleave serial (parallel-serial conversion).
$OUT_0 \sim OUT_8$	23 ~ 15	Corresponding to Items 1) and 2) of INx above. 1) 8-bit data + parity parallel HW output pin In this case, the input is the octet interleave serial HW (serial-parallel conversion). 2) Octet interleave serial HW output pin In this case, the input is the octet interleave parallel HW (parallel-serial conversion).
PER	14	Output pin of parity check result for input data of 8-bit data + parity parallel HW during parallel-serial conversion
$\overline{DG}$	13	Input pin of specified data for odd and even number sides of parity generation circuit during serial-parallel conversion
CK	11	Clock input pin
$\overline{CLR}$	10	Clear input pin

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Condition	Ratings	Unit
Supply voltage	V_{DD}	Ta = 25°C V_{SS} = 0V	−0.3 ~ +7	V
Input voltage	$V_{IN\ MAX}$	Ta = 25°C	V_{DD} + 0.5	V
	$V_{IN\ MIN}$		V_{SS} − 0.5	V
Operation temperature	T_{OP}	———	0 ~ +70	°C
Storage Temperature	T_{STR}	———	−65 ~ 150	°C

III

Recomended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Remark
Supply voltage	V_{DD}	4.75	5	5.25	V	5V ± 5%
	V_{SS}	0	0	0		
Operational temperature	T_{OP}	0	–	70	°C	
Clock duty	$D\phi$	–	50	–	%	
Input transit time	t_{INr}	–	10	–	nS	
	t_{INf}	–	10	–		
Input voltage	V_{IH}	2.2	–	V_{DD}	V	
	V_{IL}	0	–	0.8		

D.C. Characteristics

(V_{DD} = 5V±5% Ta = 0°C ~ 70°C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input current	I_{IL}	V_{IL} = 0V	−10	–	–	μA
	I_{IH}	$V_{IH} = V_{DD}$	–	–	10	
Output voltage	V_{OL}	I_O = 1.6 mA	–	–	0.4	V
	V_{OH}	I_O = −400 μA	2.4	–	–	

A.C. Characteristics

(V_{DD} = 5V±5% Ta = 0°C ~ 70°C)

Parameter		Symbol	Condition	Min	Typ	Max	Unit
Maximum clock frequency		f_{cMAX}	V_{IH} = 3.0V V_{IL} = 0V	9	–	–	MHz
Power supply current		I_{DD}	f_c = 9 MHz	–	–	50	mA
Propagation delay time	OUT_X	t_{PHL}	CL = 35 pF V_{IH} = 3.0 V V_{IL} = 0V	–	–	45	nS
	PER			–	–	65	
	OUT_X	t_{PLH}		–	–	45	
	PER			–	–	65	
Data setup time	INX	t_{SET}	V_{IH} = 3.0V V_{IL} = 0V	10	–	–	nS
	$\overline{DG}$			25	–	–	
	$\overline{CLR}$			10	–	–	–
Data hold time	INX	t_{HOLD}		30	–	–	nS
	$\overline{DG}$			20	–	–	
	$\overline{CLR}$			30	–	–	
Output transit time		t_r	CL = 35 pF V_{IH} = 3.0V V_{IL} = 0V	–	–	25	nS
		t_f		–	–	25	
Minimum pulse width of clock		t_{CWL}	V_{IH} = 3.0 V V_{IL} = 0V	38	–	–	nS
		t_{CWH}		38	–	–	

FUNCTION TABLE

Input										Output									
IN_0	IN_1	IN_2	IN_3	IN_4	IN_5	IN_6	IN_7	IN_8	$\overline{DG}$	OUT_0	OUT_1	OUT_2	OUT_3	OUT_4	OUT_5	OUT_6	OUT_7	OUT_8	PER
D_{00}	D_{10}	D_{20}	D_{30}	D_{40}	D_{50}	D_{60}	D_{70}	D_{80}	DG_0	D_{00}	D_{01}	D_{02}	D_{03}	D_{04}	D_{05}	D_{06}	D_{07}	Note 1	Note 2
D_{01}	D_{11}	D_{21}	D_{31}	D_{41}	D_{51}	D_{61}	D_{71}	D_{81}	DG_1	D_{10}	D_{11}	D_{12}	D_{13}	D_{14}	D_{15}	D_{16}	D_{17}		
D_{02}	D_{12}	D_{22}	D_{32}	D_{42}	D_{52}	D_{62}	D_{72}	D_{82}	DG_2	D_{20}	D_{21}	D_{22}	D_{23}	D_{24}	D_{25}	D_{26}	D_{27}		
D_{03}	D_{13}	D_{23}	D_{33}	D_{43}	D_{53}	D_{63}	D_{73}	D_{83}	DG_3	D_{30}	D_{31}	D_{32}	D_{33}	D_{34}	D_{35}	D_{36}	D_{37}		
D_{04}	D_{14}	D_{24}	D_{34}	D_{44}	D_{54}	D_{64}	D_{74}	D_{84}	DG_4	D_{40}	D_{41}	D_{42}	D_{43}	D_{44}	D_{45}	D_{46}	D_{47}		
D_{05}	D_{15}	D_{25}	D_{35}	D_{45}	D_{55}	D_{65}	D_{75}	D_{85}	DG_5	D_{50}	D_{51}	D_{52}	D_{53}	D_{54}	D_{55}	D_{56}	D_{57}		
D_{06}	D_{16}	D_{26}	D_{36}	D_{46}	D_{56}	D_{66}	D_{76}	D_{86}	DG_6	D_{60}	D_{61}	D_{62}	D_{63}	D_{64}	D_{65}	D_{66}	D_{67}		
D_{07}	D_{17}	D_{27}	D_{37}	D_{47}	D_{57}	D_{67}	D_{77}	D_{87}	DG_7	D_{70}	D_{71}	D_{72}	D_{73}	D_{74}	D_{75}	D_{76}	D_{77}		

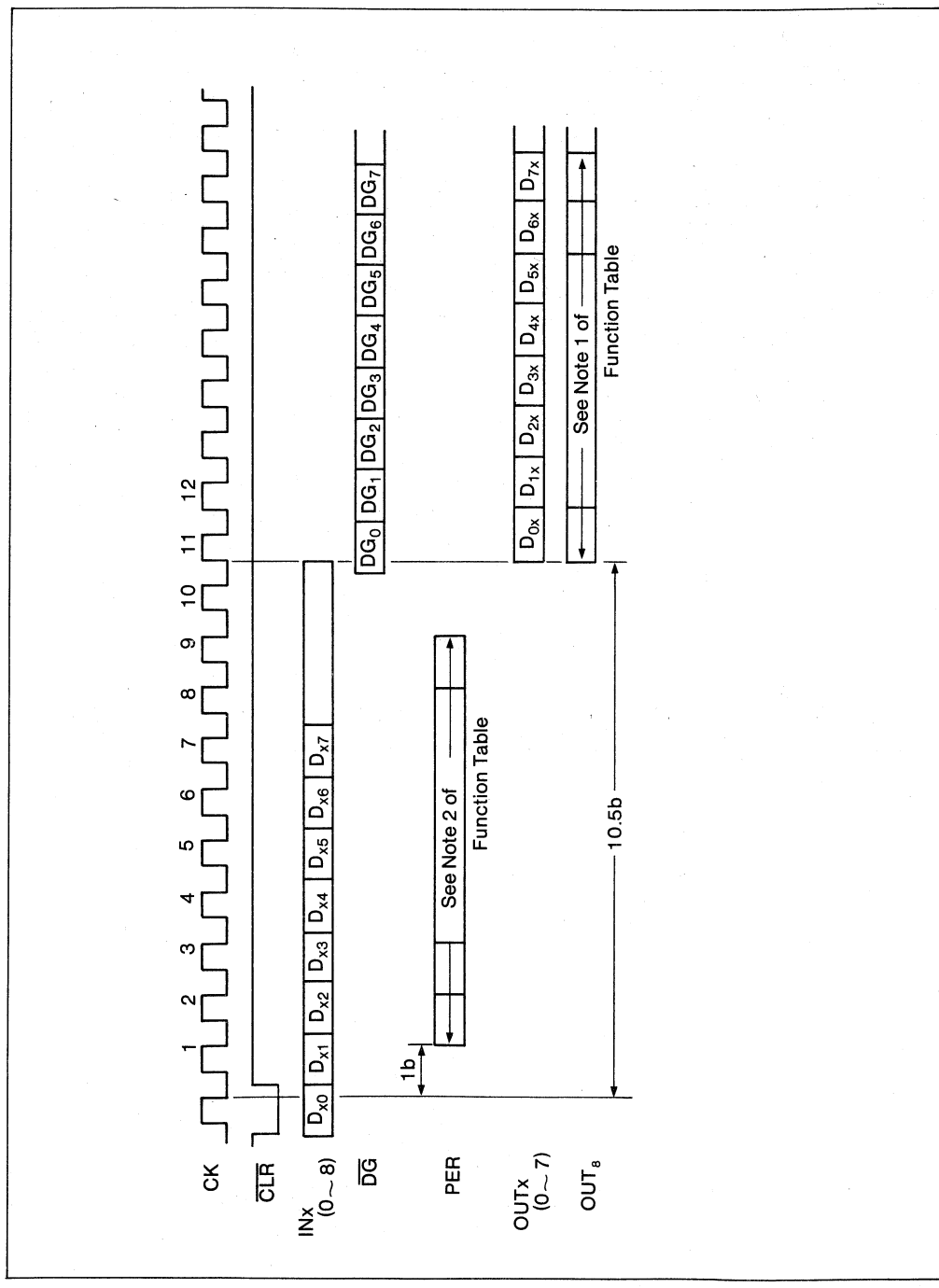
Note 1: The Xth bit of OUT_8 depends on the number of "H"s at the Xth bit of D_{x0} through D_{x7} and the $\overline{DG}$.

The number of "H" at the X bit of $D_{x0} \sim D_{x7}$ & DG	The X bit of OUT_8
0, 2, 4, 6, 8	0
1, 3, 5, 7, 9	1

Note 2: The Xth bit of PER depends on the number of "H"s of D_{0x} through D_{8x}.

The number of "H" of $D_{0x} \sim D_{8x}$ & DG	The X bit of PER
0, 2, 4, 6, 8	1
1, 3, 5, 7, 9	0

Timing Chart



MSM6914

HIGHWAY SWITCH CIRCUIT

GENERAL DESCRIPTION

The MSM6914 is a highway switch circuit LSI which is fabricated by OKI's low power consumption CMOS silicon gate technology.

The MSM6914 has 3 bits, in parallel, of 16 pins for digital data input lines and 4 pins for digital data output lines to be connected with any one of those input lines, forming the digital data switch matrix with 16 input lines × 4 output lines × 3 bits. The selection of output lines is performed by 4 bits of input control signals.

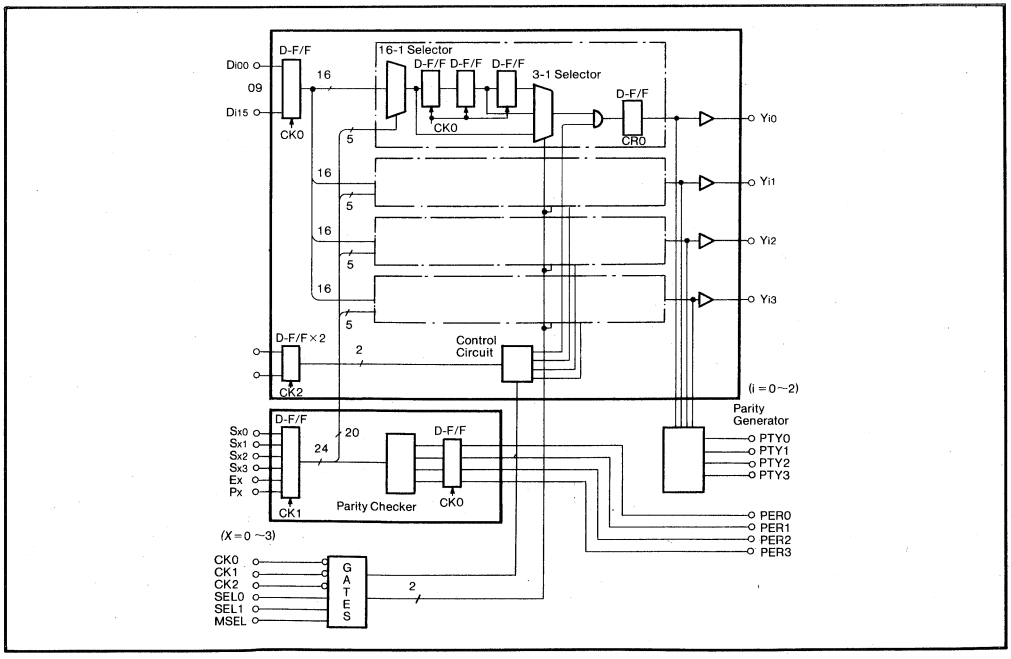
All data perform clock-synchronized operations and the number of delay clocks between input and output can be set to any one of clocks 1, 3, and 4. It also has the function to expand the lattice size of switch matrix. In addition, it has functions to perform the parity check for ouput line control signals and the parity generation for output data and allows the 9-MHz operation.

FEATURES

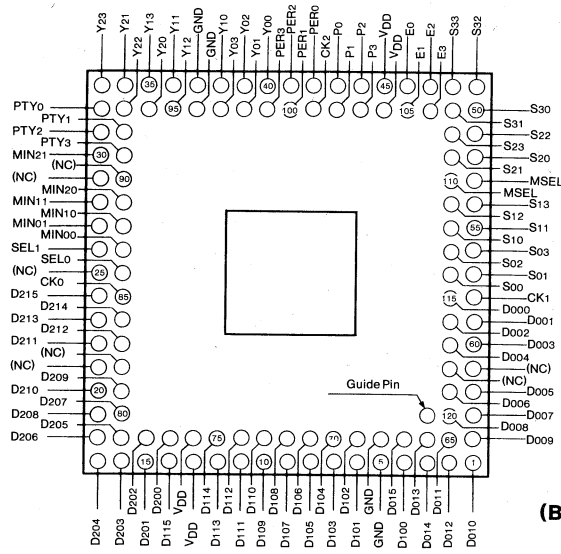
- 16 × 4 × 3 bits switch matrix
- Built-in parity-check circuit for input control signal
- Built-in parity-generation for data output signal
- Built-in multi-input circuit for expanding lattice size
- 5-V single power supply
- 120-pin ceramic PGA package

III

BLOCK DIAGRAM



PIN CONFIGURATION AND CONNECTION



(Bottom View)

Pin No.	Symbol	Pin No.	Symbol	Pin No.	Symbol	Pin No.	Symbol	Pin No.	Symbol	Pin No.	Symbol
1	D_{010}	21	N.C	41	PER_2	61	N.C.	81	D_{209}	101	CK_2
2	D_{012}	22	D_{211}	42	PER_0	62	D_{005}	82	N.C	102	P_1
3	D_{014}	23	D_{213}	43	P_0	63	D_{007}	83	D_{212}	103	P_3
4	D_{100}	24	D_{215}	44	P_2	64	D_{009}	84	D_{214}	104	V_{DD}
5	GND	25	N.C	45	V_{DD}	65	D_{011}	85	CK0	105	E_1
6	D_{101}	26	SEL_1	46	E_0	66	D_{013}	86	SEL_0	106	E_3
7	D_{103}	27	MIN_{01}	47	E_2	67	D_{015}	87	MIN_{00}	107	S_{31}
8	D_{105}	28	MIN_{11}	48	S_{33}	68	GND	88	MIN_{10}	108	S_{23}
9	D_{107}	29	N.C	49	S_{32}	69	D_{102}	89	MIN_{20}	109	S_{21}
10	D_{109}	30	MIN_{21}	50	S_{30}	70	D_{104}	90	N.C	110	MSEL
11	D_{111}	31	PTY_2	51	S_{22}	71	D_{106}	91	PTY_3	111	S_{12}
12	D_{113}	32	PTY_0	52	S_{20}	72	D_{108}	92	PTY_1	112	S_{10}
13	V_{DD}	33	Y_{23}	53	MSEL	73	D_{110}	93	Y_{22}	113	S_{02}
14	D_{115}	34	Y_{21}	54	S_{13}	74	D_{112}	94	Y_{20}	114	S_{00}
15	D_{201}	35	Y_{13}	55	S_{11}	75	D_{114}	95	Y_{12}	115	D_{000}
16	D_{203}	36	Y_{11}	56	S_{03}	76	V_{DD}	96	GND	116	D_{002}
17	D_{204}	37	GND	57	S_{01}	77	D_{200}	97	Y_{03}	117	D_{004}
18	D_{206}	38	Y_{10}	58	CK_1	78	D_{202}	98	Y_{01}	118	N.C
19	D_{208}	39	Y_{02}	59	D_{001}	79	D_{205}	99	PER_3	119	D_{006}
20	D_{210}	40	Y_{00}	60	D_{003}	80	D_{207}	100	PER_1	120	D_{008}

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Condition	Ratings	Unit
Supply voltage	V_{DD}	Ta=25°C, V_{SS}=0 V	−0.3 ~ +7.0	V
Input voltage	$V_{IN\ MAX}$	Ta=25°C	V_{DD} + 0.5	V
	$V_{IN\ MIN}$		V_{SS} − 0.5	
Operation temp.	T_{OP}	———	0 ~ +70	°C
Storage temp.	T_{STR}	———	−65 ~ +150	°C

Recomended Operating Conditions

Parameter	Symbol	Max	Typ	Min	Unit	Remark
Supply voltage	V_{DD}	4.75	5	5.25	V	5 V ± 5%
	V_{SS}	0	0	0		
Operational temp.	T_{OP}	0	–	70	°C	
Clock duty	$D\phi$	–	50	–	%	
Input transit time	t_{INr}	–	10	–	nS	
	$t_{IN\int}$	–	10	–		
Input voltage	V_{IH}	2.2	–	V_{DD}	V	
	V_{IL}	0	–	0.8		

D.C. Characteristics

(V_{DD} = 5V±5% Ta = 0 ~ 70°C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input current	I_{IL}	V_{IL} = 0 V	−10	–	–	μA
	I_{IH}	V_{IH} = V_{DD}	–	–	10	
Output voltage	V_{OL}	I_{OL} = 1.6 mA	–	–	0.4	V
	V_{OH}	I_{OH} = −400 μA	2.4	–	–	

A.C. Characteristics

(V_{DD} = 5V±5% Ta = 0 ~ 70°C)

Parameter		Symbol	Condition	Min	Typ	Max	Unit
Maximum clock frequency		$f_{C\ MAX}$	V_{IH} = 3.0V V_{IL} = 0 V	9	–	–	MHz
Power supply current		I_{DD}	fc = 9 MHz	–	–	130	mA
Propagation delay time	Yxx	t_{PHL}	CL = 35 pF V_{IH} = 3.0 V V_{IH} = 0 V	–	–	55	nS
	PERx			–	–	50	
	PTYx			–	–	85	
	Yxx	t_{PLH}		–	–	55	
	PERx		V_{IH} = 0 V	–	–	50	
	PTYx			–	–	85	
Data setup time	Dxxx	t_{SET}	V_{IH} = 3.0 V V_{IL} = 0 V	10	–	–	nS
	Sx, Ex, Px			10	–	–	
	MINx			10	–	–	
Data hold time	Dxxx	t_{HLD}	V_{IH} = 3.0 V V_{IL} = 0 V	30	–	–	nS
	Sx, Ex, Px			30	–	–	
	MINx			30	–	–	
Output transit time		tr	CL = 35 pF V_{IH} = 3.0 V V_{IL} = 0 V	–	–	25	nS
		t_f		–	–	25	
Clock skew	CK_0 → CK_1	t_{SKW01}		−5	–	tcyc −85	nS
	CK_0 → CK_2	t_{SKW02}		−2	–	tcyc −40	

Notes:
- Yxx: Y00 ~ Y03, Y10 ~ Y13, Y20 ~ Y23
- PERx: PER0 ~ PER3
- PTYx: PTY0 ~ PTY3
- Dxxx: D000 ~ D015, D100 ~ D115, D200 ~ D215
- Sx: S00 ~ S03, S10 ~ S13, S20 ~ S23, S30 ~ S33
- Ex: E0 ~ E3
- Px: P0 ~ P3
- MINx: MIN00 ~ MIN01, MIN10 ~ MIN11, MIN20 ~ MIN21

PIN DESCRIPTION

Pin Name	Function
Dxxx	Input pin of 16-highway (3 bits/1 highway) data After the latch at the CK_0 fall, output is made to any output data Yxx according to the control data.
MINxx	Input pin for multidata when expanding lattice size
Yxx	Output pin of 4-highway (3 bits/1 highway) data
Sxxx	Input pin for path select data of 16 × 4 switch matrix (Capable of performing the 9-MHz operation)
Ex	Input pin of valid and invalid data in path select data
Px	Input pin of parity (odd number side) to be added to Sxx and Ex
PTYx	Parity check (odd number side) output pin for 3 bits/1 highway of Dxxx
PERx	Parity check (odd number side) output pin of Sxx, Ex, and Px
CK_0	Latch clock of input highway data Dxxx
CK_1	Latch clock of Sxx, Ex, and Px
CK_2	Latch clock of MINxx input data
SELx	Time lag setting pin from Dxxx input data to Yxx output data
MSEL	Data to specify which Yxx output data is multiplied by MINxx input data

FUNCTION TABLE (1)

Note 1

Input											Output					Remark
① S03	S02	S01	S00	E0	P0	SEL0	SEL1	MSEL	MIN 00 ~ MIN 20	MIN 01 ~ MIN 21	Y00	Y10	Y20	PER0	PTY0	
② S13	S12	S11	S10	E1	P1						Y01	Y11	Y21	PER1	PTY1	
③ S23	S22	S21	S20	E2	P2						Y02	Y12	Y22	PER2	PTY2	
④ S33	S32	S31	S30	E3	P3						Y03	Y13	Y23	PER3	PTY3	
X	X	X	X	1	X	0	0	X	1	1	1	1	1	Note 2	↑	
0	0	0	0	0	0	0	0	X	1	1	D000	D100	D200	1		
0	0	0	0	0	1	0	0	X	1	1	D000	D100	D200	0		
0	0	0	1	0	0	0	0	X	1	1	D001	D101	D201	0		
0	0	0	1	0	1	0	0	X	1	1	D001	D101	D201	1		
0	0	1	0	0	0	0	0	X	1	1	D002	D102	D202	0		
0	0	1	0	0	1	0	0	X	1	1	D002	D102	D202	1		
0	0	1	1	0	0	0	0	X	1	1	D003	D103	D203	1		
0	0	1	1	0	1	0	0	X	1	1	D003	D103	D203	0		
0	1	0	0	0	0	0	0	X	1	1	D004	D104	D204	0		
0	1	0	0	0	1	0	0	X	1	1	D004	D104	D204	1		
0	1	0	1	0	0	0	0	X	1	1	D005	D105	D205	1		
0	1	0	1	0	1	0	0	X	1	1	D005	D105	D205	0		
0	1	1	0	0	0	0	0	X	1	1	D006	D106	D206	1		1-clock delay inside of LSI
0	1	1	0	0	1	0	0	X	1	1	D006	D106	D206	0		
0	1	1	1	0	0	0	0	X	1	1	D007	D107	D207	0		
0	1	1	1	0	1	0	0	X	1	1	D007	D107	D207	1		
1	0	0	0	0	0	0	0	X	1	1	D008	D108	D208	0		
1	0	0	0	0	1	0	0	X	1	1	D008	D108	D208	1		
1	0	0	1	0	0	0	0	X	1	1	D009	D109	D209	1		
1	0	0	1	0	1	0	0	X	1	1	D009	D109	D209	0	Note 3	
1	0	1	0	0	0	0	0	X	1	1	D010	D110	D210	1		
1	0	1	0	0	1	0	0	X	1	1	D010	D110	D210	0		
1	0	1	1	0	0	0	0	X	1	1	D011	D111	D211	0		
1	0	1	1	0	1	0	0	X	1	1	D011	D111	D211	1		
1	1	0	0	0	0	0	0	X	1	1	D012	D112	D212	1		
1	1	0	0	0	1	0	0	X	1	1	D012	D112	D212	0		
1	1	0	1	0	0	0	0	X	1	1	D013	D113	D213	0		
1	1	0	1	0	1	0	0	X	1	1	D013	D113	D213	1		

III

Input											Output					Remark
S_{03}	S_{02}	S_{01}	S_{00}	E_0	P_0	SEL0	SEL1	MSEL	MIN 00 ⌇ MIN 20	MIN 01 ⌇ MIN 21	Y_{00}	Y_{10}	Y_{20}	PER_0	PTY_0	
S_{13}	S_{12}	S_{11}	S_{10}	E_1	P_1						Y_{01}	Y_{11}	Y_{21}	PER_1	PTY_1	
S_{23}	S_{22}	S_{21}	S_{20}	E_2	P_2						Y_{02}	Y_{12}	Y_{22}	PER_2	PTY_2	
S_{33}	S_{32}	S_{31}	S_{30}	E_3	P_3						Y_{03}	Y_{13}	Y_{23}	PER_3	PTY_3	
1	1	1	0	0	0	0	0	X	1	1	D_{014}	D_{114}	D_{214}	0		1-clock delay inside of LSI
1	1	1	0	0	1	0	0	X	1	1	D_{014}	D_{114}	D_{214}	1		
1	1	1	1	0	0	0	0	X	1	1	D_{015}	D_{115}	D_{215}	1	Note 3	
1	1	1	1	0	1	0	0	X	1	1	D_{015}	D_{115}	D_{215}	0		
X	X	X	X	1	X	1	0	X	1	1	1	1	1	Note 2		3-clock delay inside of LSI
0	0	0	0	0	0	1	0	X	1	1	D_{000}	D_{100}	D_{200}	1		
0	0	0	0	0	1	1	0	X	1	1	D_{000}	D_{100}	D_{200}	0		
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮		
1	1	1	1	0	0	1	0	X	1	1	D_{015}	D_{115}	D_{215}	1		
1	1	1	1	0	1	1	0	X	1	1	D_{015}	D_{115}	D_{215}	0		
X	X	X	X	1	X	0	1	X	1	1	1	1	1	Note 2		4-clock delay inside of LSI
0	0	0	0	0	0	0	1	X	1	1	D_{000}	D_{100}	D_{200}	1		
0	0	0	0	0	1	0	1	X	1	1	D_{000}	D_{100}	D_{200}	0		
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮		
1	1	1	1	0	0	0	1	X	1	1	D_{015}	D_{115}	D_{215}	1		
1	1	1	1	0	1	0	1	X	1	1	D_{015}	D_{115}	D_{215}	0		

X: don't care Irrespective of 1/0 condition

Note 1: Function Table (1) shows the case of selection of these input pins.
Note 2: Numbers of "1" on $S_{x0} \sim S_{x3}$, Ex and Fx determines PERx

The number of "1"s $S_{x0} \sim S_{x3}$, Ex and Fx	PERx
0, 2, 4, 6	"1"
1, 3, 5	"0"

Note 3: Numbers of "1" on D_{0xx}, D_{1xx} and D_{2xx} determines PTY

The number of "1" on D_{0xx}, D_{1xx} and D_{2xx}	PERx
0, 2	"0"
1, 3	"1"

FUNCTION TABLE (2)

Input									Output						Remark
S_{00} ~ S_{03}	S_{10} ~ S_{13}	S_{20} ~ S_{23}	S_{30} ~ S_{33}	E_0 ~ E_3	P_0 ~ P_3	SEL0	SEL1	MSEL	MIN00 / MIN10 / MIN20	MIN01 / MIN11 / MIN21	Y00 / Y10 / Y20	Y01 / Y11 / Y21	Y02 / Y12 / Y22	Y03 / Y13 / Y23	PTY0 ~ PTY3	
X	X	X	X	1	X	X	X	X	1	1	1	1	1	1	1	
X	X	X	X	1	X	X	X	0	0	1	0	1	1	1	↑	
X	X	X	X	1	X	X	X	0	1	0	1	0	1	1	↑	
X	X	X	X	1	X	X	X	0	0	0	0	0	1	1	Note 4	
X	X	X	X	1	X	X	X	1	0	1	1	1	0	1	↓	
X	X	X	X	1	X	X	X	1	1	0	1	1	1	0	↓	
X	X	X	X	1	X	X	X	1	0	0	1	1	0	0	↓	

X: Irrespective of 1/0 condition

Note 4: These are determined as follows.

1) In case of MSEL = "0".
PTY0 is determined by the numbers of "1" on MIN00 ~ MIN20, while PTY1 is determined by the numbers of "1" on MIN01 ~ MIN21.
PTY2 and PTY3 are constantly "1".

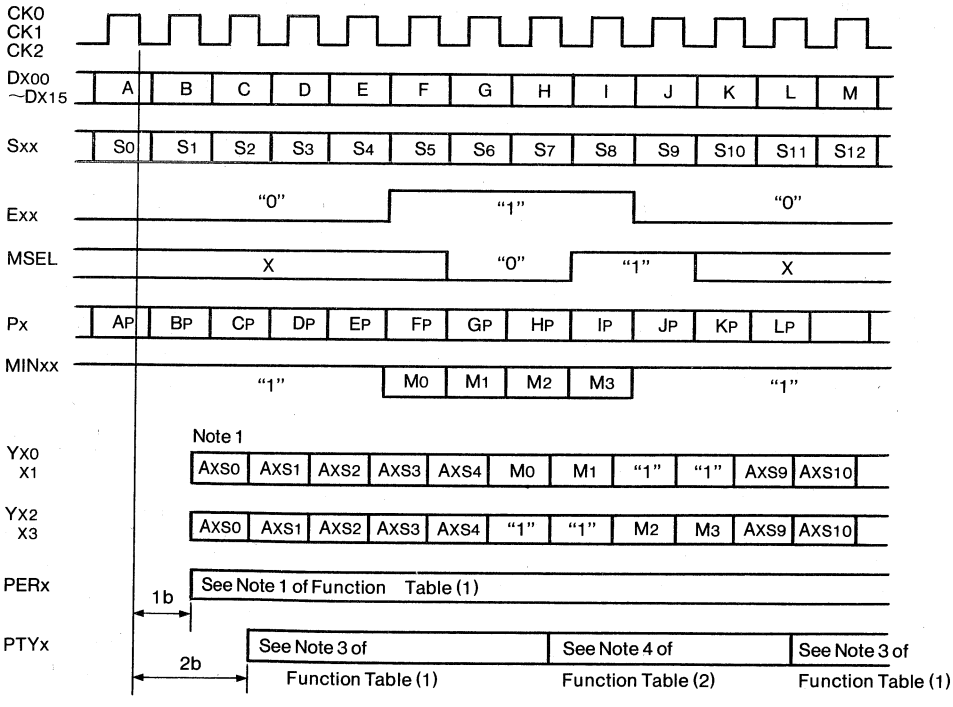
Numbers on "1" of MIN00 ~ MIN21	PTY0
0, 2	"0"
1, 3	"1"

Numbers on "1" of MIN01 ~ MIN21	PTY1
0, 2	"0"
1, 3	"1"

2) In case of MSEL = "1".
PTY0 and PTY1 are constantly "1".
PTY2 is determined by the numbers of "1" on MIN00 ~ MIN20, while PTY3 is determined by the numbers of "1" on MIN01 ~ MIN21.

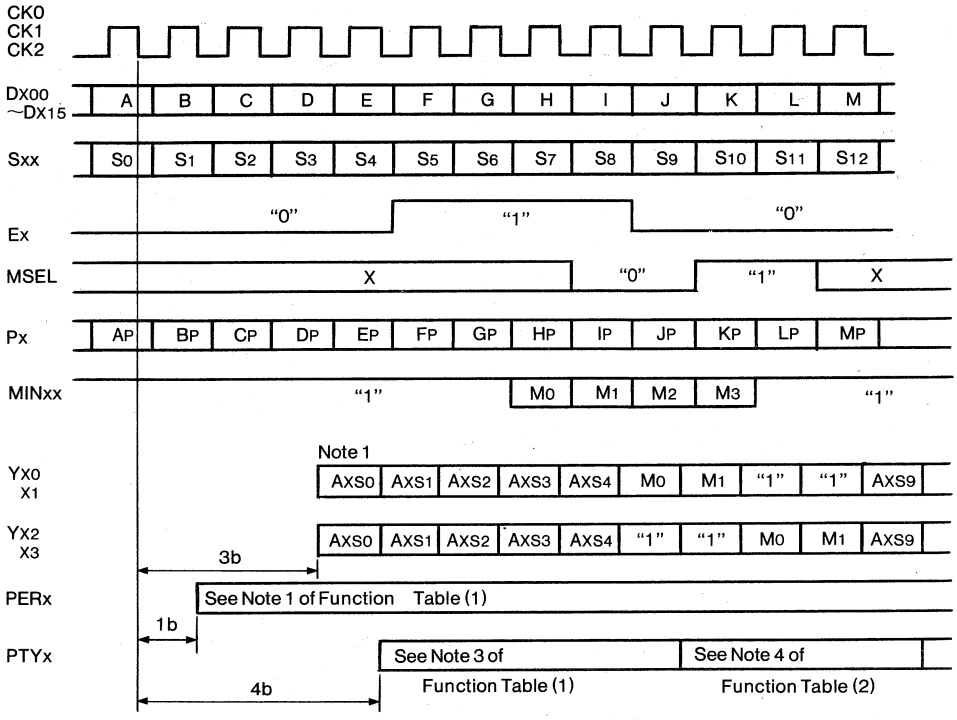
TIMING CHART

(1) In case of SEL0 = "1" and SEL1 = "1"



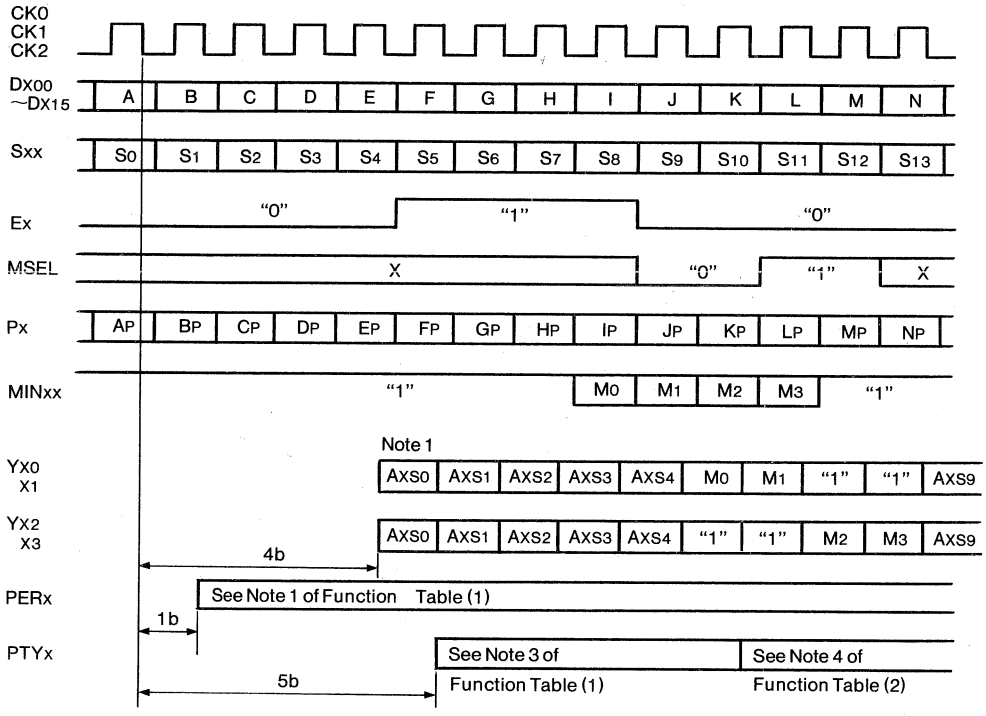
Note 1: Axsn is the value when Dxxx is selected at Sxx=Sn.

(2) In case of SEL0 = "1" and SEL_1 = "0"

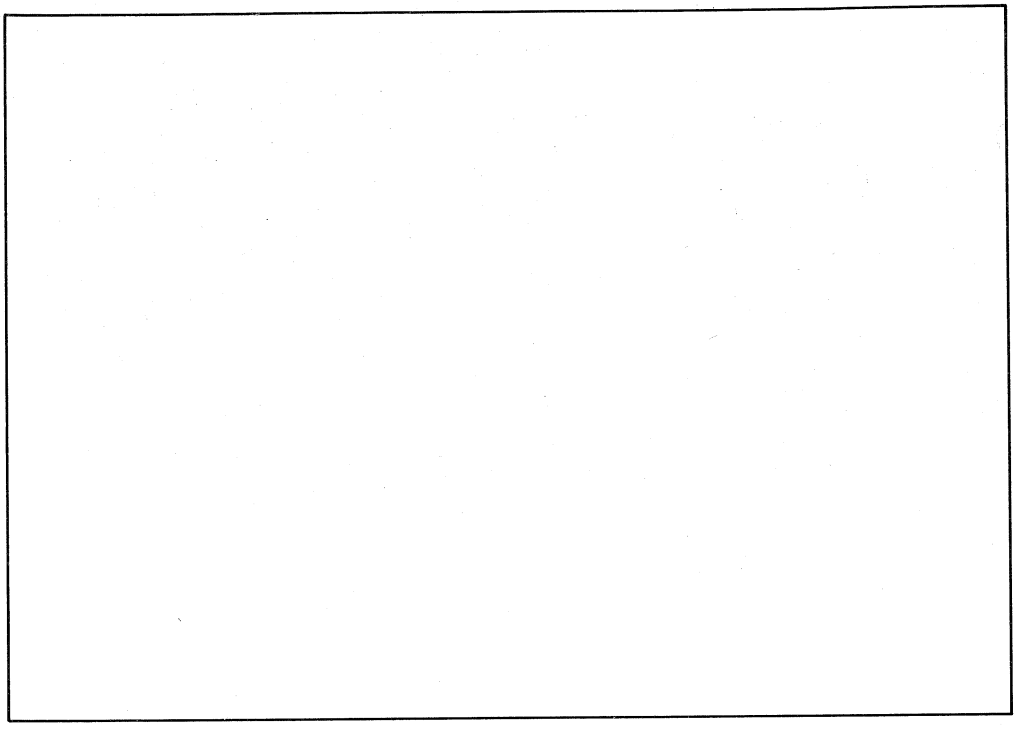


Note 1: Axsn is the value when Dxxx is selected at Sxx=Sn.

(3) In case of SEL0 = "0" and SEL_1 = "1"

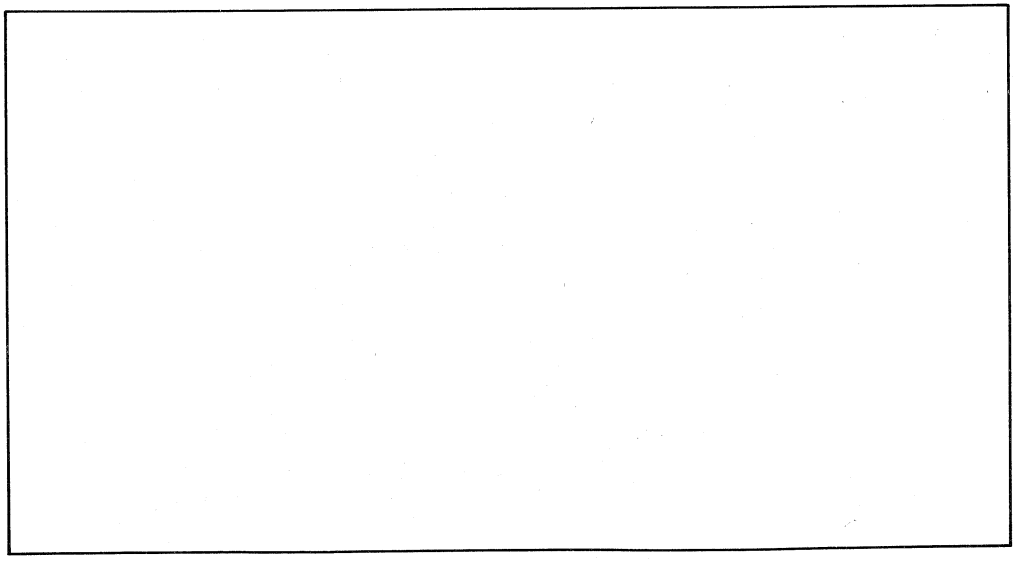


Note 1: Axsn is the value when Dxxx is selected at Sxx=Sn.



E. DIGITAL SIGNAL PROCESSOR

III



MSM77C20

DIGITAL SIGNAL PROCESSOR

GENERAL DESCRIPTION

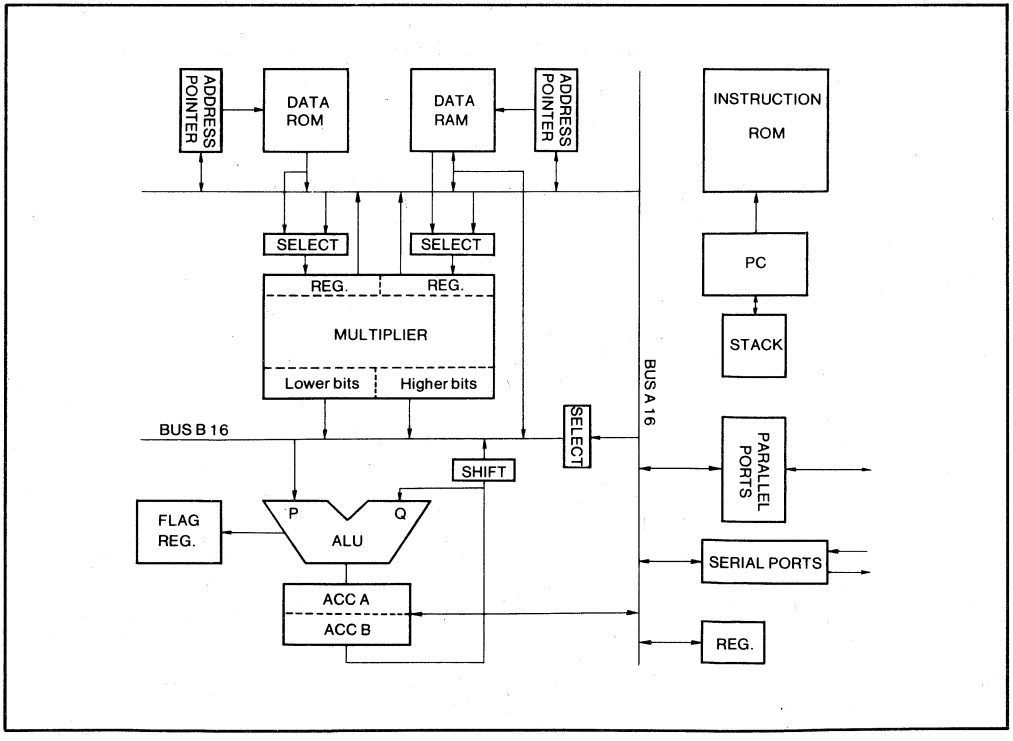
The MSM77C20 is an LSI designed for the purpose of digital signal processing in the field of speech processing and telecommunications.

Since this LSI is the one-chip microcomputer contained the ROM, RAM, ALU, and multiplier, it is applicable to different systems by re-writing contents of the program MASK ROM.

FEATURES

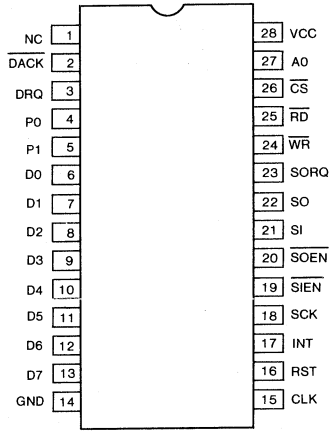
- Instruction cycle : 250 ns
- Instruction ROM : 512 words × 23 bits
- Data ROM : 512 words × 13 bits
- Data RAM : 128 words × 16 bits
- Multiplier : 16 bits × 16 bits = 31 bits
- Input/Output
  Parallel Port
  Serial Ports
  DMA transfer
- CPU interface 8080 series
- 5 V single power supply
- 3-micron CMOS
- 28-pin ceramic DIP
- 28-pin plastic DIP

FUNCTIONAL BLOCK DIAGRAM



III

PIN CONFIGURATION



(Top View)

PIN DESCRIPTION

Symbol	Description	Type	Function
D0 ~ D7	Data bus	I/O	Bi-directional port used to transfer data between the DR or SR register and the external data bus.
$\overline{RD}$	Read	I	Control signal to read out the data stored in the DR or SR register. When this signal and the $\overline{CS}$ or $\overline{DACK}$ signal become active-low, the D0 to D7 are put into the output state.
$\overline{WR}$	Write	I	Control signal to write external data into the DR register. When this signal and the $\overline{CS}$ or $\overline{DACK}$ signal become active-low, the D0 to D7 are put into the input/output enable state.
$\overline{CS}$	Chip select	I	Used along with the $\overline{RD}$ or $\overline{WR}$ signal. When this signal becomes active-low, the D0 to D7 are put into the input/output enable state.
A0	DR/SR register select signal	I	Signal to select the DR or SR register when reading out the data. When this signal is set to "1" and the SR register to "0", the DR register is selected.
RST	Reset	I	When this signal is set to "1" (at least 4 clocks should be input), the internal program counter, etc. are initialized.
$\overline{DACK}$	DMA acknowledge	I	Control signal to transfer data between the DR register and external units in the DMA mode, and input the signal indicating that the DMA cycle is permitted.
DRQ	DMA request	O	Signal to request the DMA transfer to external units when data is transferred in the DMA mode.
P0, P1	Ports 0 and 1	O	General-purpose port output assigned to the SR register.

PIN DESCRIPTION (CONT.)

Symbol	Description	Type	Function
INT	Interrupt	I	When this signal is changed from "0" to "1" (at least 8 clocks should be input) during the interruptible state (specified by the SR register), the program jumps to the interrupt address and the interrupt processing is executed.
SI	Serial input	I	The serial data is input by being synchronized with the SCK clock rising edge.
$\overline{\text{SIEN}}$	Serial input enable	I	Signal to control whether or not to input the serial data. When this signal is set to "1", the serial data is not stored.
SO	Serial output	Tri-state	The serial data is output by being synchronized with the SCK clock falling edge.
$\overline{\text{SOEN}}$	Serial output enable	I	Signal to control whether or not to output the serial data. When this signal is set to "1", the SO is put into the high-impedance state.
SORQ	Serial output request	O	When data is set to the serial output register (SO register), this signal is put into "1". When data with the specified number of bits (specified by the SR register) is output, this signal is put into "0".
SCK	Serial clock	I	Clock to synchronize the serial data. The serial data is input or output by being synchronized with this clock.
CLK	Clock	I	Clock to operate this chip.

INSTRUCTION

INSTRUCTION FORMAT

Instruction	Instruction Register 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
OP (Operation and Move)	00 | PSEL | ALU | ASEL | DPL | DPH.M | RPDEC | SRC | DST
RET (Return)	01 | PSEL | ALU | ASEL | DPL | DPH.M | RPDEC | SRC | DST
JUMP (Jump)	10 | BRANCH | JMPA
LDI (Immediate Data Load)	11 | ID | DST

INSTRUCTION FIELD

- **ALU P-Port Selection Field (OP, RET)**

Mnemonic	PSEL		Description
	I 20	I 19	
RAM	0	0	RAM
IDB	0	1	Internal data bus (*1)
M	1	0	M register
N	1	1	N register

*1 Indicates the contents of registers specified in SRC field.

Note: These fields are effective only when ALU instructions are OR, AND, XOR, SUB, ADD, SBB, and ADC.

- **ALU Operation Field (OP, RET)**

Mnemonic	ALU				Description
	I 18	I 17	I 16	I 15	
NOP	0	0	0	0	No operation
OR	0	0	0	1	(ACC) V (P) → (ACC)
AND	0	0	1	0	(ACC) Λ (P) → (ACC)
XOR	0	0	1	1	(ACC) $\forall$ (P) → (ACC)
SUB	0	1	0	0	(ACC) − (P) → (ACC)
ADD	0	1	0	1	(ACC) + (P) → (ACC)
SBB	0	1	1	0	(ACC) − (P) − (C) → (ACC)
ADC	0	1	1	1	(ACC) + (P) + (C) → (ACC)
DEC	1	0	0	0	(ACC) − 1 → (ACC)
INC	1	0	0	1	(ACC) + 1 → (ACC)
CMP	1	0	1	0	$(\overline{ACC})$ → (ACC)
SHR1	1	0	1	1	
SHL1	1	1	0	0	
SHL2	1	1	0	1	
SHL4	1	1	1	0	
XCHG	1	1	1	1	

Note: P : ALU P-port input selected by PSEL fields
C : Carry flag of FLAG register that is not selected by ASEL bit.
V : OR.
Λ : AND
$\forall$: Exclusive OR

- **Accumulator Selection Field (OP, RET)**

Mnemonic	ASEL	Description
	I 14	
ACCA	0	Accumulator A
ACCB	1	Accumulator B

- **DP Operation and Modify Field (OP, RET)**

Mnemonic	DPL		Description
	I 13	I 12	
DPNOP	0	0	No operation
DPINC	0	1	Increment DP_L
DPDEC	1	0	Decrement DP_L
DPCLR	1	1	Clear DP_L

Mnemonic	DPH.M			Description
	I 11	I 10	I 9	
M0	0	0	0	(DP6 DP5 DP4) ∀ (0 0 0)
M1	0	0	1	(DP6 DP5 DP4) ∀ (0 0 1)
M2	0	1	0	(DP6 DP5 DP4) ∀ (0 1 0)
M3	0	1	1	(DP6 DP5 DP4) ∀ (0 1 1)
M4	1	0	0	(DP6 DP5 DP4) ∀ (1 0 0)
M5	1	0	1	(DP6 DP5 DP4) ∀ (1 0 1)
M6	1	1	0	(DP6 DP5 DP4) ∀ (1 1 0)
M7	1	1	1	(DP6 DP5 DP4) ∀ (1 1 1)

- **RP Decrement Field (OP, RET)**

Mnemonic	RPDEC	Description
	I 8	
RPNOP	0	No operation
RPDEC	1	Decrement RP

- **Source Register Field (OP, RET)**

Mnemonic	SRC				Description
	I 7	I 6	I 5	I 4	
NON	0	0	0	0	No register
A	0	0	0	1	Accumulator A
B	0	0	1	0	Accumulator B
TR	0	0	1	1	TR register
DP	0	1	0	0	DP register
RP	0	1	0	1	RP register
RO	0	1	1	0	RO register
SGN	0	1	1	1	SGN register
DR	1	0	0	0	DR register
DRNF	1	0	0	1	DR register (*1)
SR	1	0	1	0	SR register
SIM	1	0	1	1	SI register (1st → MSB) (*2)
SIL	1	1	0	0	SI register (1st → MSB) (*3)
K	1	1	0	1	K register
L	1	1	1	0	L register
MEM	1	1	1	1	RAM

*1 The contents of DR register are output to the internal bus, however in the case of NON DMA mode, RQM flag is not set, and in the case of DMA mode, DRQ flag is not set.

*2 The first bit of serial data (ex. 16 bit data) is output to the bit "15" of the internal bus, and the last bit to the bit "0".

*3 The first bit of serial data (ex. 16 bit data) is output to the bit "0" of the internal bus, and the last bit to the bit "15".

- **Destination Register Field (OP, RET, LDI)**

Mnemonic	DST				Description
	I 3	I 2	I 1	I 0	
@NON	0	0	0	0	No register
@A	0	0	0	1	Accumulator A
@B	0	0	1	0	Accumulator B
@TR	0	0	1	1	TR register
@DP	0	1	0	0	DP register
@RP	0	1	0	1	RP register
@DR	0	1	1	0	DR register
@SR	0	1	1	1	SR register
@SOL	1	0	0	0	SO register
@SOM	1	0	0	1	SO register (LSB → 1st) (*1)
@K	1	0	1	0	K register
@KLR	1	0	1	1	KLR (*3)
@KLM	1	0	1	0	KLM (*4)
@L	1	1	0	1	L register
@NON	1	1	1	0	No register
@MEM	1	1	1	1	RAM

*1 The serial data is output successively starting from the bit "0" of internal bus.

*2 The serial data is output successively starting from the bit "15" of internal bus.

*3 The data on internal data bus is set to K register, and the output of RO register to L register.

*4 The contents in the RAM address, specified by DP6=1 that is (1, DP_5, DP_4, DP_3, DP_2, DP_1, DP_0), set to K register, and the data on internal data bus to L register.

• BRANCH Field (JUMP)

Mnemonic	BRANCH								Description
	I 20	I 19	I 18	I 17	I 16	I 15	I 14	I 13	
JMP	1	0	0	0	0	0	0	0	Unconditional
CALL	1	0	1	0	0	0	0	0	Unconditional
JNCA	0	1	0	0	0	0	0	0	CA=0
JCA	0	1	0	0	0	0	0	1	CA=1
JNCB	0	1	0	0	0	0	1	0	CB=0
JCB	0	1	0	0	0	0	1	1	CB=1
JNZA	0	1	0	0	0	1	0	0	ZA=0
JZA	0	1	0	0	0	1	0	1	ZA=1
JNZB	0	1	0	0	0	1	1	0	ZB=0
JZB	0	1	0	0	0	1	1	1	ZB=1
JNOVA0	0	1	0	0	1	0	0	0	OVA0=0
JOVA0	0	1	0	0	1	0	0	1	OVA0=1
JNOVB0	0	1	0	0	1	0	1	0	OVB0=0
JOVB0	0	1	0	0	1	0	1	1	OVB0=1
JNOVA1	0	1	0	0	1	1	0	0	OVA1=0
JOVA1	0	1	0	0	1	1	0	1	OVA1=1
JNOVB1	0	1	0	0	1	1	1	0	OVB1=0
JOVB1	0	1	0	0	1	1	1	1	OVB1=1
JNSA0	0	1	0	1	0	0	0	0	SA0=0
JSA0	0	1	0	1	0	0	0	1	SA0=1
JNSB0	0	1	0	1	0	0	1	0	SB0=0
JSB0	0	1	0	1	0	0	1	1	SB0=1
JNSA1	0	1	0	1	0	1	0	0	SA1=0
JSA1	0	1	0	1	0	1	0	1	SA1=1
JNSB1	0	1	0	1	0	1	1	0	SB1=0
JSB1	0	1	0	1	0	1	1	1	SB1=1
JDPL0	0	1	0	1	1	0	0	0	DP_L=0
JDPLF	0	1	0	1	1	0	0	1	DP_L=F (HEX)
JNSIAK	0	1	0	1	1	0	1	0	SI ACK=0

Mnemonic	BRANCH								Description
	I 20	I 19	I 18	I 17	I 16	I 15	I 14	I 13	
JSIAK	0	1	0	1	1	0	1	1	SI ACK=1
JNSOAK	0	1	0	1	1	1	0	0	SO ACK=0
JSOAK	0	1	0	1	1	1	0	1	SO ACK=1
JNRQM	0	1	0	1	1	1	1	0	RQM=0
JRQM	0	1	0	1	1	1	1	1	RQM=1

Note: The values of BRANCH field except the ones listed in the Table shall be unusable.

- **JMPA Field (JUMP)**

JMPA field									Jump address
I 12	I 11	I 10	I 9	I 8	I 7	I 6	I 5	I 4	
0	0	0	0	0	0	0	0	0	"0" address is specified as the jump address.
0	0	0	0	0	0	0	0	1	"1" address is specified as the jump address.
0	0	0	0	0	0	0	1	0	"2" address is specified as the jump address.
				≀					≀
1	1	1	1	1	1	1	1	1	"511" address is specified as the jump address.

- **ID Field (LDI)**

ID field																HEX
I 20	I 19	I 18	I 17	I 16	I 15	I 14	I 13	I 12	I 11	I 10	I 9	I 8	I 7	I 6	I 5	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0001
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0002
								≀								≀
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFF

III

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Limits	Unit
Supply Voltage	Vcc	GND Basis	−0.5 ~ +7.0	V
Input Voltage	V_{IN}		−0.5 ~ Vcc+0.5	V
Output Voltage	V_{OUT}		−0.5 ~ Vcc+0.5	V
Storage Temperature	Tstg		−65 ~ +150	°C
Power Dissipation	Pd	Ta=25°C	1.0	W

OPERATING RANGE

Parameter	Symbol	Min	Typ	Max	Unit	Remark
Supply Voltage	Vcc	4.75	5	5.25	V	
Operating Temperature	Top	−10	25	70	°C	
High Input Voltage	V_{IH}	2.2	–	Vcc+0.3	V	
		3.5	–	Vcc+0.3		CLK
Low Input Voltage	V_{IL}	−0.3	–	0.80	V	
		−0.3	–	0.45		CLK

III

DC CHARACTERISTICS

(V_{CC} = 5V ±5%, Ta = −10 ~ 70°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Low Output Voltage	V_{OL}	I_{OL}=2 mA	–	–	0.45	V
High Output Voltage	V_{OH}	I_{OH}=−400μA	2.4	–	–	V
Input Leak Current	I_{LI}	$0 \leqq V_{IN} \leqq Vcc$	−10	–	10	μA
Output Leak Current	I_{LO}	$0 \leqq V_{OUT} \leqq Vcc$	−10	–	10	μA
CLK, SCK Capacitance	Cϕ	fc=1 MHz	–	–	20	pF
Input Capacitance	C_{IN}		–	–	10	pF
Output Capacitance	C_{OUT}		–	–	20	pF
Current Consumption	Icc	Tcyc=122 nS	–	24	40	mA

AC CHARACTERISTICS

(Vcc = 5V ±5%, Ta = −10 ~ 70°C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
CLK cycle time	ϕCY		122	–	2000	ns
CLK pulse width	ϕD		60	–	–	ns
CLK rise time	ϕr	Voltage at timing measurement point = 1.0V & 3.0V		–	10	ns
CLK fall time	ϕf		–	–	10	ns
A0, $\overline{CS}$, and $\overline{DACK}$ setup to $\overline{RD}\downarrow$	t_{AR}		0	–	–	ns
A0, $\overline{CS}$ and $\overline{DACK}$ hold after $\overline{RD}\uparrow$	t_{RA}		0	–	–	ns
$\overline{RD}$ pulse width	t_{RR}		250	–	–	ns
Data access from $\overline{RD}\downarrow$	t_{RD}	C_L = 100 pF	–	–	150	ns
Data bus float after $\overline{RD}\uparrow$	t_{DF}	C_L = 100 pF	10	–	100	ns
A0, $\overline{CS}$, and $\overline{DACK}$ setup to $\overline{WR}\downarrow$	t_{AW}		0	–	–	ns
A0, $\overline{CS}$, and $\overline{DACK}$ hold after $\overline{WR}\uparrow$	t_{WA}		0	–	–	ns
$\overline{WR}$ pulse width	t_{WW}		250	–	–	ns
Data setup to $\overline{WR}\uparrow$	t_{DW}		150	–	–	ns
Data hold after $\overline{WR}\downarrow$	t_{WD}		0	–	–	ns
$\overline{RD}$ and $\overline{WR}$ recovery time between controls	t_{RV}		250	–	–	ns
DRQ output delay	t_{AM}	C_L = 100 pF	–	–	150	ns
$\overline{DACK}$ input delay	t_{DACK}		1	–	–	ϕD
$\overline{DACK}$ pulse width	t_{DD}	16 bit transfer	250	–	50000	ns
SCK cycle time	t_{SCY}		480	–	DC	ns
SCK pulse width	t_{SCK}		230	–	–	ns
SCK rise time	t_{rSC}		–	–	20	ns
SCK fall time	t_{fSC}		–	–	20	ns
SORQ output delay	t_{DRQ}	C_L = 100 pF	30	–	150	ns
$\overline{SOEN}$ setup to SCK$\downarrow$	t_{SOC}		50	–	–	ns
$\overline{SOEN}$ hold after SCK$\downarrow$	t_{CSO}		30	–	–	ns
SO output delay	t_{DCK}		–	–	150	ns
SO active after SCK$\uparrow$ (controlled by SORQ)	t_{DZRQ}		20	–	300	ns
SO active after SCK$\uparrow$	t_{DZSC}		20	–	300	ns

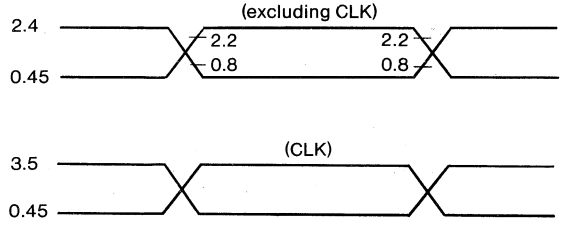
Parameter	Symbol	Condition	Min	Typ	Max	Unit
SO active after SOEN↓	t_{DZE}		20	–	180	ns
SO float after SOEN↑	t_{HZE}		20	–	200	ns
SO float after SCK↑	t_{HZSC}		20	–	300	ns
SO float after SCK↑ (controlled by SORQ)	t_{HZRQ}		70	–	300	ns
SIEN and SI setup to SCK↑	t_{DC}		55	–	–	ns
SIEN and SI hold after SCK↑	t_{CD}		30	–	–	ns
Port output delay	t_{DP}		–	–	ϕCY+ 150	ns
RST pulse width	t_{RST}		4	–	–	ϕCY
INT pulse width	t_{INT}		8	–	–	ϕCY

Note 1: Voltage at AC timing measurement point

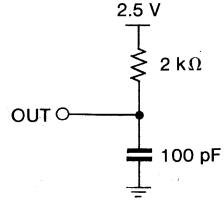
$V_{IL} = V_{OL} = 0.8$ V

$V_{IH} = V_{OH} = 2.2$ V

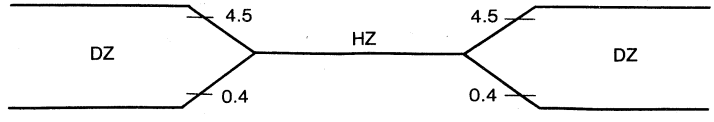
Note 2: AC test input waveform



Note 3: Output HZ and DZ test load circuit

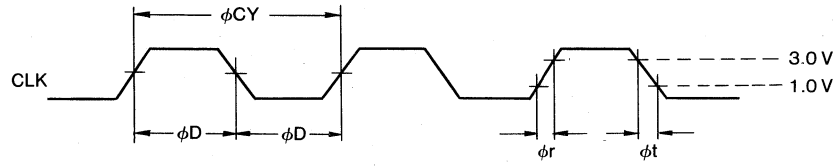


Note 4: Voltages at HZ and DZ timing measurement points

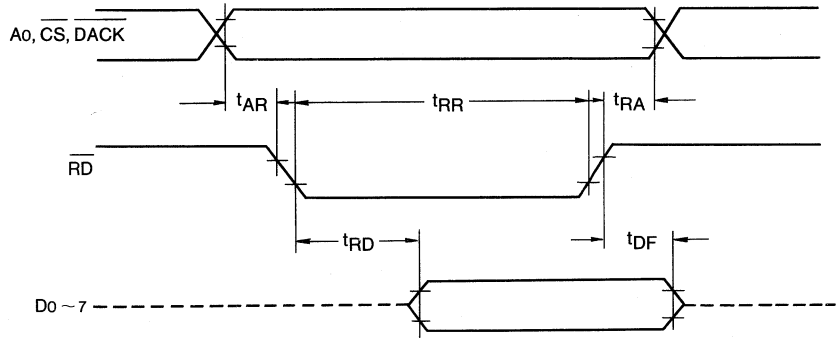


TIMING DIAGRAM

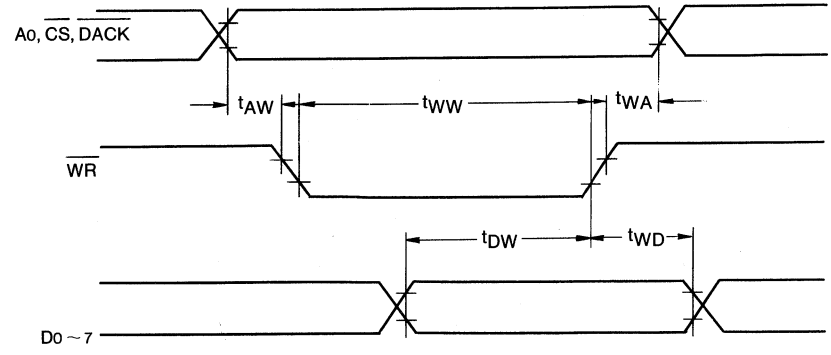
CLOCK



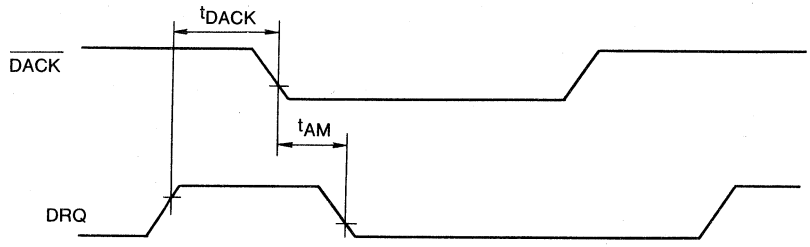
READ OPERATION



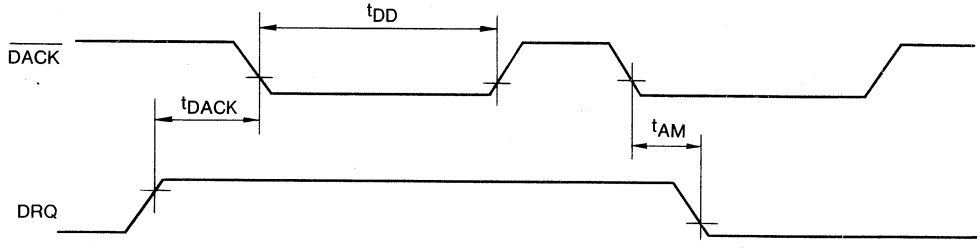
WRITE OPERATION



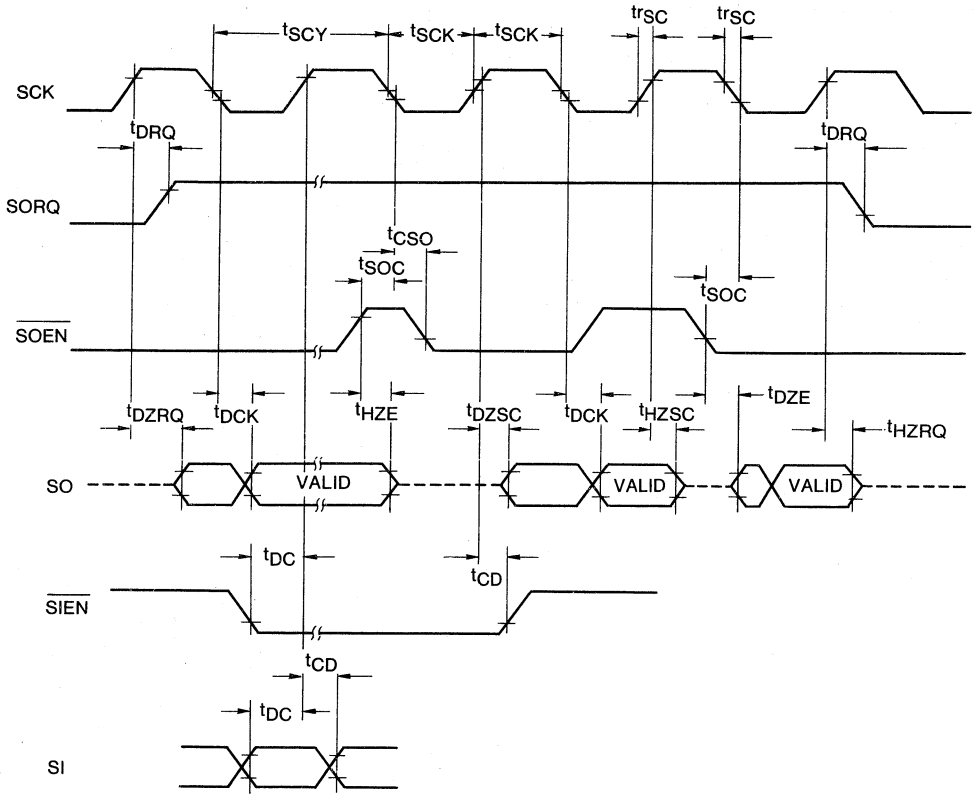
DMA OPERATION
(8 bit Transfer Mode)



(16 bit Transfer Mode)

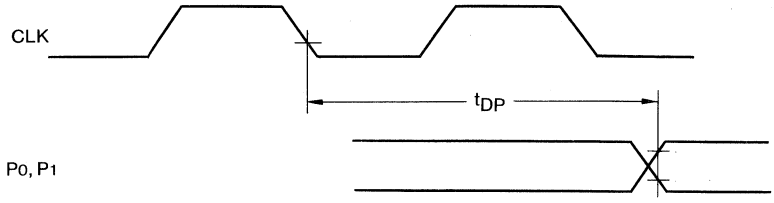


SERIAL INPUT/OUTPUT TIMING

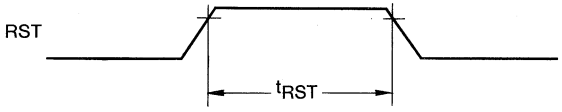


III

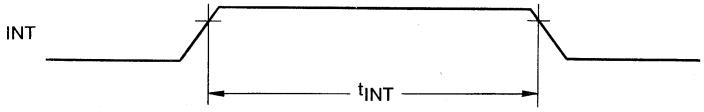
PORT OUTPUT TIMING



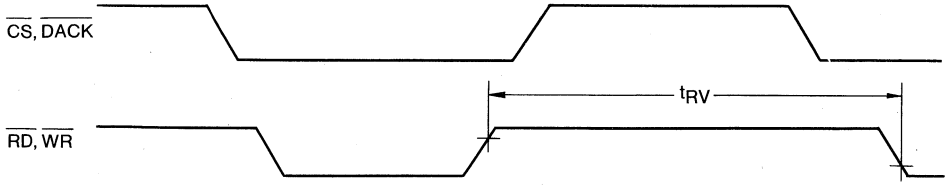
RESET



INTERRUPT



READ/WRITE CYCLE TIMING



MSM6992

HIGH PERFORMANCE DIGITAL SIGNAL PROCESSOR

GENERAL DESCRIPTION

The MSM6992 is a very high performance general purpose 22-bit floating-point digital signal processor (DSP). The MSM6992 is fabricated by using OKI's low power consumption CMOS silicon gate technology.

The MSM6992 is capable of high-speed execution of floating-point arithmetic operations (16-bit mantissa and 6-bit exponent part) and 16-bit fixed-point arithmetic operations. Devices will be available with 125nS & 100nS machine cycle time.

The MSM6992 incorporates a 1K-word × 32-bit programmable ROM and two 128-word × 22 bit data RAMs that can alos be used as a single page of 256 words.

The program and data memories can both be expanded externally up to 64K words via dedicated data and address lines.

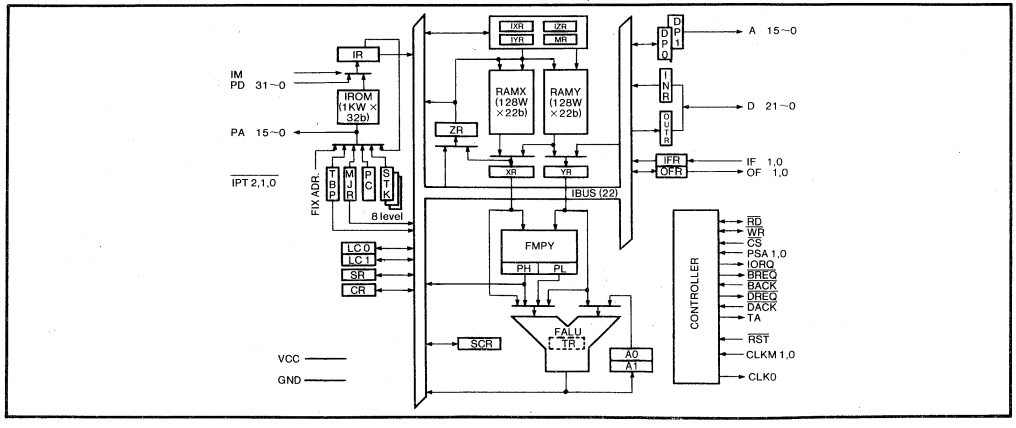
The MSM6992 is capable of functioning in the master mode as a multiprocessor or in the slave mode as a microcomputer I/O processor, hence this device can be readily incorporated into large scale systems with highly flexible system configurations.

Major MSM6992 applications include analysis for speech recognition and speech analysis/synthesis in speech processing equipment, high speed modems, codec, and echo cancellers in communication equipment. This device can also be effectively used for meter control, robotics and in audio equipment.

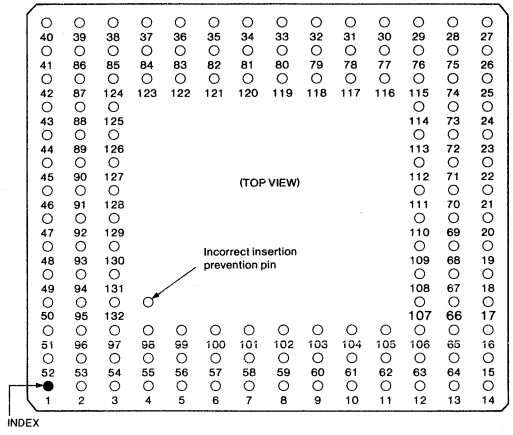
FEATURES

- Instruction cycle
  100nS/125nS
- Arithmetic formats
  Floating-point arithmetic 16E6
  Fixed-point arithmetic 16-bit
  Logical arithmetic 22-bit
- Built-in 1K-word × 32-bit instruction RAM (Also usable as data ROM)
- Built-in 1K-word × 32-bit instruction ROM
- 32-bit wide horizontal microinstruction
- 64K-word program memory area
- 64K-word data memory area
- Multiprocessor interface
- Microcomputer interface (8-bit & 16-bit)
- DMA controller connection capability
- Maximum 15-bit shift function (left or right)
- Double loop function
- +5V power supply
- Low power consumption, 400 mW
- 132-pin ceramic PGA package
- 2μm silicon gate CMOS

BLOCK DIAGRAM



PIN CONFIGURATION



Pin No.	Pin name	I/O	Pin No.	Pin Name	I/O	Pin No.	Pin name	I/O	Pin No.	Pin Name	I/O
1	$\overline{DREQ}$	O	34	D18	I/O	67	PD5	I	100	TA	O
2	PSA0	I	35	D15	I/O	68	PD3	I	101	PD28	I
3	CLK0	O	36	D13	I/O	69	PA0	O	102	PD25	I
4	*	I	37	D10	I/O	70	PA1	O	103	PD21	I
5	IM	I	38	D8	I/O	71	PA4	O	104	PD17	I
6	PD30	I	39	D5	I/O	72	PA6	O	105	PD15	I
7	PD29	I	40	NC	–	73	PA8	O	106	PD13	I
8	GND	–	41	D2	I/O	74	GND	–	107	PD10	I
9	PD24	I	42	GND	–	75	PA15	O	108	PD7	I
10	PD22	I	43	A2	O	76	$\overline{IPT0}$	I	109	PD4	I
11	PD19	I	44	VCC	–	77	*	I	110	PD0	I
12	VCC	–	45	A6	O	78	*	I	111	PA2	O
13	PD14	I	46	A7	O	79	OF0	O	112	VCC	–
14	NC	–	47	NC	–	80	GND	–	113	PA9	O
15	PD11	I	48	A12	O	81	D17	I/O	114	PA11	O
16	PD8	I	49	A14	O	82	D14	I/O	115	PA14	O
17	PD6	I	50	$\overline{RD}$	I/O	83	D11	I/O	116	$\overline{IPT1}$	I
18	GND	–	51	$\overline{BREQ}$	O	84	VCC	–	117	VCC	–
19	PD2	I	52	$\overline{DACK}$	I	85	D7	I/O	118	OF1	O
20	PD1	I	53	$\overline{CS}$	I	86	D3	I/O	119	D19	I/O
21	NC	–	54	VCC	–	87	D0	I/O	120	D16	I/O
22	PA3	O	55	MCLK0	I	88	A0	O	121	D12	I/O
23	PA5	O	56	$\overline{RST}$	I	89	A3	O	122	D9	I/O
24	PA7	O	57	PD31	I	90	A5	O	123	D6	I/O
25	PA10	O	58	PD27	I	91	A9	O	124	D4	I/O
26	PA12	O	59	PD26	I	92	A10	O	125	D1	I/O
27	PA13	O	60	PD23	I	93	A13	O	126	A1	O
28	$\overline{IPT2}$	I	61	PD20	I	94	IF1	I	127	A4	O
29	*	I	62	PD18	I	95	GND	–	128	A8	O
30	IF0	I	63	PD16	I	96	$\overline{BACK}$	I	129	A11	O
31	*	I	64	PD12	I	97	NC	–	130	A15	O
32	D21	I/O	65	PD9	I	98	PSA1	I	131	$\overline{WR}$	I/O
33	D20	I/O	66	NC	I	99	MCLK1	I	132	IORQ	O

Note: Pins marked by an * must be connected to ground.

PIN DESCRIPTION

Pin symbol	I/O	Function
$PA_{15} \sim PA_0$	O	Program memory address output pins • These pins address external program memory. • On reset this address goes to zero.
$PD_{31} \sim PD_0$	I	Program memory data input pins • Input to external program memory data.
IM	I	Internal ROM selector input pin • This signal is used to select between internal or external program memory. for internal program mode IM="1" for external program mode IM="0"
$A_{15} \sim A_0$	O (3-state)	Data memory address output pins • Designates the external data memory and external I/O addresses.
$D_{21} \sim D_0$	I/O (3-state)	Data memory data input/output pins • Parallel input and output of external data memory, microprocessor, or I/O bus data.
$\overline{IPT_{2,1,0}}$	I	3-level interrupt input pins (active low) • Interrupts accepted during the "sequence" operations. • Interrupts are accepted if interrupt level is greater than interrupt priority set in control register and fixed address corresponding to interrupt level is passed to program memory address bus. Interrupt priorities are: $\overline{IPT_2} > \overline{IPT_1} > \overline{IPT_0}$
$IF_1 \sim IF_0$	I	Universal input flag pins • Inputs to set flag in IFR register.
$OF_1 \sim OF_0$	I	Universal output flag pins • Output of OFR latch.
$\overline{RD}$	I/O (3-state)	Read control input/output pin (active low) • Output of external data memory and I/O device read control signals when in master mode. • Input of read control signals from the host MPU and other DSPs when in slave mode.
$\overline{WR}$	I/O (3-state)	Write control input/output pin (active low) • Output of external data memory and I/O device write control signals when in master mode. • Input of write control signals from the host MPU and other DSPs when in slave mode.
$\overline{CS}$	I	Chip select input pin (active low) • MSM6992 is in slave mode when this signal is active and the input/output data. Port ($D_{21} \sim D_0$) is enabled.
$PSA_1 \sim PSA_0$	I	Port select address input pin • INR/OUTR ports connected to data input/output pins are selected according to the host MPU data bit length when MSM6992 is in slave mode.

PSA1	PSA0	Host CPU		
		8-bit	16-bit	MSM6992
0	0	INR 21~16 ↔$D_5 \sim D_0$ OUTR 21~16	INR 21~16 ↔$D_5 \sim D_0$ OUTR 21~16	INR 21~0 ↔$D_{21} \sim D_0$ OUTR 21~0
0	1	INR 15~8 ↔$D_7 \sim D_0$ OUTR 15~8	INR 15~0 ↔$D_{15} \sim D_0$ OUTR 15~0	INR 21~0 ↔$D_{21} \sim D_0$ OUTR 21~0
1	0	INR 7~0 ↔$D_7 \sim D_0$ OUTR 7~8	NOP	INR 21~0 ↔$D_{21} \sim D_0$ OUTR 21~0
1	1	NOP	NOP	INR 21~0 ↔$D_{21} \sim D_0$ OUTR 21~0

III

PIN DESCRIPTION (CONT.)

Pin symbol	I/O	Function
IORQ	O (3-state)	I/O request output pin • This signal indicates whether the write or read operation is with respect to external data memory or I/O device. I/O request when IORQ = "1" Data memory request when IORQ = "0"
$\overline{\text{BREQ}}$	O	Bus request output pin (active low) • Signal to request external data bus. • Access requests passed to external devices are invalid when this DSP is accessed by external MPU ($\overline{\text{CS}}$ = "0").
$\overline{\text{BACK}}$	I	Bus acknowledge input pin (active low) • Signal to indicate that external data bus is available. • The DSP has access to bus if request signal is sent to external device ($\overline{\text{BREQ}}$ = "0") and the $\overline{\text{BACK}}$ signal is active, that is, a full "hand shake" must take place.
$\overline{\text{DREQ}}$	O	DMA request output pin (active low) • Data transfer request signal for data transfer between external memory and the DSP when in DMA mode. • $\overline{\text{DREQ}}$ is reset after transfer of one word of data has been completed to maximize utilization of system bus.
$\overline{\text{DACK}}$	I	DMA acknowledge input pin (active low) • Input signal indicating DMA cycle is enabled by external DMA control.
TA	O	Table data access indicator • TA = "1" when data is read from the program memory.
$\overline{\text{RST}}$	I	Reset input pin (active low) • This signal initializes all internal states of DSP. • The reset signal must be applied for a period greater than one machine cycle. • If reset input signal is applied for more than five machine cycles, internal clock synchronization is effected in addition to internal initialization.
MCLK0,1	I	Master clock input pin • Master clock obtained by input of external clock (50 ±10% duty) with frequency four times the machine cycle
CLKO	O	Internal system clock output pin
V_{CC}	–	+5V power supply pin
GND	–	Ground pin

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Limit	Unit
Supply voltage	V_{CC}	GND Basis	−0.5 ~ +7.0	V
Input voltage	V_{IN}		−0.5 ~ V_{CC}+0.5	V
Output voltage	V_{OUT}		−0.5 ~ V_{CC}+0.5	V
Storage temperature	T_{stg}		−65 ~ +150	°C
Power dissipation	Pd	Ta = 25°C		W

Operating Range

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
Operating temperature	T_{OP}	0	25	70	°C
"H" input voltage	V_{IH}	2.2		V_{CC}+0.3	V
"L" input voltage	V_{IL}	−0.3		0.8	V

DC Characteristics

(V_{CC} = 5V ±5%, Ta=0~70°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input leak current	I_{LI}	$0 \leqq V_{IN} \leqq V_{CC}$	−10		10	μA
Output leak current	I_{LO}	$0 \leqq V_{OUT} \leqq V_{CC}$	−10		10	μA
"H" output current	V_{OH}	I_{OH} = −400μA	2.4			V
"L" output current	V_{OL}	I_{OL} = 2.0mA			0.4	V
Stand-by supply current	Iccs	$0 \leqq V_I \leqq V_{CC}$		15		mA
Operation supply current	Icco	tϕMC=31.25nS		80		mA

Capacitance

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input capacitance	C_{IN}	f = 1MHz			10	pF
Output capacitance	C_{OUT}				20	pF

AC Characteristics

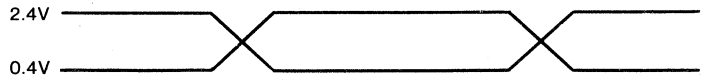
● Clock Timing

(Ta = 0 ~ 70°C, V_{DD} = 5V ±5%)

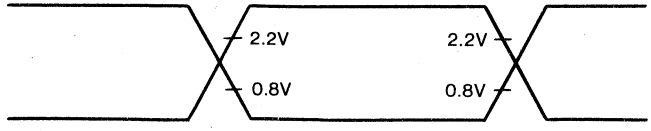
Symbol	Parameter	Condition	Min	Typ	Max	Unit
$t_{\phi MC}$	MCLK cycle time		31.25	–	DC	ns
$t_{\phi MH}$	MCLK high level pulse width		13	–	–	ns
$t_{\phi ML}$	MCLK low level pulse width		13	–	–	ns
$t_{\phi Mr}$	MCLK rise time	Voltage at timing measurement point = 0.8V & 2.2V	–	–	5	ns
$t_{\phi Mf}$	MCLK fall time		–	–	5	ns
$t_{\phi C}$	CLKO cycle time		125	–	–	ns
$t_{\phi H}$	CLKO high level pulse width		T-10	–	–	ns
$t_{\phi L}$	CLKO low level pulse width		3T-20	–	–	ns
$t_{\phi r}$	CLKO rise time	Voltage at timing measurement point = 0.8V & 2.2V	–	–	10	ns
$t_{\phi f}$	CLKO fall time		–	–	10	ns
t_{RSTS}	$\overline{RST}$ set-up to MCLK↓		10	–	–	ns
t_{RSTH}	$\overline{RST}$ hold after MCLK↓		10	–	–	ns
t_{RSTW}	$\overline{RST}$ pulse width		$2t_{\phi MC}$* $4t_{\phi MC}$	–	–	ns

$T = t_{\phi C/4}$ * Refer to User's Manual.

Note 1: AC test input waveform



Note 2: Voltage at AC timing measurement point



External Instruction Operation

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{PAD}	$PA_{15} \sim PA_0$ output delay		–	–	55	ns
t_{PAH}	$PA_{15} \sim PA_0$ hold after CLKO↓		–5	–	–	ns
t_{PDS}	$PD_{31} \sim PD_0$ set-up to CLKO↓		24	–	–	ns
t_{PDH}*	$PD_{31} \sim PD_0$ hold after CLKO↓		T	–	–	ns
t_{TAD}	TA Output delay		–	–	60	ns
t_{TAH}	TA hold after CLKO↓		–	–	40	ns

* When using MSM6992 at low speed, it is necessary to latch memory output once to satisfy hold time.

Write/Read Operation (Master mode)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{AD}	$A_{15} \sim A_0$ delay		–	–	50	ns
t_{AH}	$A_{15} \sim A_0$ hold after CLKO↓		–5	–	–	ns
t_{WA}	$A_{15} \sim A_0$ hold after WR↑		–15	–	–	ns
t_{WRD}	$\overline{WR}$ output delay		–	–	T+20	ns
t_{WRH}	$\overline{WR}$ hold after CLKO↓		–	–	20	ns
t_{WW}	$\overline{WR}$ pulse width		3T-20	–	–	ns
t_{DOD}	$D_{21} \sim D_0$ output delay	C_L=100pF	–	–	T+40	ns
t_{DOH}	$D_{21} \sim D_0$ hold after CLKO↓	C_L=100pF	0	–	–	ns
t_{RDD}	$\overline{RD}$ output delay CLKO↓		–	–	T+20	ns
t_{RDH}	$\overline{RD}$ hold after CLKO↓		–	–	20	ns
t_{RR}	$\overline{RD}$ pulse width		3T-20	–	–	ns
t_{DIS}	$D_{21} \sim D_0$ set-up to CLKO	C_L=100pF	35	–	–	ns
t_{DIH}	$D_{21} \sim D_0$ hold after CLKO↓	C_L=100pF	0	–	–	ns
t_{IOQD}	IORQ output delay		–	–	60	ns
t_{IOQH}	IORQ hold after CLKO↓		–	–	40	ns

Read/Write Operation (Slave mode)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{AR}	$\overline{CS}$, $PSA_{0,1}$ setup to $\overline{RD}\downarrow$		0	–	–	ns
t_{RA}	$\overline{CS}$, $PSA_{0,1}$ hold after $\overline{RD}\uparrow$		20	–	–	ns
t_{RR}	$\overline{RD}$ pulse width		50	–	–	ns
t_{RD}	$D_{21} \sim D_0$ access from $\overline{RD}\downarrow$	C_L=100pF	–	–	60	ns
t_{DF}	$D_{21} \sim D_0$ float after $\overline{RD}\uparrow$	C_L=100pF	10	–	100	ns
t_{AW}	$\overline{CS}$, $PSA_{0,1}$ setup to $\overline{WR}\downarrow$		20	–	–	ns
t_{WA}	$\overline{CS}$, $PSA_{0,1}$ hold after $\overline{WR}\uparrow$		20	–	–	ns
t_{WW}	$\overline{WR}$ pulse width		50	–	–	ns
t_{DW}	$D_{21} \sim D_0$ setup to $\overline{WR}\uparrow$	C_L=100pF	20	–	–	ns
t_{WD}	$D_{21} \sim D_0$ hold after $\overline{WR}\uparrow$	C_L=100pF	30	–	–	ns
t_{CS}	$\overline{CS}$ setup to CLKO$\downarrow$		40	–	–	ns
t_{CH}	$\overline{CS}$ hold after CLKO$\downarrow$		0	–	–	ns
t_{DS}	$D_{21} \sim D_0$ setup to CLKO$\downarrow$	C_L=100pF	40	–	–	ns
t_{DH}	$D_{21} \sim D_0$ hold after CLKO$\downarrow$	C_L=100pF	0	–	–	ns

III

DMA Write/Read Operation

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{DRQ}	$\overline{DREQ}$ output delay (CLKO$\downarrow$)		–	–	30	ns
t_{AKQ}	$\overline{DREQ}$ output delay ($\overline{DACK}\downarrow$)		–	–	8T+30	ns
t_{AKS}	$\overline{DACK}$ setup to CLKO$\downarrow$		30	–	–	ns
t_{AKH}	$\overline{DACK}$ hold after CLKO$\downarrow$		10	–	–	ns
t_{AKC}	$\overline{DACK}$ setup to $\overline{RD}/\overline{WR}$		0	–	–	ns
t_{CAK}	$\overline{DACK}$ hold after $\overline{RD}/\overline{WR}$		20	–	–	ns
t_{RW}	$\overline{RD}/\overline{WR}$ pulse width		50	–	–	ns
t_{DC}	$D_{21} \sim D_0$ setup to $\overline{WR}\uparrow$	CL=100pF	20	–	–	ns
t_{CD}	$D_{21} \sim D_0$ hold after $\overline{WR}\downarrow$	C_L=100pF	30	–	–	ns
t_{RD}	$D_{21} \sim D_0$ access from $\overline{RD}\downarrow$	C_L=100pF	–	–	60	ns
t_{DF}	$D_{21} \sim D_0$ float after $\overline{RD}\uparrow$	C_L=100pF	10	–	100	ns

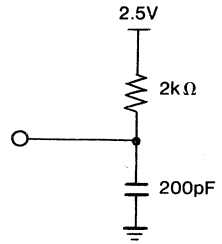
BREQ & BACK Timing

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{BRQ}	$\overline{BREQ}$ output delay (CLKO↓)		–	–	50	ns
t_{BQK}	$\overline{BREQ}$ output delay ($\overline{BACK}$↓)		–	–	8T+50	ns
t_{BKS}	$\overline{BACK}$ setup to CLKO↓		30	–	–	ns
t_{BKH}	$\overline{BACK}$ hold after CLKO↓		10	–	–	ns
t_{ZDA}	Address enable delay ($\overline{BACK}$↓)		–	–	4T+60	ns
t_{DZA}	Address disable delay ($\overline{BACK}$↑)		–	–	4T+60	ns
t_{ZDB}	Data Bus enable delay ($\overline{BACK}$↓)	C_L=100pF	–	–	5T+60	ns
t_{DZB}	Data Bus disable delay ($\overline{BACK}$↑)	C_L=100pF	–	–	4T+60	ns

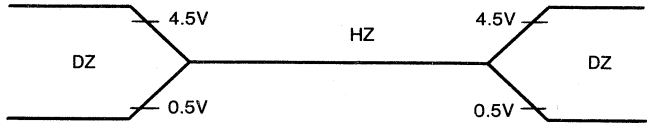
Interrupt & Port Timing

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{IPS}	$\overline{ITP_0}$ ~ $\overline{ITP_2}$ setup to CLKO↓		40	–	–	ns
t_{IPH}	$\overline{ITP_0}$ ~ $\overline{ITP_2}$ hold after CLKO↓		10	–	–	ns
t_{IFS}	IF_0 ~ IF_1 setup to CLKO↓		40	–	–	ns
t_{IFH}	IF_0 ~ IF_1 hold after CLKO↓		10	–	–	ns
t_{OFD}	OF_0 ~ OF_1 output delay		–	–	50	ns

Note 3: Output HZ and DZ test load circuit

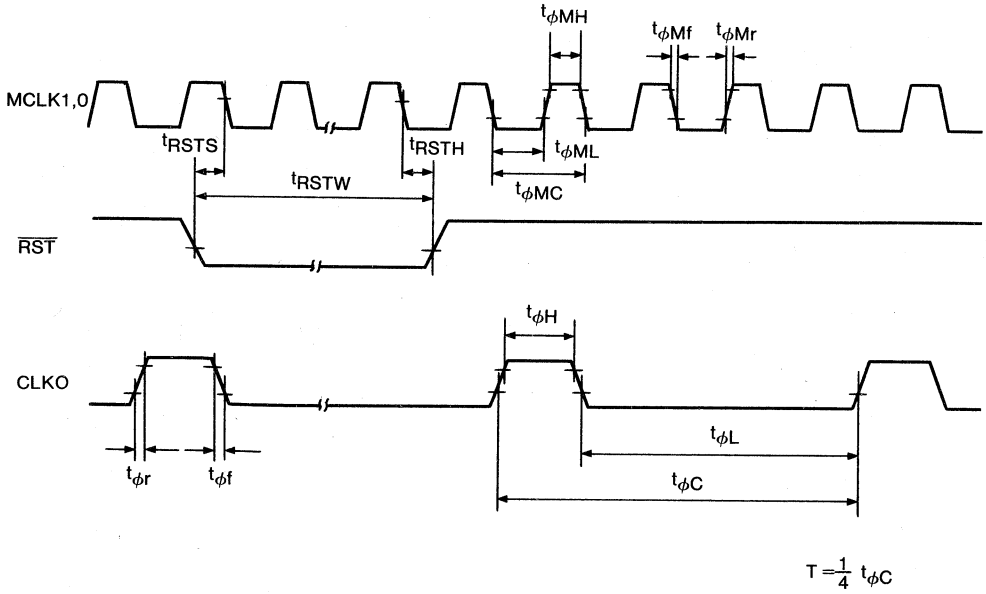


Note 4: Voltages at HZ and DZ timing measurement points

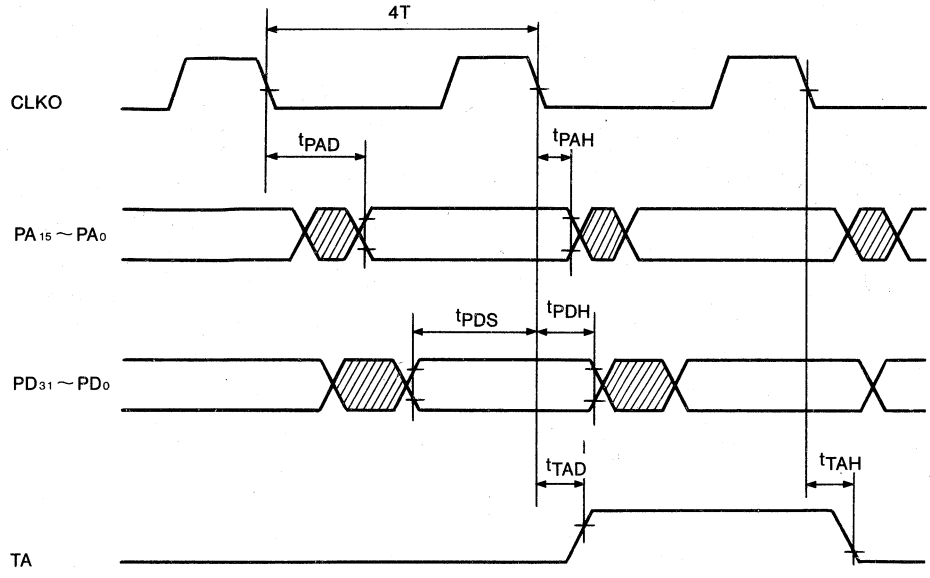


TIMING CHARTS

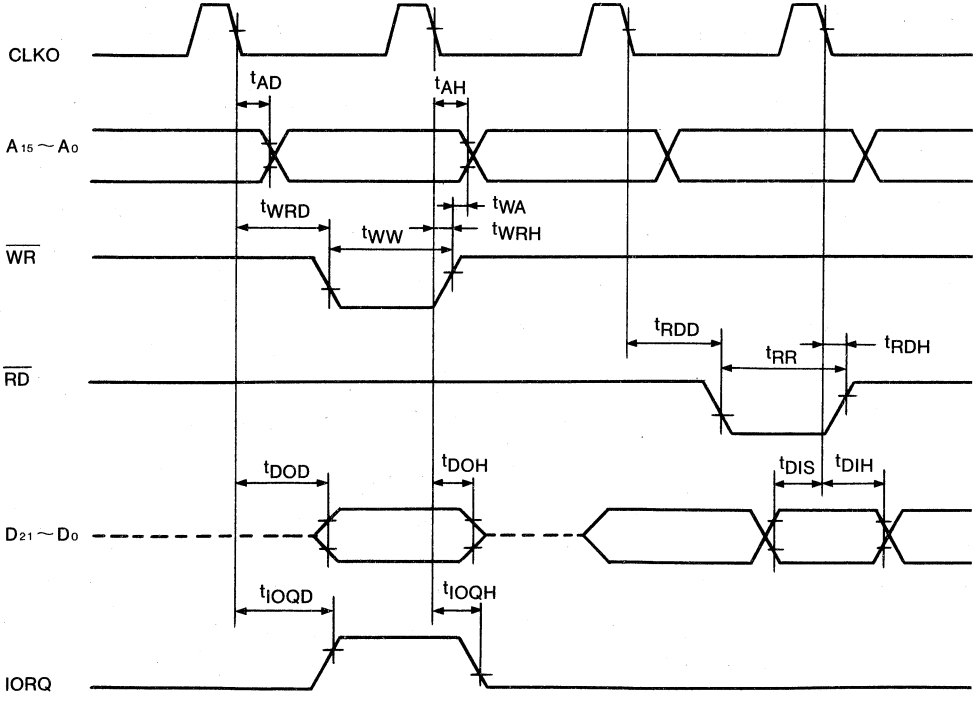
Clock



External Instruction Operation

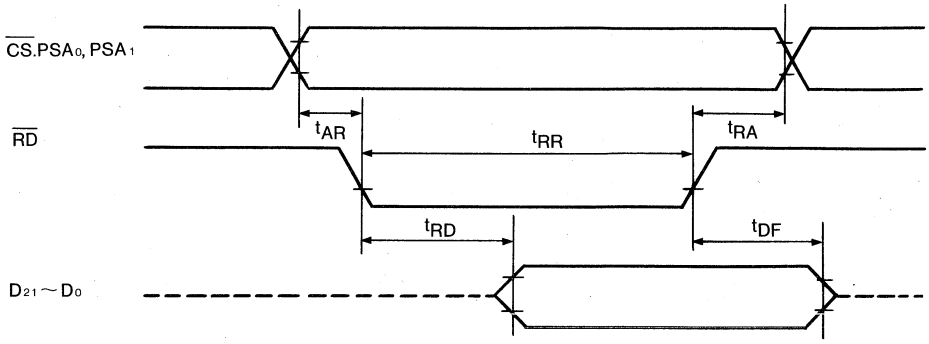


Write/Read Operation (Master mode)

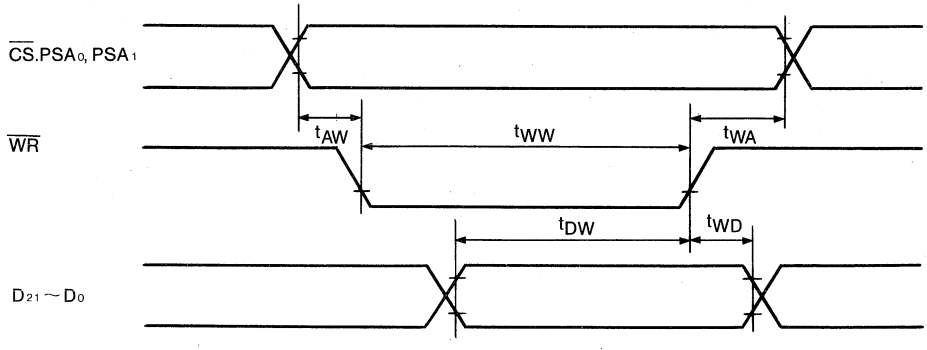


III

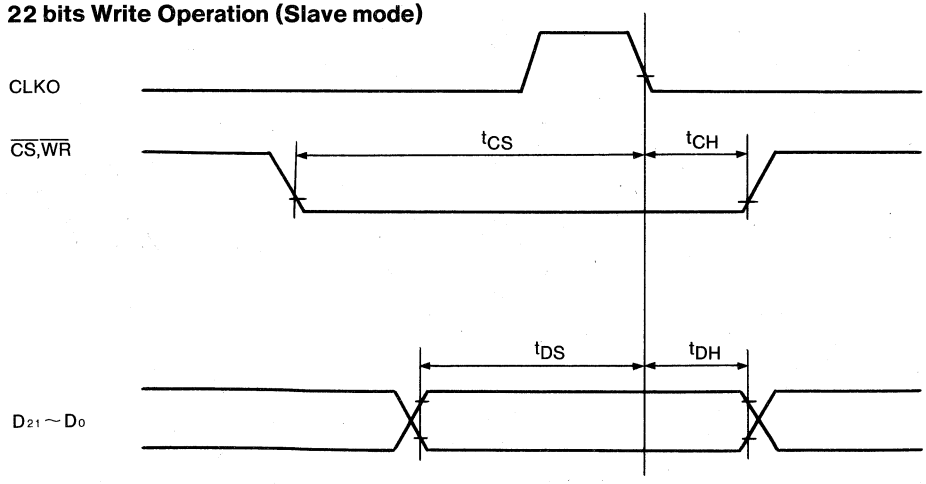
Read Operation (Slave mode)



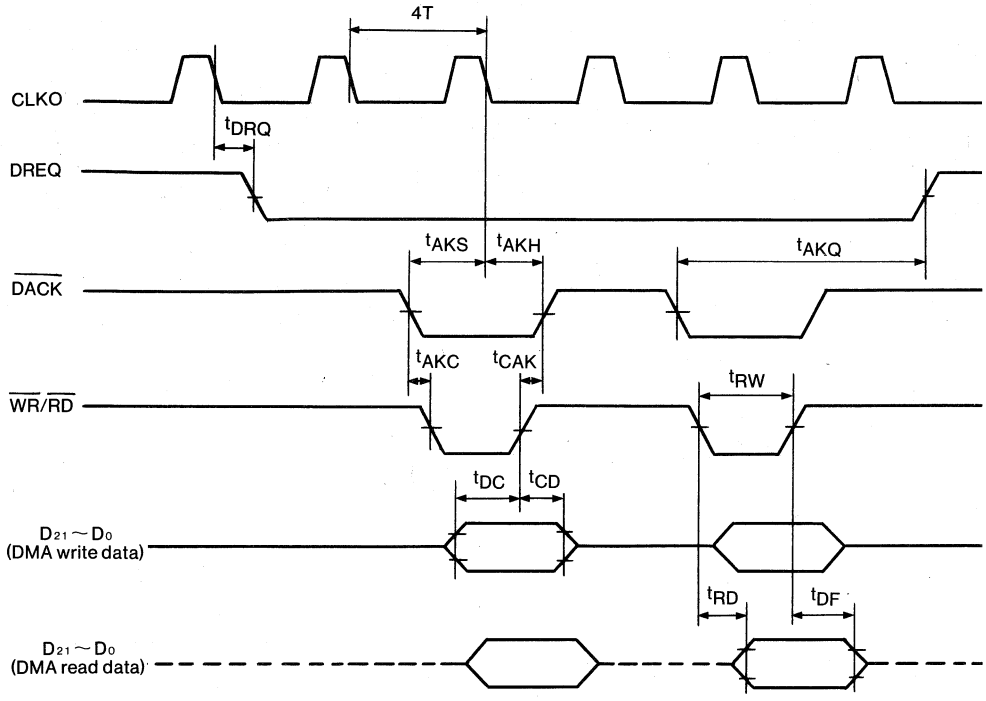
8, 16 bits Write Optation (Slave mode)



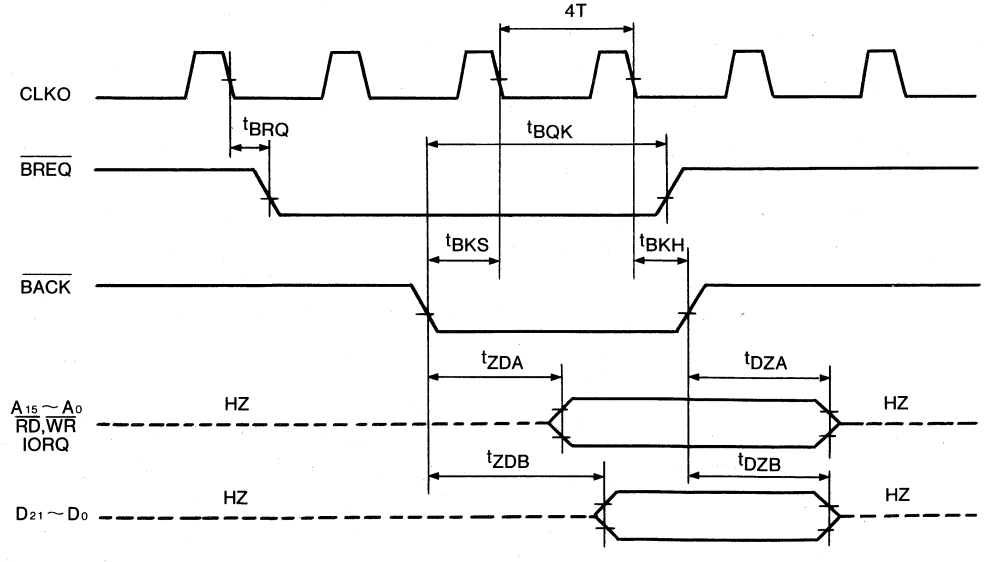
22 bits Write Operation (Slave mode)



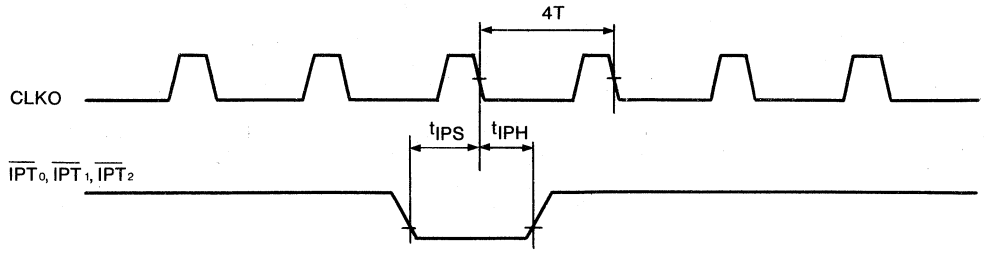
DMA Write/Read Operation BREQ & BACK Timing



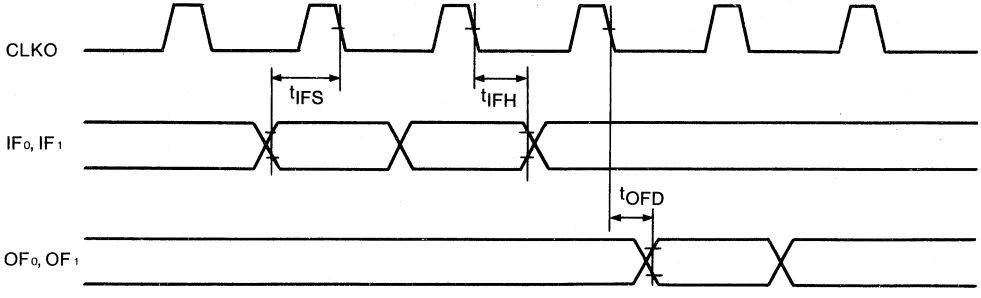
BREQ & BACK Timing

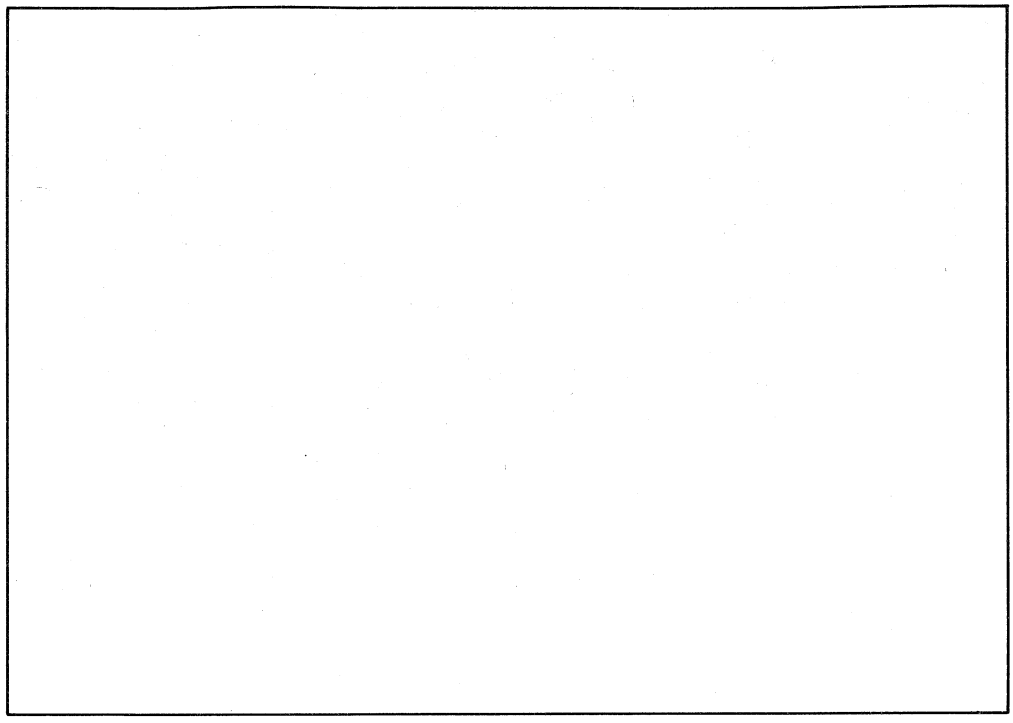


Interrupt Timing



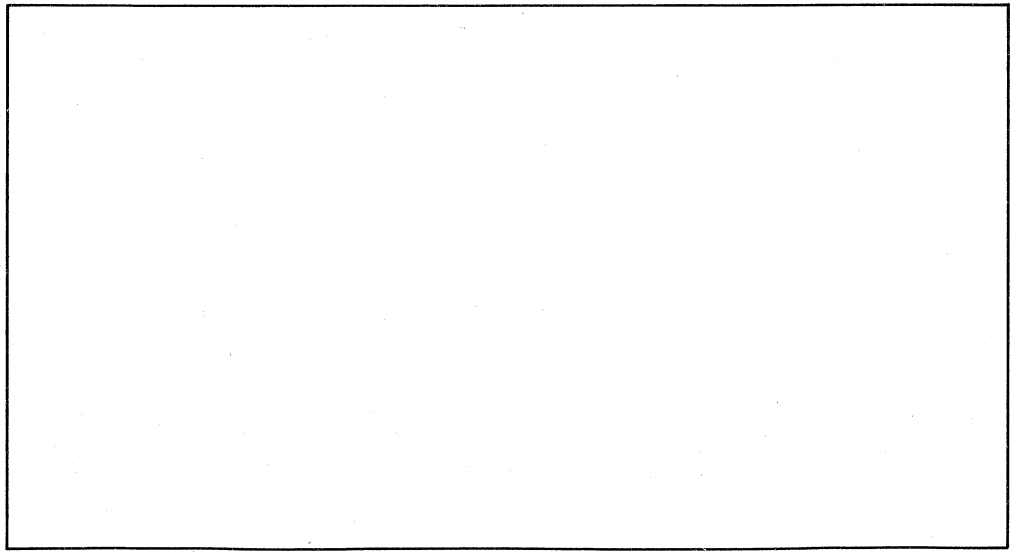
Port Input/Output Timing





F. CELLULAR MOBILE PHONE

III



OKI semiconductor

MSM6807/6817

BASEBAND FILTER LSI FOR CELLULAR MOBILE TELEPHONE

GENERAL DESCRIPTION

The MSM6807 and MSM6817 perform the baseband filtering function for PM transmitter/receiver in the cellular mobile telephone.

Each of MSM6807 and MSM6817 consists of a voice band-pass filter, pre-emphasis and de-emphasis circuits, a deviation limitter, a splatter filter, a receiver volume control attenuator, and a muting circuit and is fabricated by OKI's low power consumption CMOS silicon gate technology.

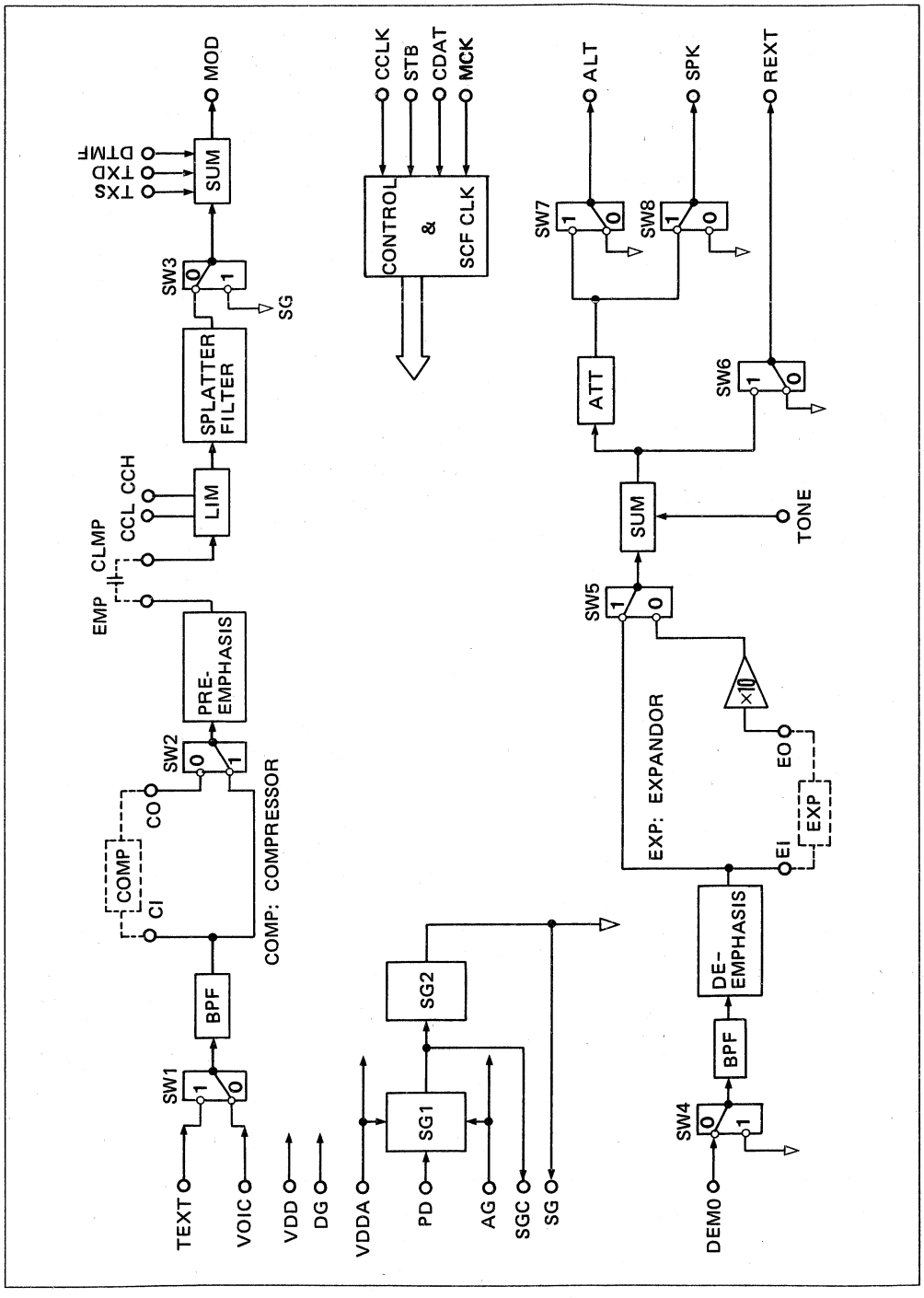
MSM6807 realizes the baseband filtering function for AMPS (Advanced Mobile Phone Service) system, while MSM6817 can realize the baseband filtering function for TACS (Total Access Communications System) system.

FEATURES

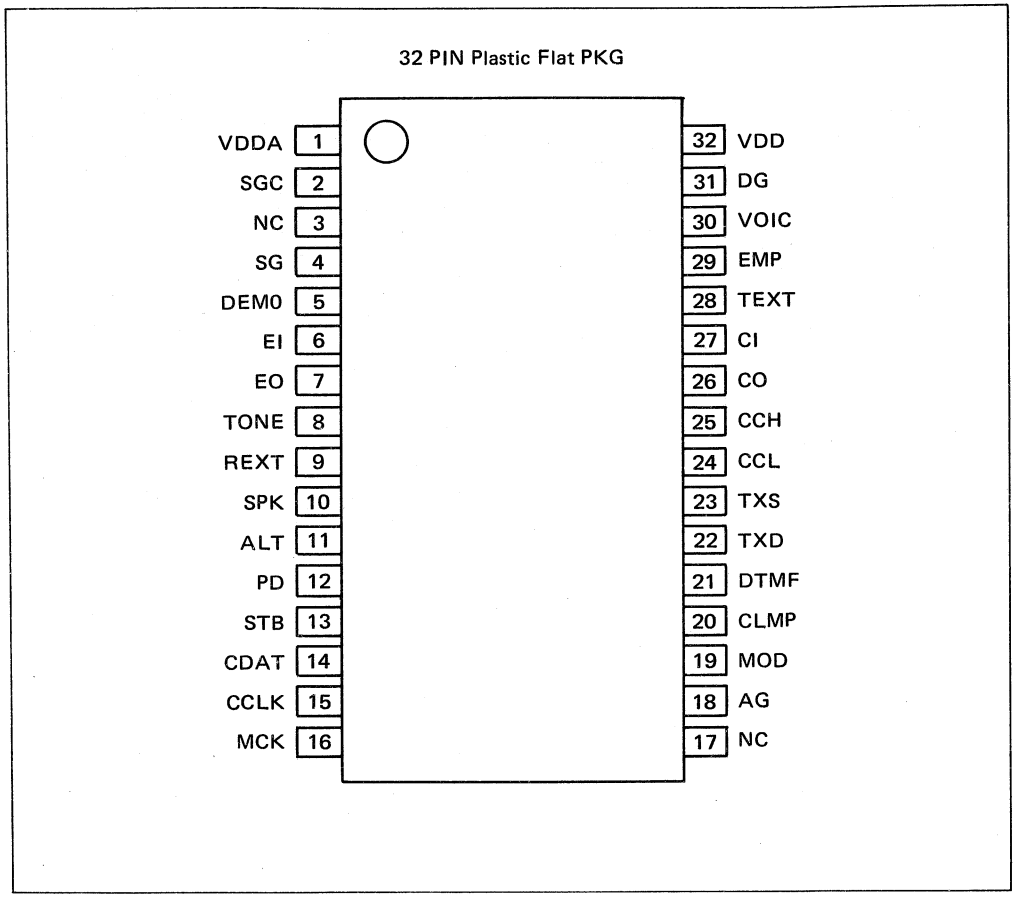
- Built-in mixing amplifier for transmitting MODEM data and DTMF signals.
- Built-in anti-aliasing filter and smoothing filter.
- Pre-emphasis, de-emphasis circuit on chip.
- Microcomputer interface serial control data.
- CMOS sillicon gate process.
- Power supply: +5V.
- Low power consumption: 30 mW.
- 32 pin plastic FLAT package.

III

BLOCK DIAGRAM

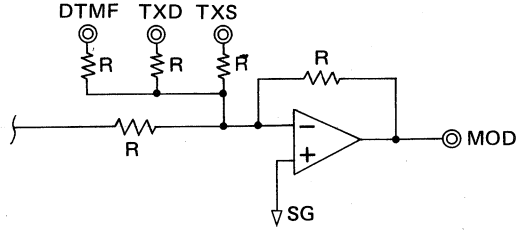


PIN CONFIGURATION



PIN DESCRIPTIONS

Pin Name	Pin No.	I/O	Function
VDDA	1	Power	Power supply pin for the analog circuit. +5V shall be applied.
SGC	2	O	This is the voltage reference for SG and is obtained by two-equal resistors division between VDDA and AG. It is necessary to be AC grounded for AG via a bypass capacitor of more than 2.2 μF so as to keep SG silent.
SG	4	O	SG is built-in analog ground. This voltage is nearly $\frac{VDDA}{2}$ V. To make its impedance lower, it is necessary to be AC grounded for AG via a bypass capacitor of more than 2.2 μF.
DEM0	5	I	Demodulated signals input. The demodulated baseband signal input to DEM0 can be sent out via ALT, SPK, REXT and EI.
EI	6	O	Expandor Input. When the control data B0 (refer to table 1) is logical 0, the transmitting circuit shall include the expandor portion of a 2:1 compandor. For every 1 dB change in input level to a 1:2 expandor, the change in output level is 2 dB. See Figure 6.
EO	7	I	Expandor Output. The signal input to EO has 20 dB gain between EO and SUM. Refer to description of pin 6 for details.
TONE	8	I	This is an input to SUM (Summing Amplifier) in the received audio line. In an application, DTMF SIDE TONE signal shall be injected.
REXT	9	O	These are received analog outputs. The REXT, SPK and ALT are selective. One of three outputs is available at any one time. The ALT and SPK output level can be adjusted by the CDAT. See Table 1.
SPK	10	O	
ALT	11	O	
PD	12	I	Power Down function enable pin. A logical 0 enables the power down function.

Pin Name	Pin No.	I/O	Function
STB	13	I	Strobe signal. STB, CDAT and CCLK control the status of internal switches, and attenuation of output level through ALT, SPK. See Table 1 for an explanation of how these control signals shall be set at.
CDAT	14	I	Control Data. Refer to the description of pin 13 for details.
CCLK	15	I	Control Clock. Refer to the description of pin 13 for details.
MCK	16	I	Master Clock. The MCK pin must be injected with a 1 MHz (±0.01%) input signal.
AG	18	Power	Analog Ground. This pin should be common with DG at the point which is as close as possible to the system ground.
MOD	19	O	Transmitting Modulated analog signals output. When the B1 bit of CDAT is logical 1, the input of SUM is connected to SG.
CLMP	20	I	LIM input. This pin should be connected to EMP through a capacitor.
DTMF	21	I	These are inputs to SUM in the transmitting line. The internal circuit is as follows.  These pins shall be connected with SG when these are not used. The value of R is about 70 kΩ.
TXD	22	I	
TXS	23	I	
CCL	24	I	This is an input pin for Deviation Limitter cramp level (low level). When any reference voltage is not supplied to this pin, a built-in reference voltage (-.375V with respect to SG) will be supplied to the Limitter. In this case, it is necessary to be AC grounded for AG via a bypass capacitor. In addition, the cramp level can be adjusted by supplying an external reference voltage. See Figure 5.

Pin Name	Pin No.	I/O	Function
CCH	25	I	This is an input pin for Deviation Limitter cramp level (high level). A built-in reference shows +.375V with respect to SG. Refer to the description about CCL.
CO	26	I	Compressor Output. When the control data B0 (refer to Table 1) is logical 0, the receive circuit shall include the compressor portion of a 2:1 compandor. For every 2 dB change in input level to a 2:1 compressor, the change in output level is 1 dB. See Figure 6.
CI	27	O	Compressor Input. Refer to the description about pin 26 for details.
TEXT	28	I	Tone External. Transmit baseband signals input. As TEXT is biased internally to SG with a resistor (200 kΩ), the interface must be implemented by AC-coupling.
EMP	29	O	Emphasis Output. Refer to the description about pin 20.
VOIC	30	I	Transmitting baseband signals input. Refer to the description about pin 28 for detials.
DG	31	Power	Digital Ground. This pin should be common with AG at the point which is as close as possible to the system ground.
VDD	32	Power	Power supply pin for the digital circuit. +5 V shall be supplied to this pin.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Condition	Min	Type	Max	Unit
Power Supply Voltage	V_{DD} V_{DDA}	T_a = +25°C With respect to AG or DG	-0.3	–	7	V
Analog Input Voltage*1	V_{IA}		-0.3	–	V_{DDA} +0.3	
Digital Input Voltage*2	V_{ID}		-0.3	–	V_{DD} +0.3	
Operating Temperature	T_{op}	—	-40	–	85	°C
Storage Temperature	T_{stg}		-55	–	125	

*1 TEXT, VOIC, DEM0, TONE, CLMP, TXS, TXD, DTMF
*2 CCLK, STB, CDAT, MCK, PD

Recommended Operating Conditions

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Power supply Voltage	V_{DD} V_{DDA}	With respect to AG or DG	4.75	5.0	5.25	V
Operating Temperature	T_{op}		-30	–	70	°C
Master Clock Frequency	f_{MCK}		0.9999	1	1.0001	MHz

III

DC AND DIGITAL INTERFACE CHARACTERISTICS

V_{DDA}, V_{DD} = 5V ±5%, T_a = -30 ~ 70°C

Parameter	Symbol	Condition	Min	Typ	Max	Unit	Note
Power Dissipation (standby)	I_{DD}	–	–	7	14	mA	–
	I_{DDS}		–	0.2	0.5		
Input Leak Current	I_{IL}	V_I = 0V	-10	–	10	μA	CCLK CDAT STB MCK PD
	I_{IH}	V_I = V_{DD}	-10	–	10		
Input Voltage	V_{IL}	–	0	–	0.3 V_{DD}	V	
	V_{IH}		0.7 V_{DD}	–	V_{DD}		

ANALOG INTERFACE CHARACTERISTICS

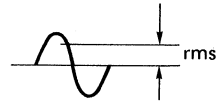
V_{DDA}, V_{DD} = 5V ±5%, T_a = −30 ~ 70°C

Parameter	Symbol	Condition	Min	Typ	Max	Unit	Note
Input Impedance	R_I	f ≦ 4 KHz	100	—	—	kΩ	*1
Deviation Limitter Cramp Level	V_{CCL}	V_{DDA} = 5 V With respect to SG	—	+0.375	—	V	CCL
	V_{CCH}		—	-0.375	—		CCH

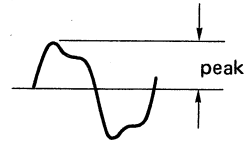
*1 TEXT, VOIC, DEM0, EO, CO, TONE, CLMP

Definitions of Units

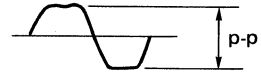
dBV_{rms} : 20*logV, where V denotes the root mean square value of the signal voltage.



dBVp : 20*logV, where V denotes the peak value of the signal voltage.



Vp-p : Peak-peak value of the signal voltage.



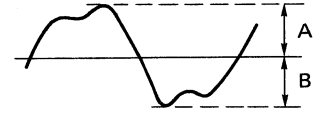
TRANSMIT CHARACTERISTICS (MOD)

V_{DDA}, V_{DD} = 5V ±5%, T_a = -30 ~ 70°C

Parameter	Symbol	Condition	Min	Typ	Max	Unit	Note
VOIC/TEXT Standard Deviation Input Level	V_{ITX}	Vo (MOD) =-8.2 dBVp fi=1 kHz	–	-11.2	–	dBVrms	
MOD Standard Deviation Distortion	D_{MOD}		–	–	-24	dB	SW2="1"
MOD MAX Deviation Output Level	V_{OTX}	Vi (VOIC) =0 dBVrms fi=1 kHz	–	–	-6	dBVp	SW3="0"
MOD Output Signal Peak Ratio*1	V_{SYM}		-5	–	-5	%	
TX-AUDIO Muting Attenuation	L_{TXM}	Vi (VOIC) =-11.2 dBVrms fi=1 kHz	40	–	–	dB	SW3="0" → "1"
TX-AUDIO BPF Characteristics	–	–	–	Figure 1	–	–	CI
TX-AUDIO Overall Response	–	–	–	Figure 2	–	–	MOD SW2="1" SW3="0"
MOD In-band Noise Level	–	0.3~3 kHz CMESS filter	–	–	-62	dBVrms	SW2="1"
MOD Out-band Noise Level	–	VOIC/TEXT silent	–	Figure 4	–	–	

*1 MOD output signal (after DC cutting)

100*(A/B-1) ; (%)

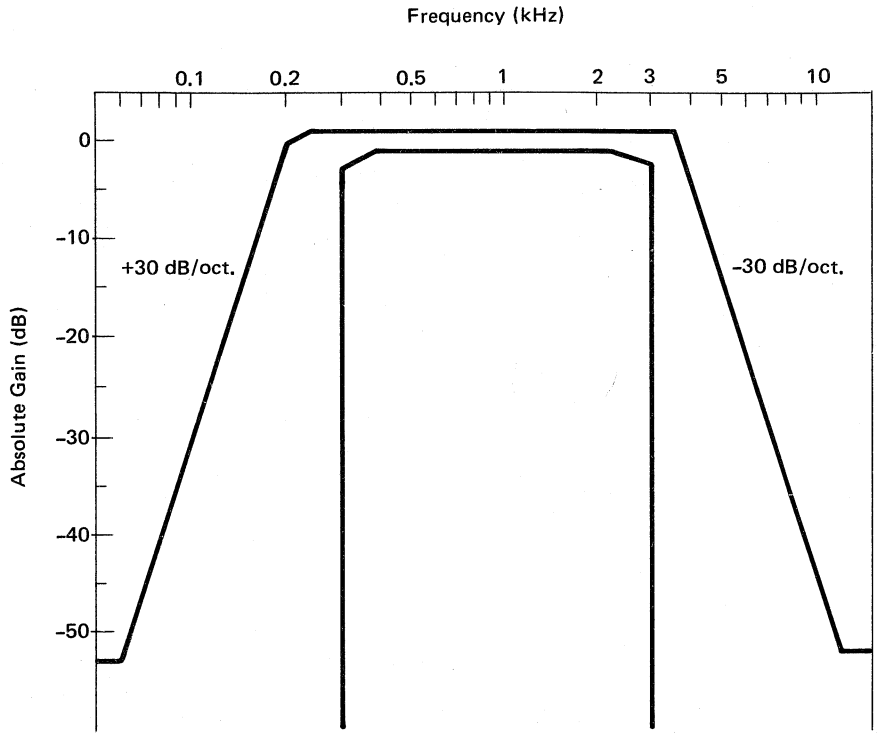


III

RECEIVE CHARACTERISTICS (ALT/SPK/REXT)

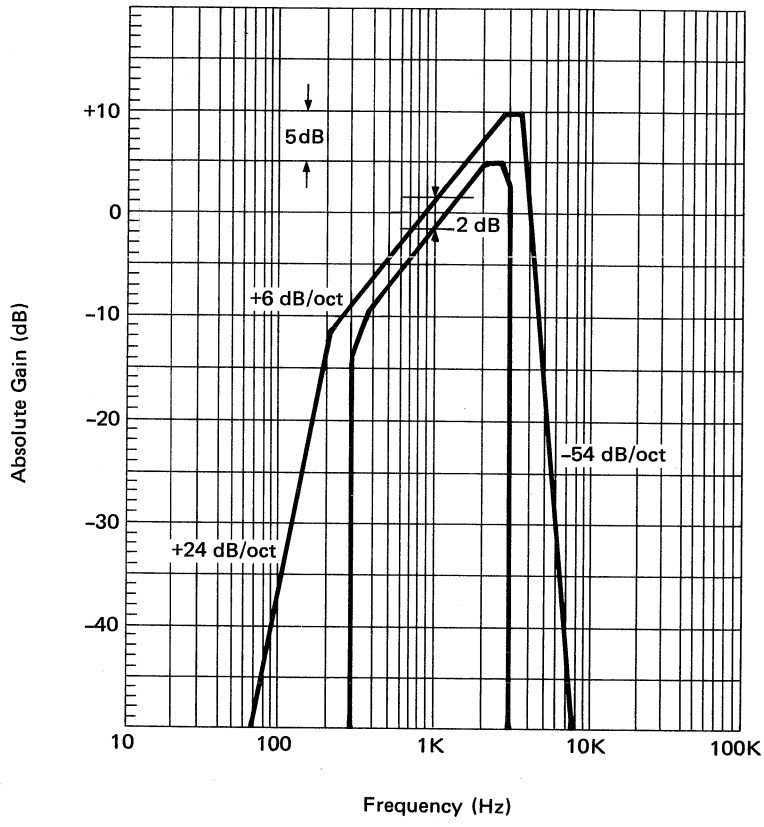
V_{DDA}, V_{DD} = 5V ±5%, T_a = -30 ~ 70°C

Parameter	Symbol	Condition	Min	Typ	Max	Unit	Note
ALT/SPK/REXT Standard Demodulation Output Level	V_{ORX}	Vi (DEM0) =-11.2 dBVrms fi=1 kHz ATT=0 dB	–	-11.2	–	dBVrms	SW5="1"
ALT/SPK/REXT Output Distortion	D_R		–	–	-40	dB	
ATT Attenuation Step	G_{ATT}	–	–	2.5	–	dB	
RX-AUDIO Overall Response	–	–	–	Figure 3	–	–	
ALT/SPK/REXT In-band Noise Level	–	CMESS filter 0.3 ~ 3.0 kHz	–	–	-62	dBVrms	
ALT/SPK/REXT Out-band Noise Level	–	–	–	Figure 4	–	–	



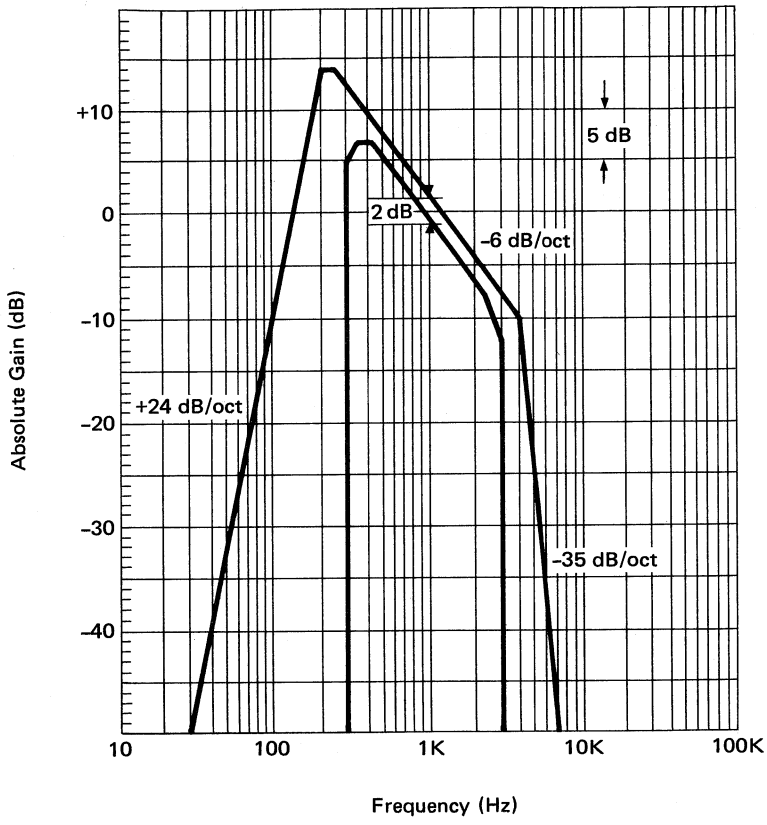
Upper Limits:	(1)	below 60 Hz	Less than	-53 dB
	(2)	200 Hz		-0.5 dB
	(3)	240 Hz		+1.0 dB
	(4)	240~3500 Hz		Flat
	(5)	above 12 kHz		-52 dB
Lower Limits:	(1)	300 Hz		-3 dB
	(2)	400 Hz		-1 dB
	(3)	400~2200 Hz		Flat
	(4)	3000 Hz		-2.6 dB

Figure 1 BPF Frequency Characteristics



Upper limits:	1	200 to 3000 Hz	: 6 dB/oct
	2	3000 to 3500 Hz	: Flat
Lower limits:	1	400 to 2250 Hz	: 2 dB below the upper limit line
	2	300 Hz	: 4.5 dB below 400 Hz
	3	2250 to 2500 Hz	: Flat
	4	3000 Hz	: 3 dB below 2500 Hz

Figure 2 TX-AUDIO Overall Response



Upper limits:	1	240 to 3800 Hz	: -6 dB/oct
	2	200 to 240 Hz	: Flat
Lower limits:	1	400 to 2250 Hz	: 2 dB below the upper limit line
	2	360 to 400 Hz	: Flat
	3	300 Hz	: 3 dB below 360 Hz
	4	3000 Hz	: 4.5 dB below 2250 Hz

Figure 3 RX-AUDIO Overall Response

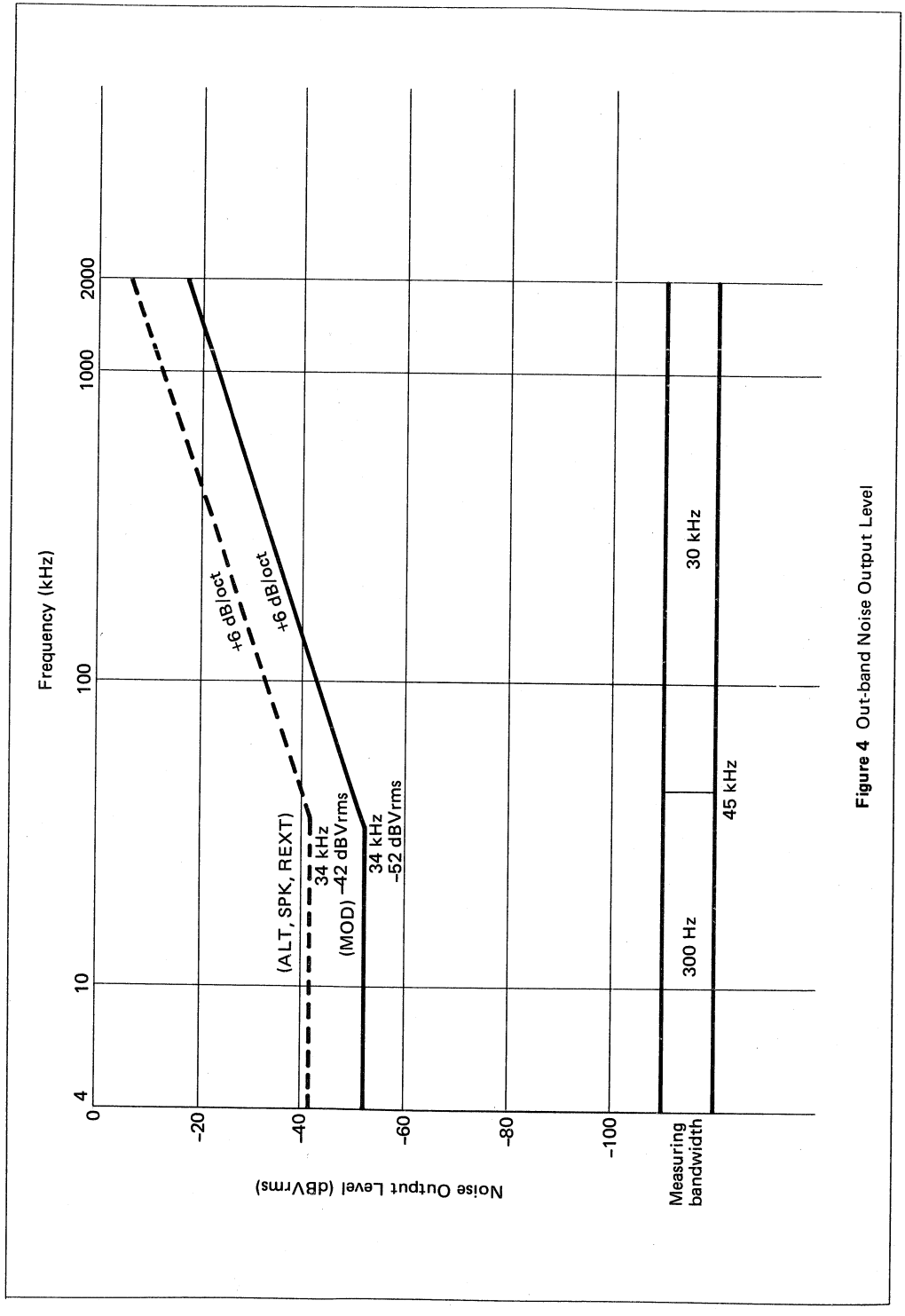
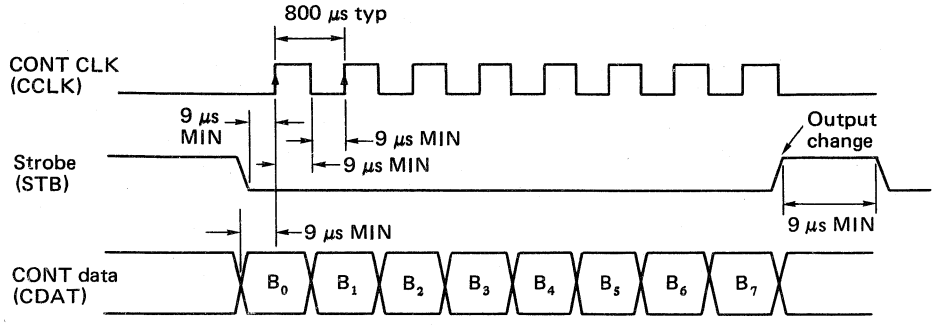


Figure 4 Out-band Noise Output Level

Control Pin Specifications



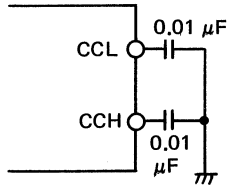
The CONT CLK (CCLK) is edge triggered.

Symbol	Name	Switch Status
B0	COMPANDOR selection	H: SW2 = "1", L: SW2 = "0" SW5 = "1", SW5 = "0"
B1	TX-AUDIO mute	H: SW3 = "1", L: SW3 = "0"
B2	RX-AUDIO mute	H: SW4 = "1", L: SW4 = "0"
B6	TEXT/VOIC selection	H: SW1 = "1", L: SW1 = "0"
B6, B7	ALT/SPK/REXT selection	B6 B7 output: 1 X REXT; 0 0 SPK; 0 1 ALT X: Irrespective of 1/0.

ATT CONT			Attenuation (dB)
B5	B4	B3	
0	0	0	0
0	0	1	2.5
0	1	0	5
0	1	1	7.5
1	0	0	10
1	0	1	12.5
1	1	0	15
1	1	1	17.5

Table 1

Internal Reference Voltage



CCL = VDDA/2 - 0.375 (V)
CCH = VDDA/2 + 0.375 (V)

External Reference Voltage

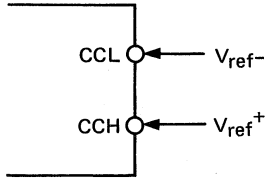


Figure 5 Deviation Limitter

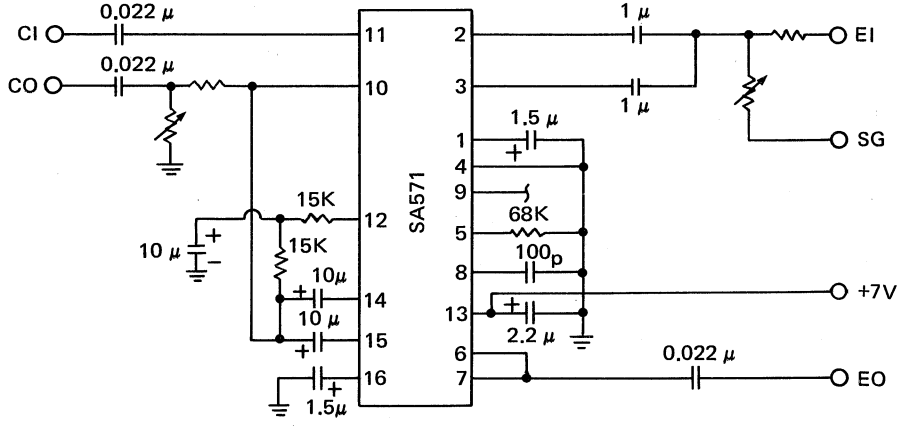
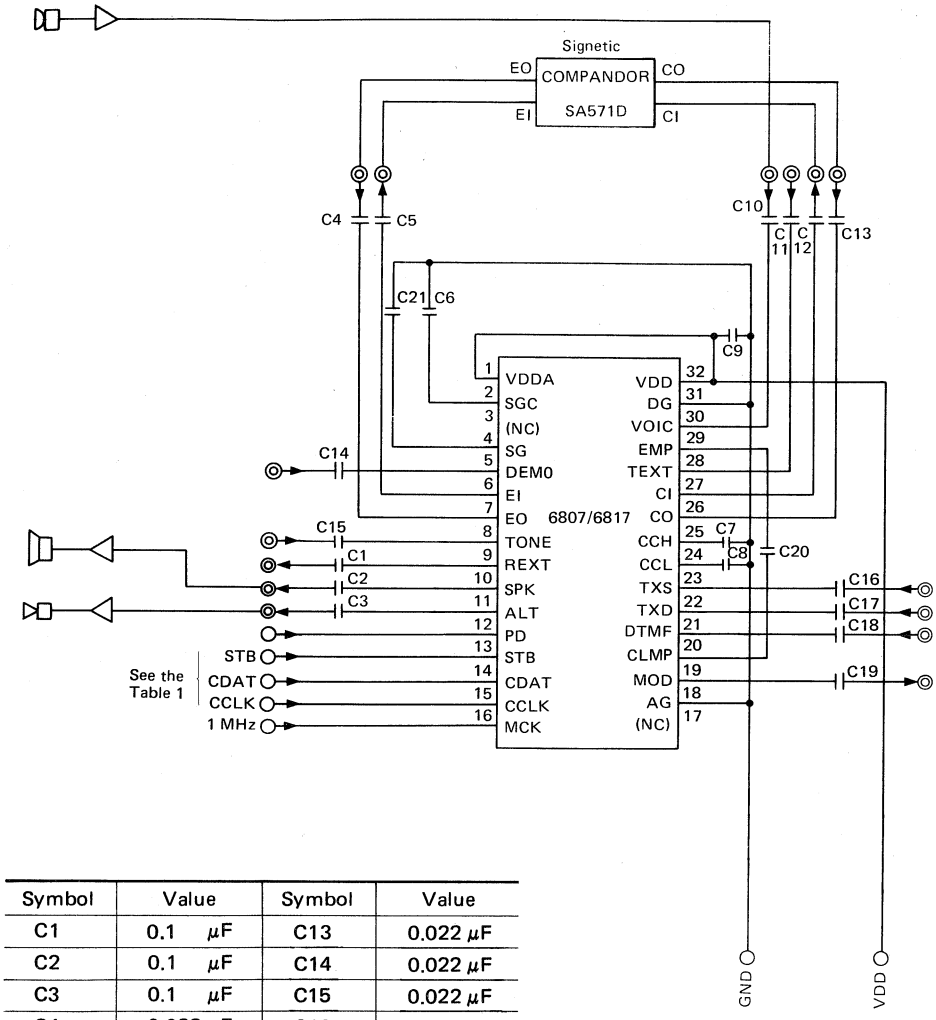


Figure 6 Compandor



Symbol	Value	Symbol	Value
C1	0.1 μF	C13	0.022 μF
C2	0.1 μF	C14	0.022 μF
C3	0.1 μF	C15	0.022 μF
C4	0.022 μF	C16	0.022 μF
C5	0.022 μF	C17	0.022 μF
C6	2.2 μF	C18	0.022 μF
C7	0.01 μF	C19	0.022 μF
C8	0.01 μF	C20	0.1 μF
C9	10 μF	C21	2.2 μF
C10	0.022 μF		
C11	0.022 μF		
C12	0.022 μF		

Figure 7 Application

III

MSM6808/6818

SPLIT FILTER LSI FOR MODEM FUNCTION IN THE CELLULAR MOBILE PHONE

GENERAL DESCRIPTION

The MSM6808 and MSM6818 perform the split filtering functions in the modem part of the cellular mobile phone.

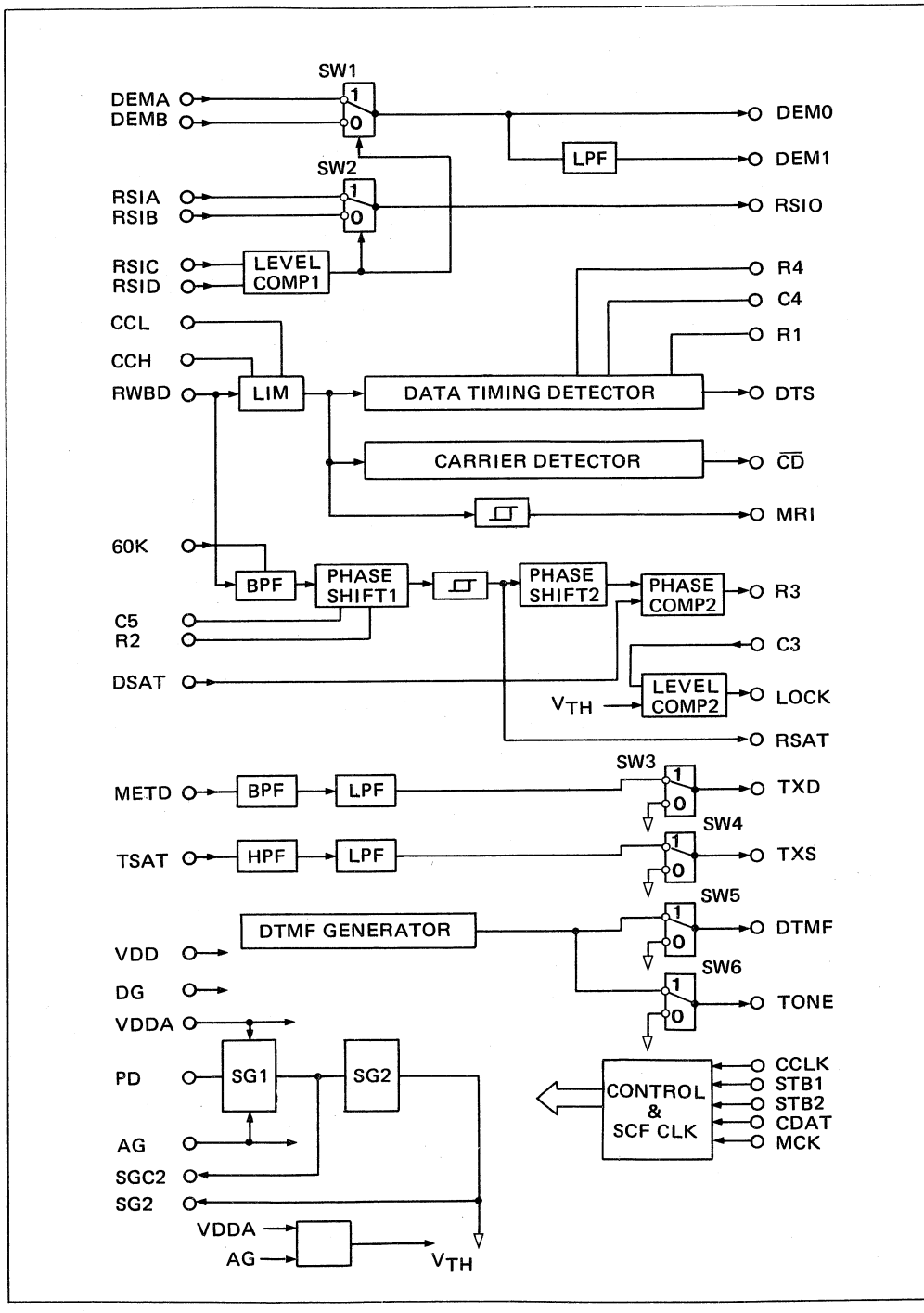
Each of the MSM6808 and MSM6818 consists of a Received Wide Band Data (RWBD) detecter, a MODEM DATA Signal (MODEM DATA) transmitter, a Supervisary Audio Tone (SAT) receiver, a SAT transmitter, and a DTMF signal transmitter and is fabricated by OKI's low power consumption CMOS silicon gate technology.

In combination with the MSM74017, MSM6808 can realize a 10K bps SPL modem for AMPS (Advanced Mobile Phone Service) system. MSM6818 can realize a 8K bps SPL modem for TACS (Total Access Communications System) system in combination with MSM74017.

FEATURES

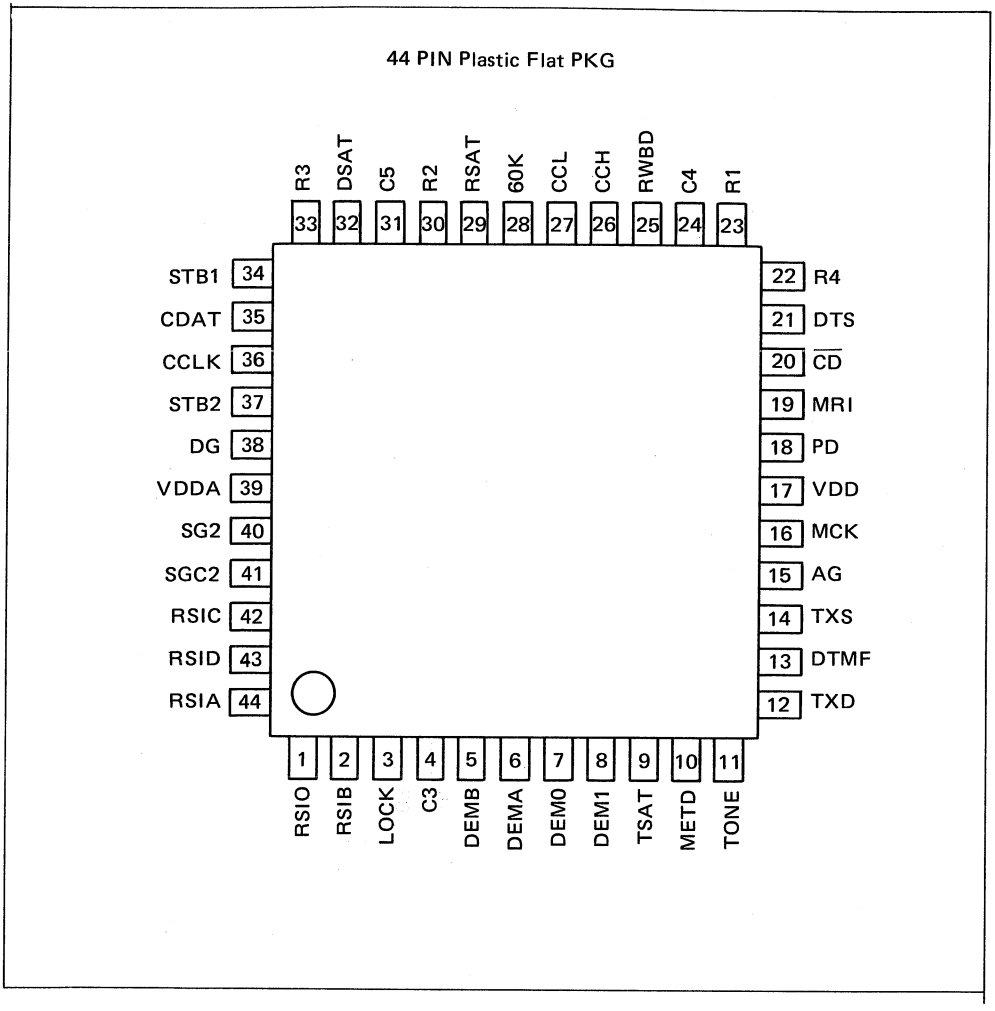
- Built-in timing re-generating circuit for received data.
- Built-in Switched Capaciter Filters for SAT and MODEM data.
- Built-in Anti-Aliasing filters and Smoothing Filters.
- DTMF generator circuit on chip.
- Received signal level comparator for diversity system.
- Microcomputer interface serial control data.
- Power supply: +5 V.
- Low power consumption: 40 mW (typ).
- 44-pin plastic FLAT package.

BLOCK DIAGRAM



III

PIN CONFIGURATION



PIN DESCRIPTION

Pin Name	Pin No.	I/O	Function
RSIO	1	O	Received signal Strength Output. The larger DC level applied to RSIA and RSIB is put out of RSIO.
RSIB	2	I	Received signal Strength Input (B). DC levels are applied to RSIA and RSIB pins.
LOCK	3	O	SAT (Supervisory Audio Tone) Lock. The LOCK determines whether RSAT (Received SAT) and TSAT (Transmitting SAT) are synchronized or not. The LOCK is set at logical 1, when the phase of DSAT exceeds +270° compared with that of the RSAT signal.
C3	4	I	Form LPF by connecting a resistor and a capacitor between R3 and C3. See Figure 7.
DEMB	5	I	Demodulated signal input (B). The DEMB pin is enabled if RSIC<RSID.
DEMA	6	I	Demodulated signal input (A). The DEMA pin is enabled if RSIC>RSID.
DEM0	7	O	Demodulated signal output (0). Connect this pin to DEM0 of MSM6807 or MSM6817.
DEM1	8	O	Demodulated signal output (1). Connect this pin to RWBD.
TSAT	9	I	Transmitting SAT signal. The phase of TSAT should be more than +270° compared with that of the RSAT output signal. The TSAT signal is same as the DSAT signal.
METD	10	I	Transmitting Manchester Encoded Data. See Figure 5.
TONE	11	O	DTMF SIDETONE output. Connect this pin to TONE of MSM6807 or MSM6817.
TXD	12	O	Transmitting Data. Digital data applied to METD becomes sinusoidal wave signals coming through filters.
DTMF	13	O	Dual Tone Multi Frequency. Each DTMF signal consists of two sinusoidal waves, one from a low group (697, 770, 852, 941 Hz) and the other from a high group (1209, 1336, 1477, 1633, 2016 Hz).

Pin Name	Pin No.	I/O	Function
DTMF	13	O	The level has +6 dB/oct. pre-emphasis characteristics. CCLK, STB2 and CDAT control the frequency, selection of dual tone or single tone. See Table 2.
TXS	14	O	Transmitting SAT. The digital signal input to TSAT becomes sinusoidal wave through a band limited filter.
AG	15	–	Analog Ground. This pin should be common with the DG at the point which is as close as possible to the system ground.
MCK	16	I	Master Clock. Use a 1 MHz (±0.01%) MCK.
VDD	17	–	Power supply pin for the digital circuit. +5V shall be applied.
PD	18	I	Power Down function enable pin. The PD signal selects power on or off; logical 0 enables the power down mode. In the power down mode, transmitting function, SAT function and DTMF output function are suspended.
MRI	19	O	Output for the Manchester Encoded data derived from RWBD input data. See Figure 5.
$\overline{CD}$	20	O	Carrier Detection. The carrier detector detects dotting pattern (1010101010) input to the RWBD. When the frequency of input signal to MSM6808 is approx. 5 kHz, the $\overline{CD}$ of MSM6808 becomes logical 0, while $\overline{CD}$ is logical 1 for any other frequencies. When the frequency of input signal to MSM6818 is approx. 4 kHz, the $\overline{CD}$ of MSM6818 becomes logical 0, while $\overline{CD}$ is logical 1 for any other frequencies.
DTS	21	O	Derived Timing Signal. Output for the timing clock derived from the RWBD input data. When a 5 kHz data is input to the RWBD of MSM6808, a 10 kHz signal is obtained. When a 4 kHz data is input to the RWBD of MSM6818, a 8 kHz signal is obtained.
R4	22	–	DTS sensitivity adjustment. An external resistor R9 shall be connected between R4 and SG2.

<table>
<tr><th>Pin Name</th><th>Pin No.</th><th>I/O</th><th>Function</th></tr>
<tr><td>R1</td><td>23</td><td>–</td><td>DTS phase adjustment.
An external resistor R8 shall be connected between R1 and SG2.</td></tr>
<tr><td>C4</td><td>24</td><td>–</td><td>DTS phase adjustment.
If phase cannot be sufficiently adjusted, connect an external capacitor between C4 and R1.
C4 pin shall be left open when it is not used.</td></tr>
<tr><td>RWBD</td><td>25</td><td>I</td><td>Received Wide Band Data input pin.
Received data and SAT signal are input to this pin.
This pin shall be connected to DEM1 directly.</td></tr>
<tr><td>CCH</td><td>26</td><td>–</td><td rowspan="2">An external resistor and capacitor shall be connected between CCL and CCH.
See Figure 7.</td></tr>
<tr><td>CCL</td><td>27</td><td>–</td></tr>
<tr><td>60K</td><td>28</td><td>I</td><td>The 60K signal controls the center frequency of the BPF (RWBD block).
According to the SAT frequency input to RWBD, the frequency of control signal input to the 60K pin changes as below.
<table>
<tr><th colspan="2">SAT (WRBD)</th><th colspan="2">RS10</th><th colspan="2">Center Frequency (BPF)</th></tr>
<tr><td>5970</td><td rowspan="3">Hz</td><td>59.7</td><td rowspan="3">kHz</td><td>5970</td><td rowspan="3">Hz</td></tr>
<tr><td>6000</td><td>60.0</td><td>6000</td></tr>
<tr><td>6030</td><td>60.3</td><td>6030</td></tr>
</table>
Normally the 60K control signal is made by the digital PLL.</td></tr>
<tr><td>RSAT</td><td>29</td><td>O</td><td>Received SAT.
The RSAT output signal is applied to the external digital PLL.
The phase of RSAT through the PLL exceeds +270°.</td></tr>
<tr><td>R2</td><td>30</td><td>–</td><td>Received SAT signal phase adjustment.
An external resistor R7 shall be connected between R2 and SG2.</td></tr>
<tr><td>C5</td><td>31</td><td>–</td><td>Received SAT signal phase adjustment.
An external capacitor C22 shall be connected between C5 and R2.</td></tr>
<tr><td>DSAT</td><td>32</td><td>I</td><td>Data SAT.
The "PHASE COMP2" judges the difference of the phase between RSAT and DSAT.
The phase of DSAT (equals to TSAT) should be exceeded +270° compared with RSAT.
In other cases, RSAT and TSAT is not locked.
See "BLOCK DIAGRAM".</td></tr>
</table>

III

Pin Name	Pin No.	I/O	Function
R3	33	–	Refer to the description of pin 4.
STB1	34	I	Strobe 1. Refer to the description of CDAT.
CDAT	35	I	Serial Control Data. The CDAT and STB1 signal control the internal switches. DTMF frequency is selected by CDAT and STB2. See Table 1.
CCLK	36	I	Control timing clock. See Table 1.
STB2	37	I	Strobe 2. Refer to the description of CDAT.
DG	38	–	Digital Ground. This pin should be common with the AG at the point which is as close as possible to the system ground.
VDDA	39	–	Power supply pin for the analog circuit. +5V shall be applied.
SG2	40	Power	SG2 is built-in analog ground. This voltage is nearly $\frac{VDDA}{2}$ V, so the analog line interface must be implemented by AC-coupling except in the case of connecting with MSM6807 (in case of MSM6808) or MSM6817 (in case of MSM6818). To make its impedance lower, it is necessary to be AC grounded for AG via a bypass capacitor of more than 2.2 μF.
SGC2	41	Power	This is voltage reference for SG and is obtained by two-equal resistors division among VDDA and AG. It is necessary to be AC grounded for AG via a bypass capacitor of more than 2.2 μF so as to keep SG2 silent.
RSIC	42	I	Received signal Strength input (C). The rectified signal of the RSIA input signal is applied to this pin through external LPF. See "APPLICATION".
RSID	43	I	Received signal Strength input (D). Same as RSIC, the rectified signal of the RSIB is applied to this pin through LPF. The DC levels of RSIC and RSID determine the status of SW1, SW2. See Table 1.
RSIA	44	I	Received signal Strength input (A). DC levels are applied to RSIA and RSIB.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Condition	Min	Type	Max	Unit
Power Supply Voltage	V_{DD} V_{DDA}	T_a = +25°C With respect to AG or DG	-0.3	–	7	V
Analog Input Voltage*1	V_{IA}		-0.3	–	V_{DDA} +0.3	
Digital Input Voltage*2	V_{ID}		-0.3	–	V_{DD} +0.3	
Operating Temperature	T_{op}		-40	–	85	°C
Storage Temperature	T_{stg}		-55	–	125	

*1 DEMA, DEMB, RSIA, RSIB, RWBD
*2 RSIC, RSID, RS10, DSAT, METD, TSAT, STB1, STB2, CDAT, MCK, CCLK

Recommended Operating Conditions

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Power supply Voltage	V_{DD} V_{DDA}	With respect to AG or DG	4.75	5.0	5.25	V
Operating Temperature	T_{op}		-30	–	70	°C
Master Clock Frequency	f_{MCK}		0.9999	1	1.0001	MHz

III

DC AND DIGITAL INTERFACE CHARACTERISTICS

V_{DDA}, V_{DD} = 5V ±5%, T_a = -30 ~ 70°C

Parameter	Symbol	Condition	Min	Typ	Max	Unit	Note
Power Dissipation (standby)	I_{DD}	–	–	10	15	mA	–
	I_{DDS}		–	6	9		
Input Leak Current	I_{IL}	V_I = 0V	-10	–	10	μA	MCK STB1 STB2 CCLK CDAT
	I_{IH}	V_I = V_{DD}	-10	–	10		
Input Voltage	V_{IL}	–	0	–	0.3 V_{DD}		
	V_{IH}		0.7 V_{DD}	–	V_{DD}		
Output Voltage	V_{OL}	I_{OL} = -1.6 mA	–	–	0.3 V_{DD}	–	DTS MRI $\overline{CD}$ RSAT
	V_{OH}	I_{OH} = 400 μA	0.7 V_{DD}	–	–		

ANALOG INTERFACE CHARACTERISTICS

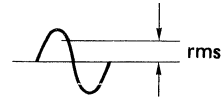
V_{DDA}, V_{DD} = 5V ±5%, T_a = -30 ~ 70°C

Parameter	Symbol	Condition	Min	Typ	Max	Unit	Note
Input Impedance*1	R_{AIN}	–	100	–	–	kΩ	–

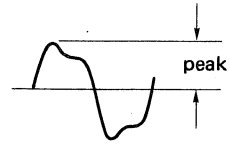
*1 RSIC, RSID, RWBD, METD, TSAT, DSAT

Definition of Units

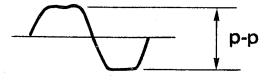
dBV_{rms} : 20*logV, where V denotes the root mean square value of the signal voltage.



dBVp : 20*logV, where V denotes the peak value of of the signal voltage.



Vp-p : Peak-peak value of the signal voltage.



III

DEM, RSSI CHARACTERISTICS

V_{DDA}, V_{DD} = 5V ±5%, T_a = -30 ~ 70°C

Parameter	Symbol	Condition		Min	Typ	Max	Unit	Note
DEM0 Output Level	V_{ODEM0}	Vi (DEM) = -14.2 dBVrms fi = 1 kHz		–	-11.2	–	dBVrms	+3dB
DEM1 Output Level	V_{ODEM1}			–	2.2	–	Vp-p	+12dB
RSIO Output Level	V_{ORSIL}	V_I=0V	RL≧100K	–	0	–	V	–
	V_{ORSIH}	V_I=3.15V		–	3.15	–		
RSSI Hysteresis	V_{HYS}	–		–	30	–	mV	RSIC RSID
DEM1 LPF Cut-off frequency	f_{CDEM}	At the point 2dB lower		20	–	–	kHz	–
DEM1 Undesired Wave Leakage	–	DEMA, DEMB silent		–	–	-50	dBVrms	–

RWBD SAT

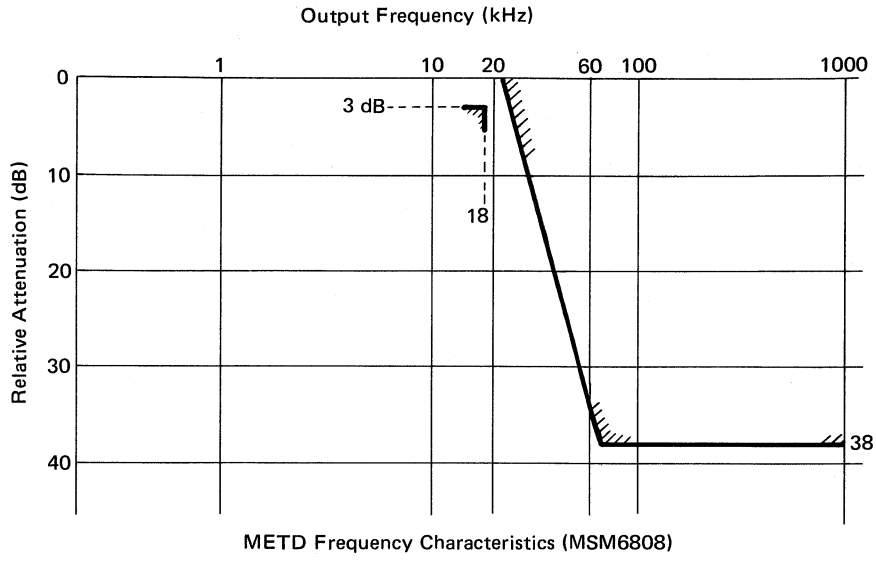
V_{DDA}, V_{DD} = 5V ±5%, T_a = −30 ~ 70°C

Parameter		Symbol	Condition			Min	Typ	Max	Unit	Note
DTS Output Duty Ratio		DR_{DTS}	Vi (RWBD) = 2.3Vp-p fi = 5 kHz			—	50	—	%	f_{DTS} = kHz
$\overline{CD}$	Sensitivity	FS_{CD1}	Vi(RWBD) =2.3Vp-p	MSM6808 fi = 3.5k±100Hz	MSM6818 fi = 2.8k±100Hz	—	V_{DD}	—	V	—
		FS_{CD2}		5k ± 100Hz	4k ± 100Hz	—	DG	—		
		FS_{CD3}		6.5k±100Hz	5.2k±100Hz	—	V_{DD}	—		
	Response	t_{D1}	Figure 5			—	—	2	ms	
		t_{D2}				2	—	—		
MRI/DTS Delay Time		t_d	R9 = 10 Ω R8 = 175 kΩ C4 open			—	21	—	μs	Figure 6
RSAT Sensitivity		V_{RSAT}	fi = 5970 Hz 6000 6030			-20	—	—	dBV-rms	

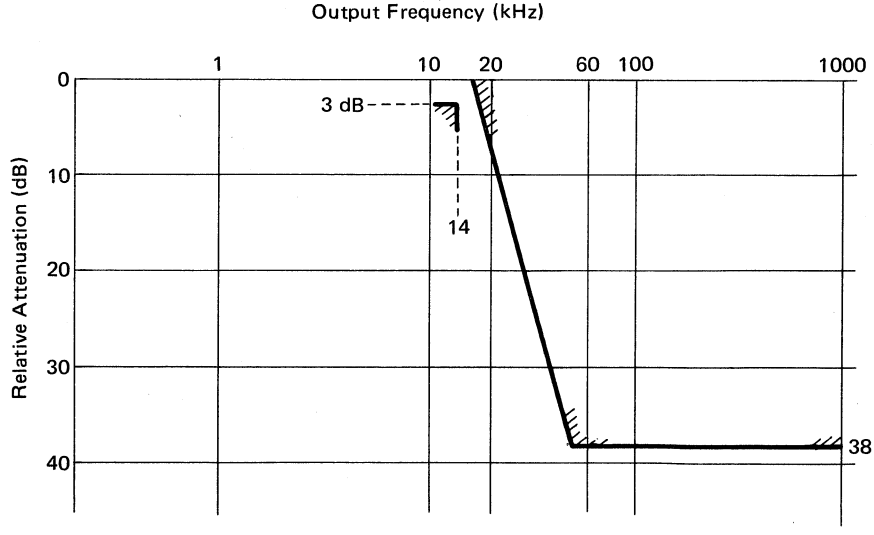
TX-AUDIO (TXD/TXS/DTMF) CHARACTERISTICS

V_{DDA}, V_{DD} = 5V ±5%, T_a = -30 ~ 70°C

Parameter	Symbol	Condition	Min	Typ	Max	Unit	Note
METD Output Level	V_{OTXD}	V_{IL} = 0 V, V_{IH} = V_{DD} fi = 10 kHz (MSM6808) fi = 8 kHz (MSM6818) square wave (50%)	—	-8.2	—	dBVp	SW3 = "1"
METD Frequency Characteristics	—	V_{IL} = 0 V, V_{IH} = V_{DD} square wave (50%)	Figure 1			—	—
TXS Output Level	V_{OTXS}	V_{IL} = 0 V, V_{IH} = V_{DD} square wave (50%) fi = 6 kHz	—	-23.2	—	dBVrms	SW4="1"
TSAT Frequency Characteristics	—	V_{IL} = 0 V, V_{IH} = V_{DD} square wave (50%)	Figure 2			—	—
DTMF Output Level	V_{OL1}	f0 = 697 Hz	—	-19.3	—	dBVrms	Emphasis (6dB/oct) Figure 3 MCK=1MHz
	V_{OL2}	770	—	-18.4	—		
	V_{OL3}	852	—	-17.6	—		
	V_{OL4}	941	—	-16.7	—		
	V_{OH1}	f0 = 1209 Hz	—	-14.5	—		
	V_{OH2}	1336	—	-13.6	—		
	V_{OH3}	1477	—	-12.8	—		
	V_{OH4}	1633	—	-11.9	—		
Sounder Output Level	V_{OTONE}	f0 = 2016 Hz	—	-25	—	dBVrms	SW6="1"
DTMF Side Tone Output Level	V_{ODST}	697, 1633 Hz Pair	—	-22	—	dBVrms	
DTMF Distortion	D_{DTMF}	—	—	—	10	%	—
DTMF Output Frequency Error	ΔF_{DTMF}	MCK = 1 MHz	-1.5	—	+1.5	%	—
TONE Undesired Wave Leakage	—	TXD/TXS/DTMF	—	—	-61	dBVrms	SW3="0" SW4="0" SW5="0"
Out-band Noise Level	—	TX-AUDIO RX-AUDIO	Figure 4			—	—



METD Frequency Characteristics (MSM6808)



METD Frequency Characteristic (MSM6818)

Figure 1

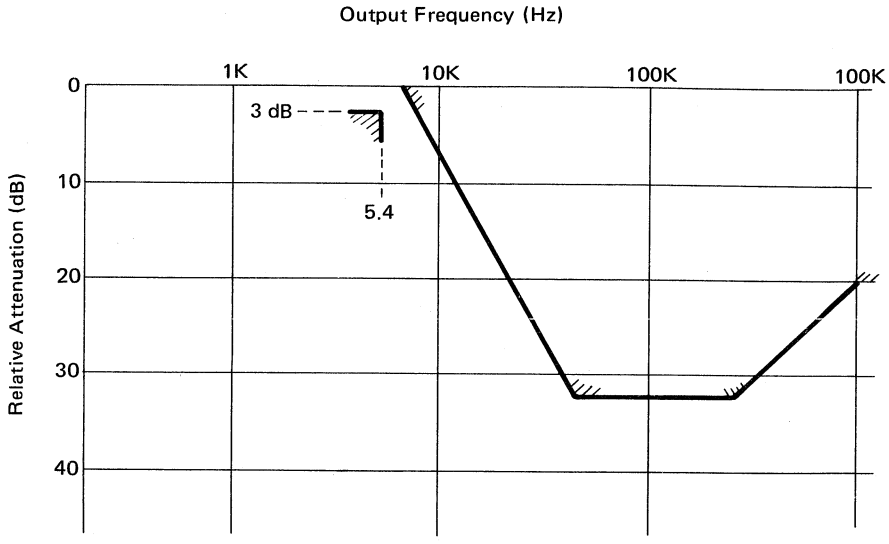


Figure 2 TSAT Frequency Characteristic

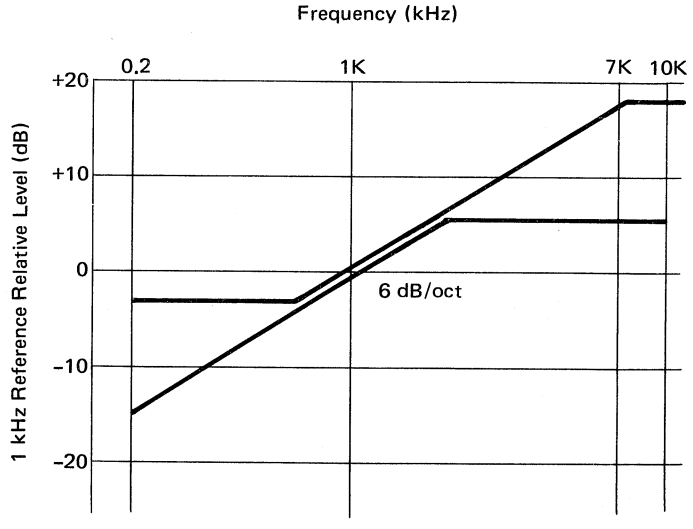


Figure 3 DTMF Emphasis Characteristic

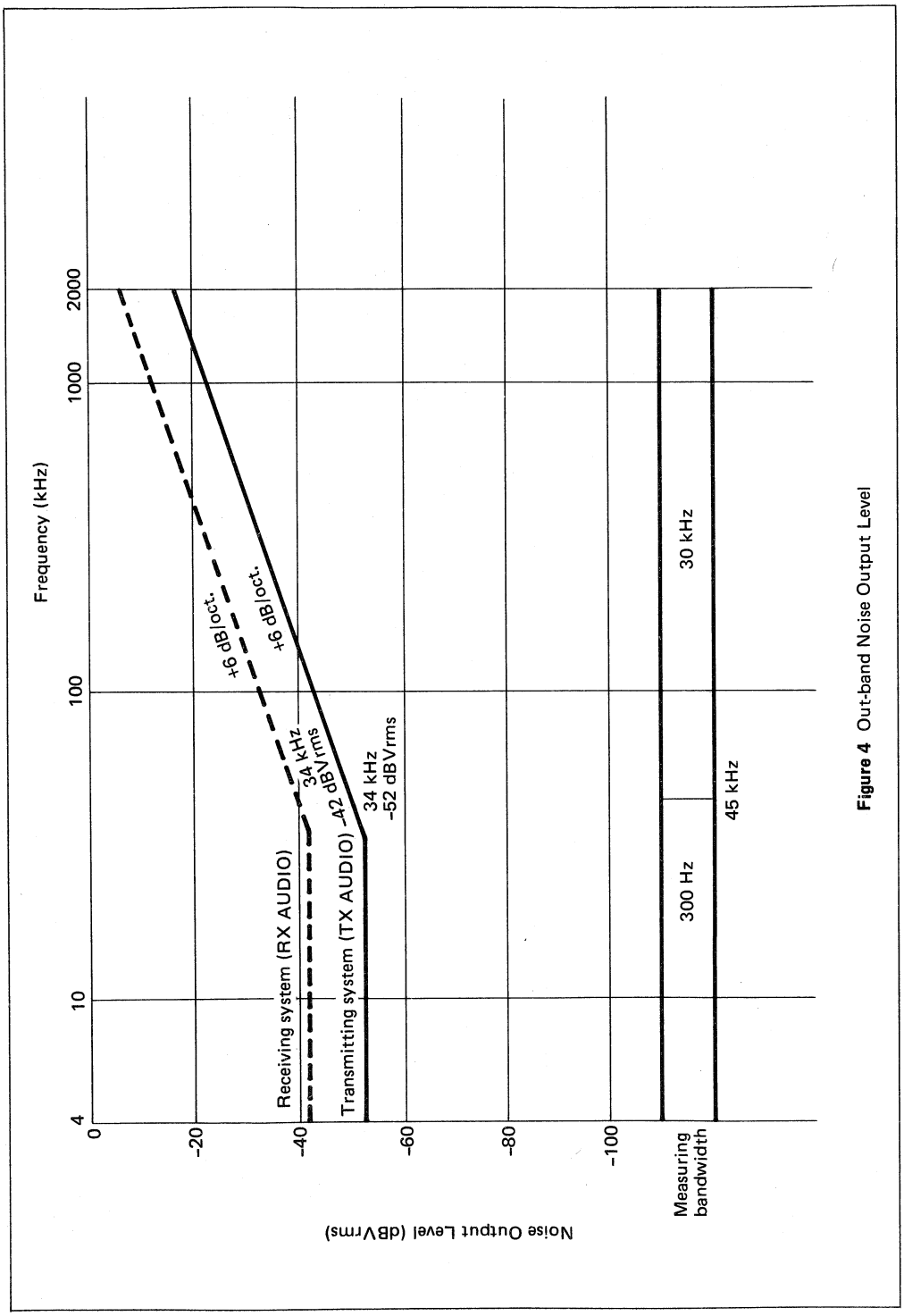


Figure 4 Out-band Noise Output Level

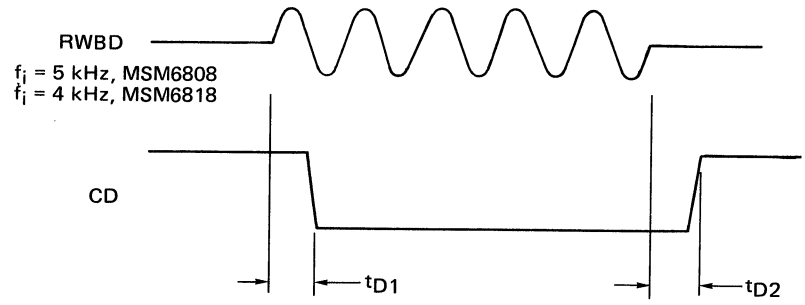
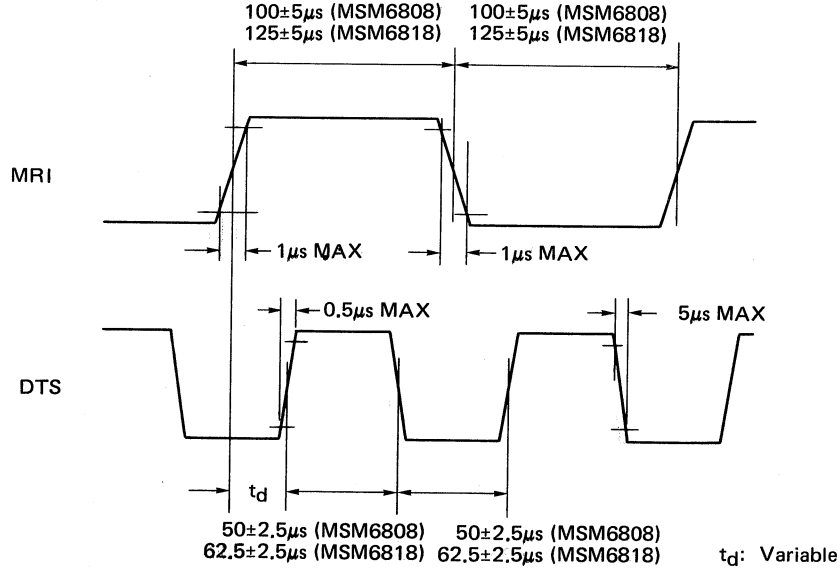


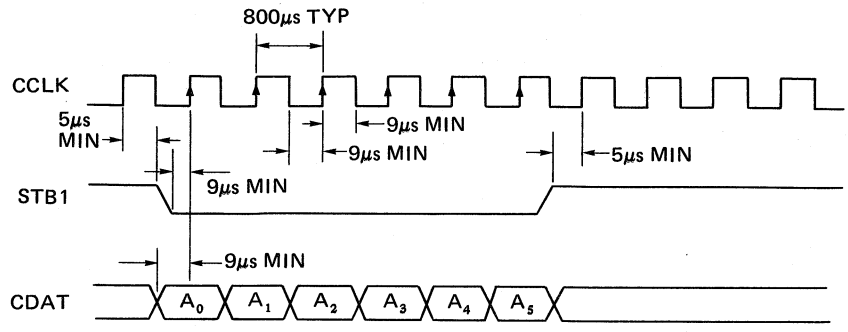
Figure 5 CD



f_i (RWBD) = 5 kHz (MSM6808)
f_i (RWBD) = 4 kHz (MSM6818)

Figure 6 MRI/DTS

CONTROL PIN SPECIFICATIONS



Note: The CCLK is edge triggered.

Symbol	Name	Switch Status
A_0	(DEMA, DEMB) (RSIA, RSIB) selection switch	
A_1	(DEMA, DEMB) (RSIA, RSIB) selection switch enable	

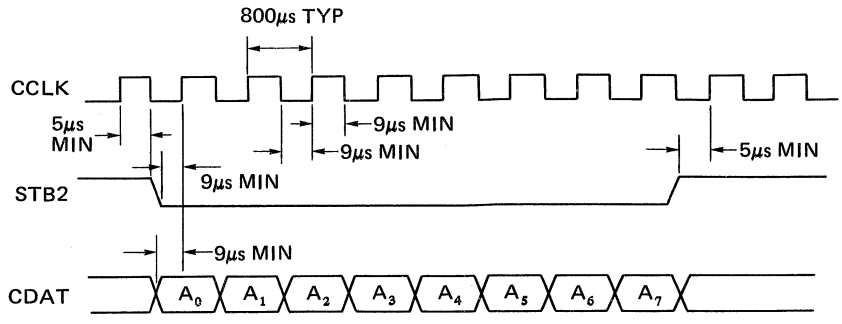
RSIC, RSID Input DC Level	Control Data A0	Control Data A1	Switch Status SW1	Switch Status SW2
RSIC > RSID	L	L	0	0
	L	H	1	1
	H	L	1	1
	H	H	1	1
RSIC < RSID	L	L	0	0
	L	H	0	0
	H	L	1	1
	H	H	0	0

Control data L: Logic Low Level
H: Logic High Level
Switch status "0", "1": Refer to the block diagram

A_2	Data transmission enable	H: SW3 = "1", L: SW3 = "0"
A_3	SAT transponder enable	H: SW4 = "1", L: SW4 = "0"
A_4	DTMF transmission enable	H: SW5 = "1", L: SW5 = "0"
A_5	Side tone enable	H: SW6 = "1", L: SW6 = "0"

See the block diagram

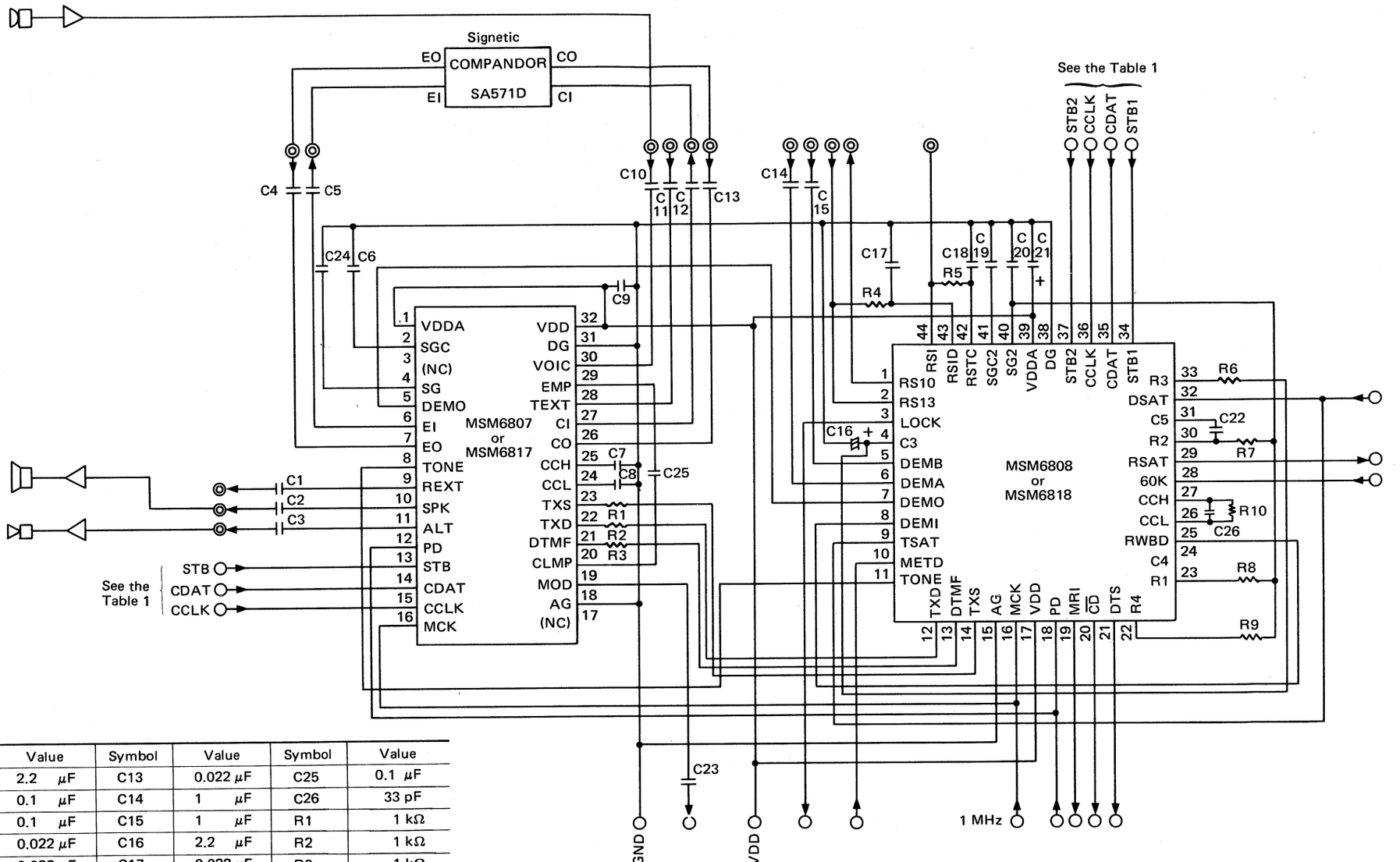
Table 1



The CCLK is edge triggered.

A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	Low Tone Frequency (Hz)	High Tone Frequency (Hz)	Remarks
0	0	0	x	x	x	x	x	697		
0	0	1	x	x	x	x	x	770		
0	1	0	x	x	x	x	x	852		
0	1	1	x	x	x	x	x	941		
1	0	0	x	x	x	x	x			
1	0	1	x	x	x	x	x			A_6 = H: Low tone on
1	1	0	x	x	x	x	x			L: Low tone off
1	1	1	x	x	x	x	x			
x	x	x	0	0	0	x	x		1209	A_7 = H: High tone on
x	x	x	0	0	1	x	x		1336	
x	x	x	0	1	0	x	x		1477	L: High tone on
x	x	x	0	1	1	x	x		1633	
x	x	x	1	0	0	x	x		2016	
x	x	x	1	0	1	x	x			
x	x	x	1	1	0	x	x			
x	x	x	1	1	1	x	x			

Table 2



Symbol	Value	Symbol	Value	Symbol	Value
C1	2.2 μF	C13	0.022 μF	C25	0.1 μF
C2	0.1 μF	C14	1 μF	C26	33 pF
C3	0.1 μF	C15	1 μF	R1	1 kΩ
C4	0.022 μF	C16	2.2 μF	R2	1 kΩ
C5	0.022 μF	C17	0.022 μF	R3	1 kΩ
C6	2.2 μF	C18	0.022 μF	R4	330 kΩ
C7	0.01 μF	C19	2.2 μF	R5	330 kΩ
C8	0.01 μF	C20	2.2 μF	R6	33 kΩ
C9	10 μF	C21	10 μF	R7	22 kΩ
C10	0.022 μF	C22	3300 pF	R8	175 kΩ
C11	0.022 μF	C23	1 μF	R9	10 Ω
C12	0.022 μF	C24	2.2 μF	R10	91 kΩ

Figure 7 Application Circuit

MSM74017

MODULATOR/DEMODULATOR FOR MODEM FUNCTION IN THE CELLULAR MOBILE PHONE

GENERAL DESCRIPTION

The MSM74017 performs the modulator/demodulator functions in the modem part of the cellular mobile phone.

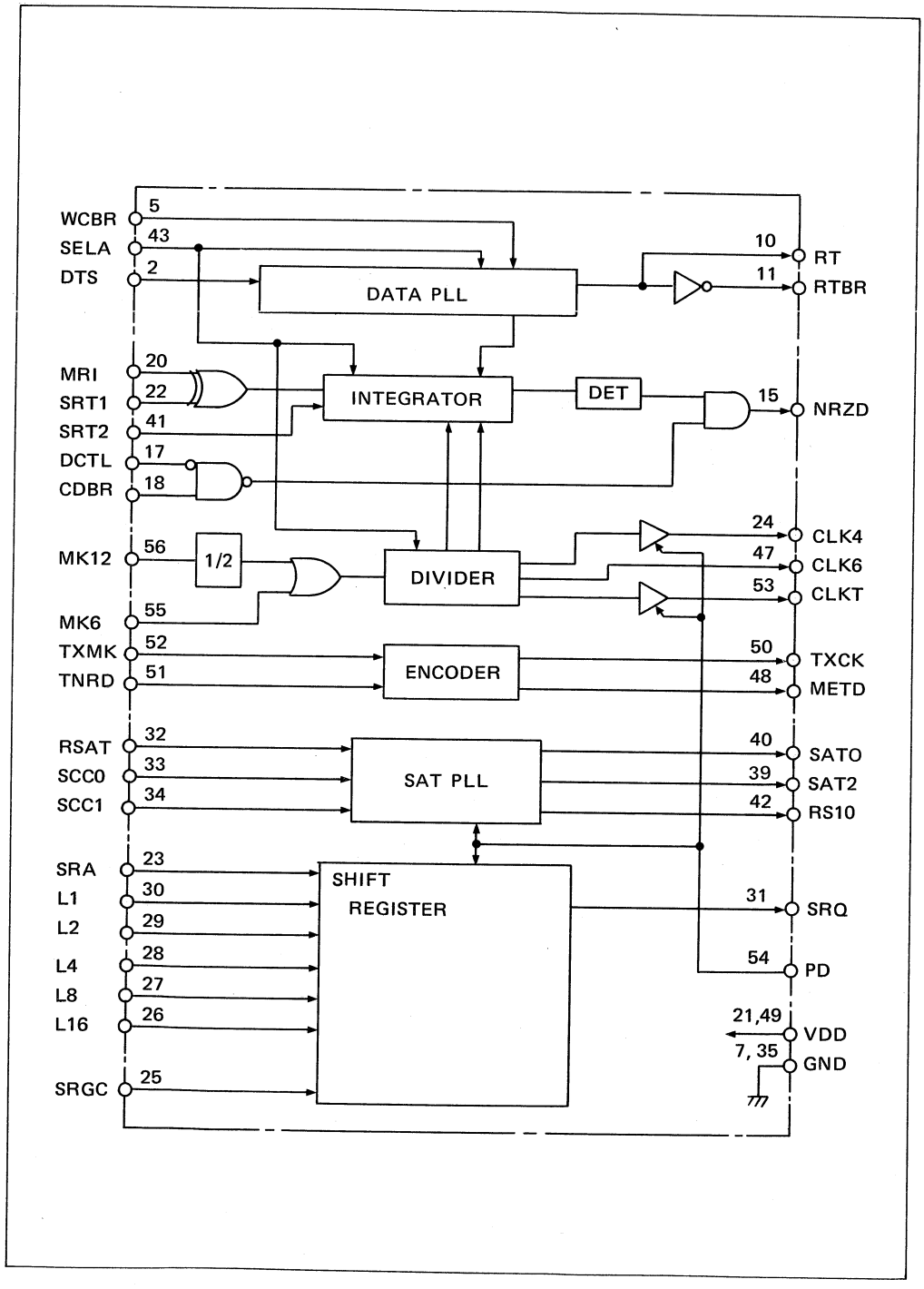
The MSM74017 consists of digital PLL for Data Timing Signal (DTS), Received Audio Tone (RSAT) and shift register and is fabricated by OKI's low power consumption CMOS silicon gate technology.

The MSM74017 can configurate a 10K bps SPL modem for AMPS system in combination with MSM6808. A 8K bps SPL modem for TACS system can be configurated in combination with MSM6818.

FEATURES

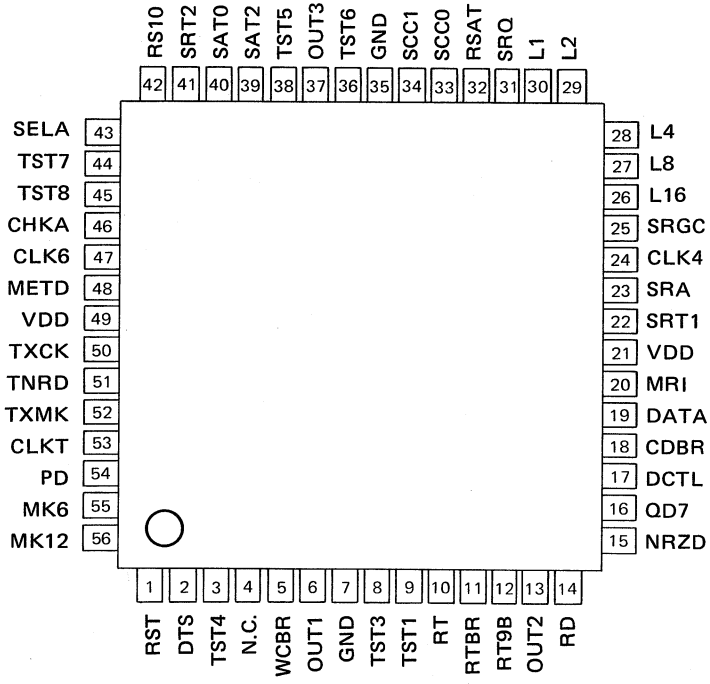
- Built-in DATA PLL to derive a phase from DTS.
- Built-in SAT PLL to derive a phase from RSAT.
- Built-in Detector for MRI demodulation.
- Built-in Manchester Encoder.
- TTL compatible digital interface.
- Low power consumption: 20 mW (typ).
- 56-pin plastic package.

BLOCK DIAGRAM



PIN CONFIGURATION

MSM74017GS-VK



56 pin FLAT package

III

PIN DESCRIPTION

Pin Name	Pin No.	I/O	Function
DTS	2	I	This is a Data Timing Signal input from MSM6808/6818. The input signal is output as the Received Timing (RT), after the S/N has been improved by a built-in Digital PLL.
WCBR	5	I	This input controls the bandwidth of the Digital PLL for Received Timing. WCBR = "1": narrow band width WCBR = "0": wide band width
RT	10	O	Received Timing Signal. When DTS is nearly equal to 10 kHz (AMPS) or 8 kHz (TACS), RT harmonizes with DTS. Refer to the description of DTS.
RTBR	11	O	This pin is the inverting output of RT, and is connected to SRT1 and SRT2 for demodulation clock.
NRZD	15	O	Manchester Received Input Signal (MRI) is demodulated by RTBR and is output as Non Return Zero Data (NRZD). See Figure 1.
DCTL	17	I	This pin controls the output of NRZD. Refer to the description about CDBR.
CDBR	18	I	This signal is Carrier Detection Data which is detected in MSM6808/6818. CDBR controls the output of NRZD with DCTL.
MRI	20	I	Manchester Received Input Signal. See Figure 1.
SRT1	22	I	This pin should be connected to RTBR. RTBR is used for Demodulation Clock.
SRA	23	I	Shift Register Data input. This shift register is a static clock serial shift register whose length may be programmed to be any number of bits between 1 and 32.
CLK4	24	O	This is a clock output, the frequency of which, is 1.5 MHz devided from MK6 or MK12. This may be used for Shift Register Clock.

DCTL	CDBR	NRZD
0	0	NRZD
0	1	0
1	0	NRZD
1	1	NRZD

<table>
<tr><th>Pin Name</th><th>Pin No.</th><th>I/O</th><th>Function</th></tr>
<tr><td>SRGC</td><td>25</td><td>I</td><td>Shift Register Clock input.</td></tr>
<tr><td>L16</td><td>26</td><td>I</td><td rowspan="5">Length Control inputs. The number of selected bit is equal to the sum of the subscripts of these enabled inputs plus one.</td></tr>
<tr><td>L8</td><td>27</td><td>I</td></tr>
<tr><td>L4</td><td>28</td><td>I</td></tr>
<tr><td>L2</td><td>29</td><td>I</td></tr>
<tr><td>L1</td><td>30</td><td>I</td></tr>
<tr><td>SRQ</td><td>31</td><td>O</td><td>Shift Register Output.</td></tr>
<tr><td>RSAT</td><td>32</td><td>I</td><td>Received Supervisory Audio Tone.
This pin should be connected to RSAT of MSM6808/6818. The signal is input into a buld-in Digital PLL for SAT so that the S/N is improved, and is output as SATO, SAT2, RS10.</td></tr>
<tr><td>SCC0</td><td>33</td><td>I</td><td rowspan="2">SCC0 and SCC1 are SAT Color Code.
These signals determine the center frequency of the Digital PLL for SAT.
<table><tr><th>SCC1</th><th>SCC0</th><th>Center Frequency</th></tr><tr><td>0</td><td>0</td><td>5970 Hz</td></tr><tr><td>0</td><td>1</td><td>6000 Hz</td></tr><tr><td>1</td><td>0</td><td>6030 Hz</td></tr><tr><td>1</td><td>1</td><td>—</td></tr></table></td></tr>
<tr><td>SCC1</td><td>34</td><td>I</td></tr>
<tr><td>SAT2</td><td>39</td><td>I</td><td>The double frequency of SAT Signal is output.
This may be used for discrimination of SAT frequencies. Refer to the description about RSAT.</td></tr>
<tr><td>SATO</td><td>40</td><td>I</td><td>This is an output for transmitting SAT signal.
Before this signal is input into DSAT of MSM6808/6818, the phase of the signal may be delayed by build-in Shift Register.</td></tr>
<tr><td>SRT2</td><td>41</td><td>I</td><td>This pin should be tied to RTBR. SRT1 is used for the Demodulation Clock, same as SRT2.</td></tr>
<tr><td>RS10</td><td>42</td><td>O</td><td>The output is ten times of the frequency of RSAT signal.
When this signal is input to MSM6808/6818, it controls the center frequency of SAT and BPF to fit to RSAT signal.</td></tr>
</table>

Pin Name	Pin No.	I/O	Function
SELA	43	I	This pin is used for selecting the center frequency of built-in Digital PLL for DTS and used for selecting Transmitting Data Rate. SELA = "1": 10 kHz (AMPS) SELA = "0": 8 kHz (TACS)
METD	48	O	Manchester Encoded Data output. See Figure 2.
TXCK	50	O	This is a clock output using for Transmitting Data. Refer to the description of SELA and Figure 2.
TNRD	51	I	Transmit NRZ Data. This input signale is modulated by an internal TXCK and is output as METD. See Figure 2.
TXMK	52	I	This pin should be connected to CLKT.
CLKT	53	O	The double frequency of TXCK is output. CLKT should be connected with TXMK.
PD	54	I	Power down function enable pin. Logical "0" enables the power down mode.
MK6	55	I	Main Clock Input. One of MK6 and MK12 should be input. When this pin is not used, it should be set to digital "0".
MK12	56	I	Main Clock Input. See the description of MK6. When this pin is not used, it should be set at digital "0".
GND	7		Ground level: 0 V
	35		
VDD	21		Power Supply: +5V
	49		
RST	1	I	These pins are used for various tests. These pins should be usually connected to GND.
TST4	3	I	
TST3	8	I	
TST1	9	I	
TST6	36	I	
TST5	38	I	

Pin Name	Pin No.	I/O	Function
TST7	44	I	These pins are used for various tests. These pins should be usually connected to GND.
TST8	45	I	
OUT1	6	O	These pins are output pins for test.
RT9B	12	O	
OUT2	13	O	
RD	14	O	
QD7	16	O	
DATA	19	O	
OUT3	37	O	
CHKA	46	O	

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATING

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Power Supply Voltage	V_{DD}	T_a = 25°C	-0.5	–	+7	V
Input/Output Voltage	V_I, V_O	with reset to GND	-0.5	–	V_{DD}+0.5	V
Input/Output Current	I_I, I_O	T_a = 25°C	-10	–	+10	mA
Storage Temperature	T_{st}	–	-55	–	+150	°C
Power Dissipation	Pd	–	–	1	–	W

OPERATING RANGE

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	V_{DD}	3	–	6	V
Operating Temperature	T_{opr}	-40	–	85	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{DD}	4.25	5	5.25	V
Operating Temperature	T_{opr}	-40	25	85	°C
"1" Input Voltage	V_{IH}	2.2	–	V_{DD}+0.3	V
"0" Input Voltage	V_{IL}	-0.3	–	0.8	V

MASTER CLOCK

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Frequency	Fi	MK6 = 6 MHz or MK12 = 12 MHz	-0.01	0	+0.01	%
Duty Ratio	Fd	MK6 = 6 MHz	45	50	55	%
		MK12 = 12 MHz	20	50	80	

DC CHARACTERISTICS

(V_{DD} = 5V + 5%, T_a = -40 +85°C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
"1" Input Current	I_{IH}	$V_i = V_{DD}$ V_{DD} = 5.25 V	—	—	10	μA
"0" Input Current	I_{IL}	V_i = GND	-10	—	—	
"1" Output Voltage	V_{OH}	I_o = -40 μA V_{DD} = 4.75 V I_o = -400 μA	4.2 2.4	— —	— —	V
"0" Output Voltage	V_{OL}	I_o = 2 mA (*1) I_o = 5 mA	— —	— —	0.4 0.5	V
Standby Current	I_{CCS}	$V_i = V_{DD}$/GND V_{DD} = 5.25 V	—	1	0.5	mA
Operation Power Supply Cullent	I_{CCO}	$V_i = V_{DD}$/GND Output pin open	—	4	6	mA

(*1) V_{OH}: upper/CMOS4000
lower/TTL74, 74LS

V_{OL}: upper/CMOS4000, TTL74LS
lower/TTL74

III

AC CHARACTERISTICS

(V_{DD} = 5V +5%, T_a = -40 +85°C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Output Frequency	RT	f RT1 DTS = 10 kHz, SELA = "1" f RT0 DTS = 8 kHz, SELA = "0"	— —	10 8	— —	kHz
	RTBR	f RTBR1 DTS = 10 kHz, SELA = "1" f RTBR0 DTS = 8 kHz, SELA = "0"	— —	10 8	— —	kHz
	RS10 SAT2 SATO CLK4 CLK6	f RS10 RSAT = 6 kHz	—	60	—	kHz
		f SAT2 f SATO SCC0 = "1", SCC = "0"	— —	12 6	— —	kHz
		f CLK4 f CLK6	— —	1.5 1	— —	MHz
	CLKT	f CLKT1 SELA = "1" SELA = "0"	— —	20 16	— —	kHz
	TXCK	f TXCK TXMK = 20 kHz TXMK = 16 kHz	— —	10 8	— —	kHz
PLL Capture Range	DTS-RT	f LDN1 f HDN1 SELA = "1", WCBR = "1"	9.993	—	10.007	kHz
		f LDW1 f HDW1 SELA = "1", WCBR = "0"	9.939	—	10.061	kHz
		f LDN0 f HDN0 SELA = "0", WCBR = "1"	7.993	—	8.007	kHz
		f LDW0 f HDW0 SELA = "0", WCBR = "0"	7.961	—	8.040	kHz
		f LS0 f HS0 SCC0= SCC1 = "0"	5952.4	—	5988.0	Hz
	RSAT-STO	f LS1 f HS1 SCC0 = "1", SCC1 = "0"	5982.1	—	6018.1	Hz
		f LS2 f HS2 SCC0 = "0", SCC1 = "1"	6012.0	—	6048.4	Hz

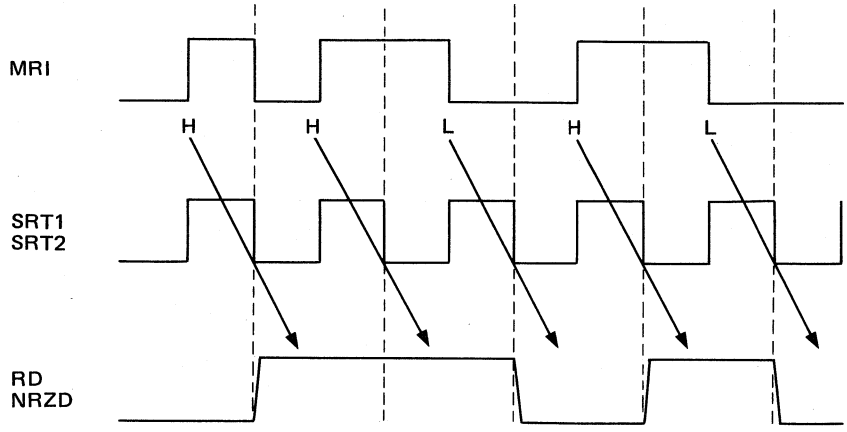


Figure 1 MRI – NRZD Timing Chart

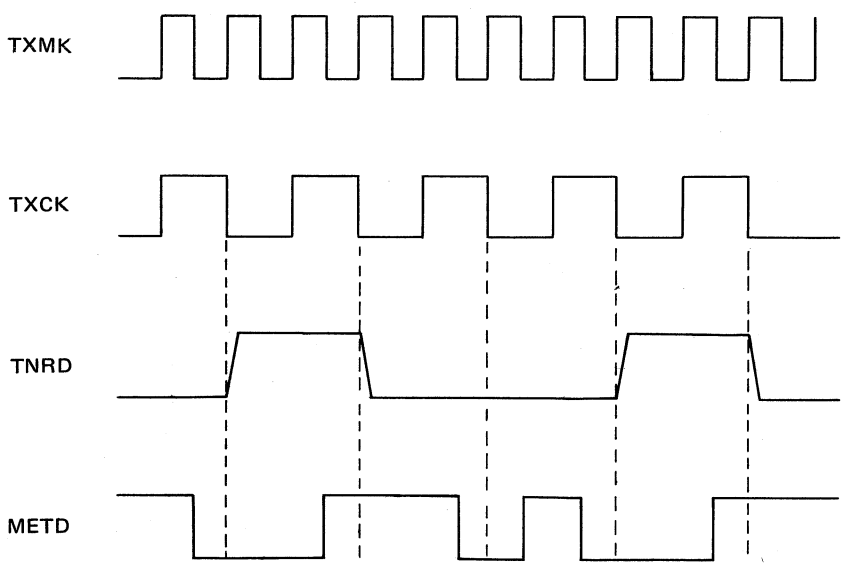
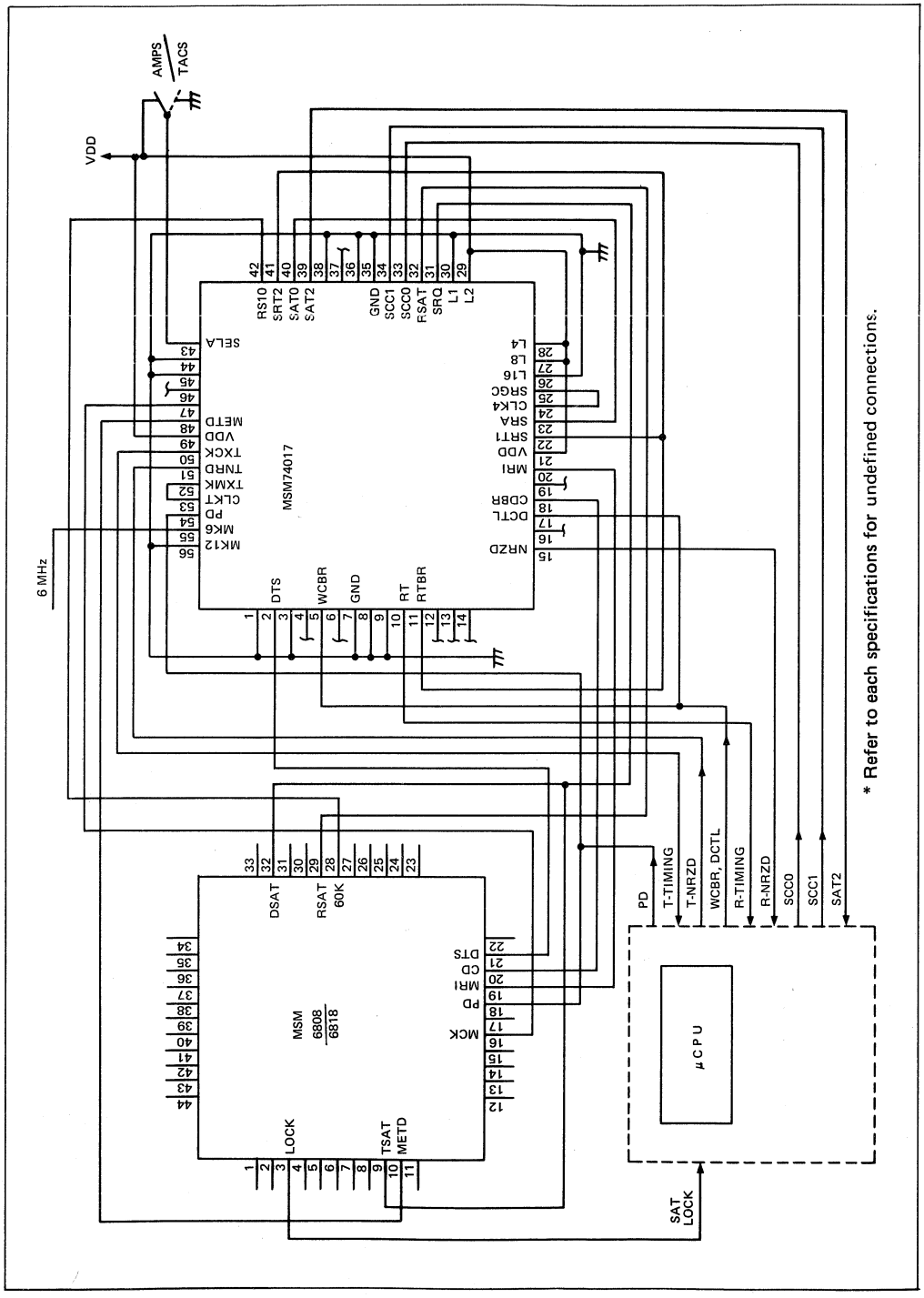


Figure 2 METD Timing Chart

APPLICATION CIRCUIT



MSM6960

PLL FREQUENCY SYNTHESIZER LSI

GENERAL DESCRIPTION

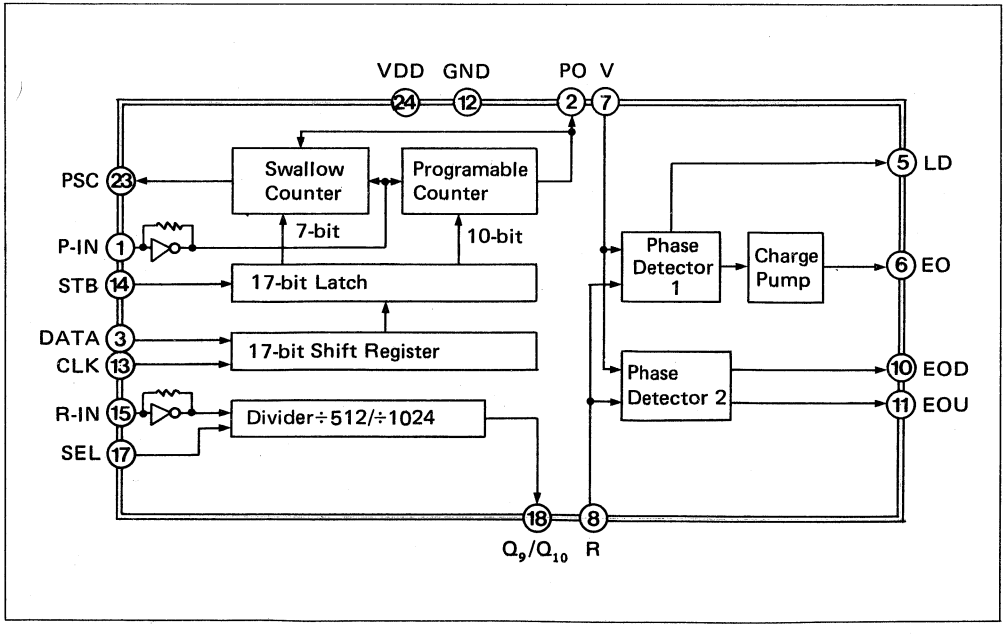
The MSM6960 is a PLL frequency synthesizer LSI which is fabricated by OKI's low power consumption CMOS silicon gate technology. The MSM6960 consists of a 10-bit programmable counter, 7-bit swallow counter, a reference frequency divider, phase detectors and charge pump.

The MSM6960 can be combined with a 1 GHz band prescaler to configurate a directly divided frequency synthesizer.

FEATURES

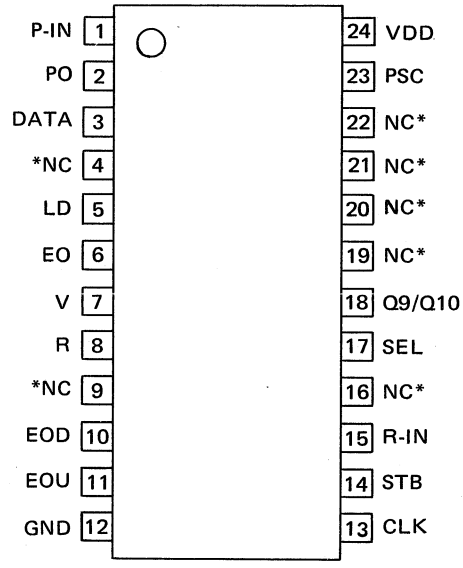
- Frequency synthesizer operating on a pulse swallow method.
- Built-in reference frequency division factor selector.
- Serial interface counter data.
- Two types of phase comparator output: Tristate (EO) and double end (EOU, EOD).
- Unlocked phase detection output.
- 24-pin mini-mold flat package.

BLOCK DIAGRAM



PIN CONFIGURATION

(Top View) 24 lead plastic flat



*NC: Left unconnected.

III

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Power Supply Voltage	V_{DD}	T_a = +25°C	-0.3	–	+7	V
Input Voltage	V_{IN}	T_a = +25°C	-0.5	–	V_{DD}+0.5	V
Output Voltage	V_{OUT}	T_a = +25°C	-0.5	–	V_{DD}+0.5	V
Operating Temperature	T_{OP}	–	-40	–	+85	°C
Storage Temperature	T_{STG}	–	-55	–	+150	°C
Output Voltage	V_{OUT}	EOD T_a = +25°C	-0.5	–	V_{DD}+3	V

RECOMMENDED OPERATING CONDITIONS

(V_{DD} = 5V ±10%, T_a = -40 ~ +85°C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input Rise Time	tir	STB, DATA, CLK, V, R, SEL	–	20	500	ns
Input Fall Time	tif	STB, DATA, CLK, V, R, SEL	–	20	500	ns

DC CHARACTERISTICS

(V_{DD} = 5V ±10%, T_a = -40 ~ +85°C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Low-level Input Voltage	V_{IL}	STB, DATA, CLK, V, R, SEL	–	–	0.3xV_{DD}	V
High-level Input Voltage	V_{IH}	STB, DATA, CLK, V, R, SEL	0.7xV_{DD}	–	–	V
Low-level Ouput Voltage	V_{OL}	I_{OL} = 3 mA	–	0.2	0.4	V
High-level Output Voltage	V_{OH}	I_{OH} = -1 mA	4.0	4.9	–	V
Input Leak Current	I_{Li}	R-IN, P-IN	–	±7	±40	μA
Output Leak Current	I_{LO}	EO	–	±0.05	±1	μA

AC CHARACTERISTICS

(V_{DD} = 5V ±10%, T_a = -40 ~ +85°C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Maximum Operating Frequency	fin (R)	R-IN Vin = 1 Vp-p sine wave	16	130	–	MHz
	fin (P)	P-IN Vin = 1 Vp-p sine wave	10	45	–	MHz
Output Delay Time	tpd	P-IN → PSC C_L = 20 pF	–	12	80	ns
Supply Current	I_{DD}	R-IN = 16 MHz, 1 Vp-p P-IN = 10 MHz, 1 Vp-p	–	4	10	mA
Input Amplitude	Vin	R-IN, P-IN	1.0	–	V_{DD}	Vp-p

PIN DESCRIPTION

Pin Name	Pin No.	Function
P-IN	1	Programmable divider input pin.
PO	2	Programmable divider output pin.
DATA	3	17-bit shift register data input pin.
LD	5	Unlocked phase detection pin (lock detector); high when locked, pulse output when unlocked.
EO	6	Phase detector output (tristate).
V	7	Phase detector variable input; connected to PO when the LPF is of inverted type.
R	8	Phase detector reference input; a reference signal is input when the LPF is of inverted type.
EOD	10	Phase detector output (for external charge pump installation), N-ch open drain.
EOU	11	Phase detector output (for external charge pump installation, CMOS output.
GND	12	System ground.
CLK	13	17-bit shift register clock input pin.
STB	14	17-bit latch strobe input pin to specify the N-value.
R-IN	15	Reference frequency divider input.
SEL	17	Reference frequency division factor selector; division by 1,024 when high, division by 512 when low.
Q9/Q10	18	Reference frequency divider output.
PSC	23	Prescaler control output; high:÷P, Lo:÷(P+1)
VDD	24	Power supply pin (+5V)

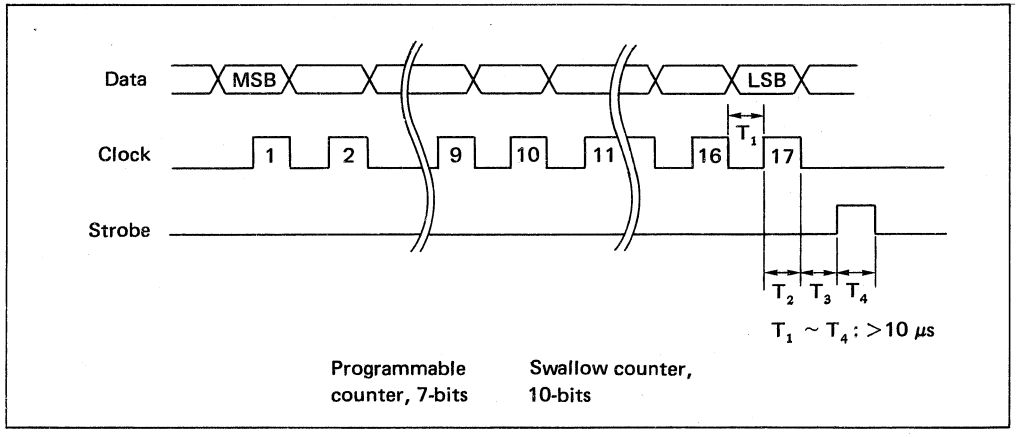
APPLICATION NOTE

Data Input Method:

As the N-value for the programmable divider, 17-bit binary data is input to the shift register, starting with the most significant bit (MSB), which is finally latched by a strobe signal.

The input data has positive logic. It is shifted on the leading edge of each clock pulse, is through when the strobe goes high, is latched on its trailing edge, and is held when it goes low. With the prescaler being set to ÷128/÷129 (7-bit), the input data is directly acceptable if the total N-value is converted to binary. With a lower divider ratio, such as ÷64/÷65 or ÷32/÷33, the addition of dummy bytes is necessary.

Input Timing



III

Dummy Bit Handling: $N_{16} \sim N_0$ represent a calculated N-value (N_{16}: MSB). $D_{16} \sim D_0$ represent input data (D_{16}: MSB) to the MSM6960.

÷128/÷129 (No dummy bits are required.)

N_{16} N_{15} N_{14} N_{13} N_{12} N_{11} N_{10} N_9 N_8 N_7 N_6 N_5 N_4 N_3 N_2 N_1 N_0

↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓

D_{16} D_{15} D_{14} D_{13} D_{12} D_{11} D_{10} D_9 D_8 D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0

÷64/÷65 (One dummy bits are required.)

N_{15} N_{14} N_{13} N_{12} N_{11} N_{10} N_9 N_8 N_7 N_6 N_5 N_4 N_3 N_2 N_1 N_0

↓ ↓ ↓ ↓ ↓ ↓

D_{16} D_{15} D_{14} D_{13} D_{12} D_{11} D_{10} D_9 D_8 D_7 [D_6] D_5 D_4 D_3 D_2 D_1 D_0

↑ Insert dummy bit 0.

÷32/÷33 (Two dummy bits are required.)

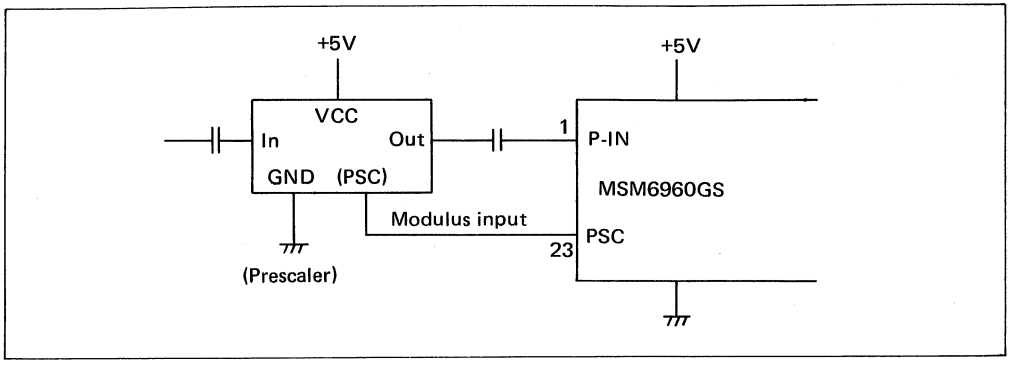
– N_{14} N_{13} N_{12} N_{11} N_{10} N_9 N_8 N_7 N_6 N_5 N_4 N_3 N_2 N_1 N_0

↓ ↓ ↓ ↓ ↓

D_{16} D_{15} D_{14} D_{13} D_{12} D_{11} D_{10} D_9 D_8 D_7 [D_6 | D_5] D_4 D_3 D_2 D_1 D_0

↑ Insert dummy bit 0.

Prescaler Connection



- The prescaler output and the programmable divider input (pin 1) are connected to each other by cutting the current flow with a capacitor.
- Connect the prescaler modulus input pin and the MSM6960GS PSC output pin directly to each other, as they require DC coupling.

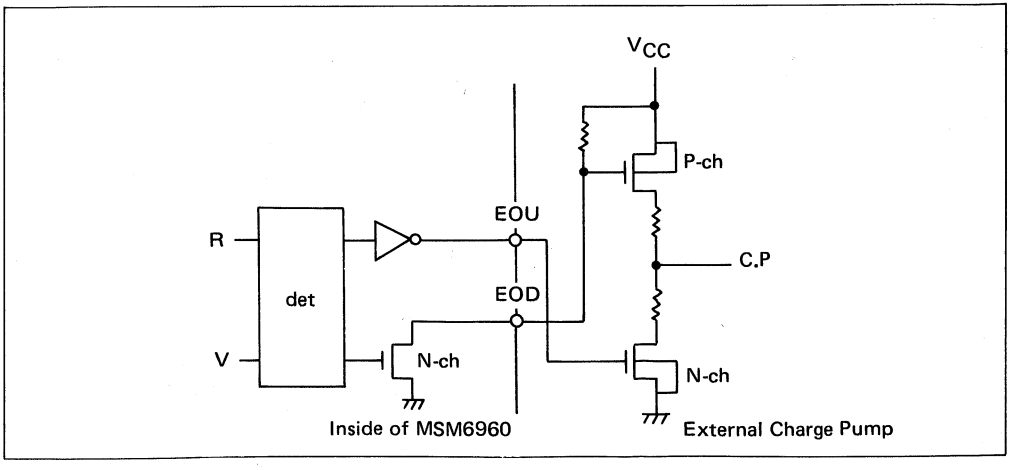
PLL Polarity

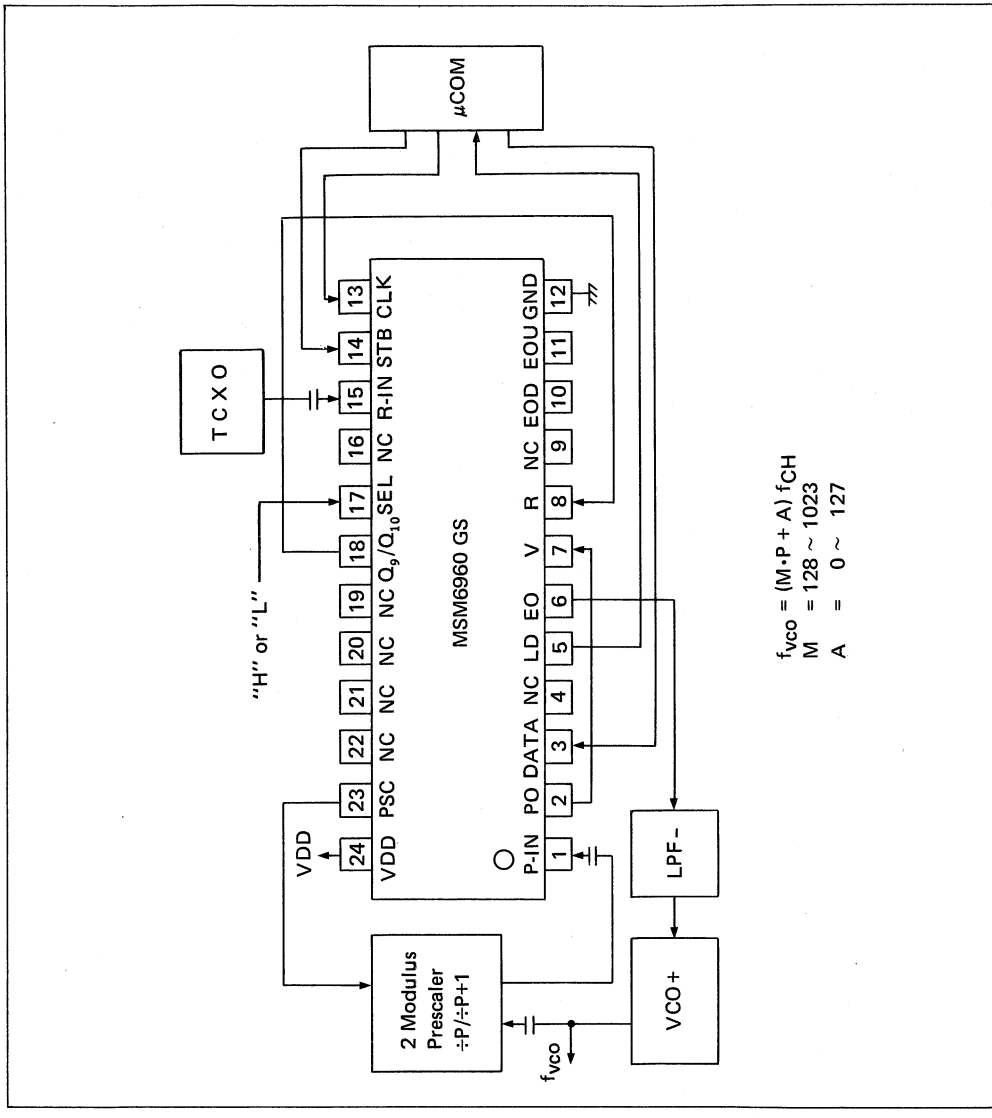
- With an inverted low-pass filter LPF, connect phase detector input R (pin 8) to the reference signal and V (pin 7) to the programmable divider output if a mixer with a higher level of local oscillation than VCO is not available in the PLL loop or if direct division is desired.
- With a non-inverted LPF (such as a passive filter), interchange the R and V connections.

III

External Charge Pump Installation

- CMOS output (pin 11) and N-ch open drain (pin 10) are available to allow external installation of a charge pump.
- The charge pump supply voltage can be raised 3V above MSM6960GS V_{DD}.
- An example of a circuit setup in which an external charge pump is configured by using P-ch and N-ch transistors (enhancement type) is shown at as follow.





AVAILABLE SYSTEM FREQUENCY

Channel Spacing f_{CH}	TCXO Frequency	Ref. Divider SEL Input	VCO Frequency Range	
			Prescaler P / P + 1	
			÷ 128 / ÷ 129	÷ 64 / ÷ 65
30 KHz System	15.36 MHz	L	491.520 ~ 1300 MHz	122.880 ~ 640 MHz
25 KHz System	12.8 MHz	L	409.600 ~ 1300 MHz	102.400 ~ 640 MHz
12.5 KHz System	12.8 MHz	H	204.800 ~ 1300 MHz	51.200 ~ 640 MHz

G. OTHERS III

MSM6252

64 WORDS × 4-BITS FIRST IN FIRST OUT MEMORY

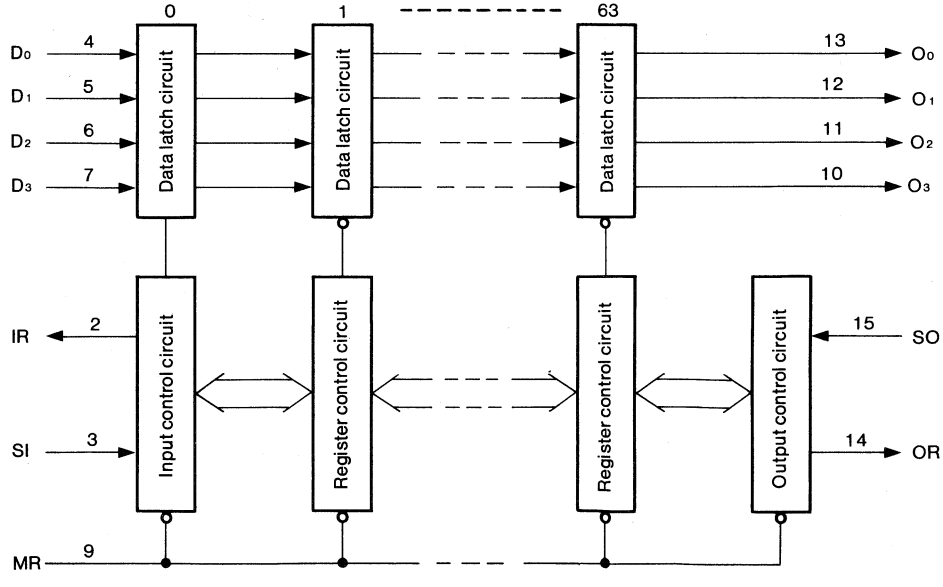
GENERAL DESCRIPTION

The MSM6252RS is a 64-word × 4-bit first-in first-out memory using silicon gate CMOS technology. This memory is compatible with Fairchild 3341 MOS FIFO.
Data input (shift in) and data output (shift out) operations may be executed asynchronously, and the memory can be easily extended in both bit and word directions.

FEATURES

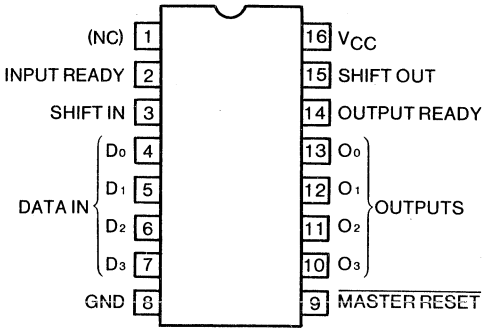
- Silicon gate CMOS technology
- 5V single power supply
- 6 MHz shift out/shift in rates
- Low power consumption (150 mW max. when operating at 6 MHz)
- Fairchild F3341 MOS FIFO compatibility (No data reset function)
- TTL compatible input/output
- 16-pin plastic DIP

CIRCUIT CONFIGURATION



(These specifications are subject to modification without prior notification.)

PIN CONFIGURATION



Pin No.	Symbol	Name	Pin No.	Symbol	Name
1	–	(N. C.)	9	$\overline{MR}$	$\overline{\text{MASTER RESET}}$
2	IR	INPUT READY	10	O_3	Data output
3	SI	SHIFT IN	11	O_2	Data output
4	D_0	Data input	12	O_1	Data output
5	D_1	Data input	13	O_0	Data output
6	D_2	Data input	14	OR	OUTPUT READY
7	D_3	Data input	15	SO	SHIFT OUT
8	GND	Power supply (0V)	16	V_{CC}	Power supply (5V)

An abbreviated format (M6252) is used to indicate the type name.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Ratings	Unit
Power Supply Voltage	V_{CC}	Respect to GND	−0.5 ~ +7.0	V
Input voltage	V_{IN}		−0.5 ~ V_{CC}+0.5	V
Output voltage	V_{OUT}		−0.5 ~ V_{CC}+0.5	V
Storage temperature	Tstg	–	−55 ~ +150	°C
Power dissipation	Pd	Ta = 25°C	0.8	W

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Operating temperature	V_{OP}	−40	+25	+85	°C
"L" input voltage	V_{IL}	−0.3	–	+0.8	V
"H" input voltage	V_{IH}	2.2	–	V_{CC}+0.3	V

DC Characteristics

(V_{CC} = 4.5V ~ 5.5V, Ta = −40°C ~ +85°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
"L" output voltage	V_{OL}	I_{OL} = 2mA	–	–	0.45	V
"H" output voltage	V_{OH}	I_{OH} = −400μA	2.4	–	–	V
		I_{OH} = −40μA	4.2	–	–	
Input leak current	I_{LI}	$0V \leqq V_{IN} \leqq V_{CC}$	−10	–	10	μA
Operating supply current	I_{CCO}	Load capacity CL= 0 when operating at 6 MHz	–	16	30	mA

AC Characteristics

(V_{CC} = 4.5V ~ 5.5V, Ta = −40°C ~ +85°C)

Parameter	Symbol	Figure No.	Min	Max	Unit
SI "H" time	t_{SIH}	1	30	–	ns
SI "L" time	t_{SIL}	1	120	–	ns
Data set-up time in respect to SI leading edge	t_{IDS}	1	10	–	ns
Data hold time in respect to SI leading edge	t_{IDH}	1	120	–	ns
SO "H" time	t_{SOH}	5	30	–	ns
SO "L" time	t_{SOL}	5	120	–	ns
$\overline{MR}$ pulse width	t_{MRW}	9	80	–	ns
Interval from $\overline{MR}$ leading edge to SI leading edge	t_{MRS}	9	80	–	ns
SI rate	f_{IN}	1	–	6	MHz
Delay time from SI leading edge to IR trailing edge	t_{IRL}	1	–	110	ns
Delay time from SI trailing edge to IR leading edge	t_{IRH}	1	–	120	ns
SO rate	f_{OUT}	5	–	6	MHz
Delay time from SO leading edge to OR trailing edge	t_{ORL}	5	–	110	ns
Delay time from SO trailing edge to OR leading edge	t_{ORH}	5	–	120	ns
Delay time from SO trailing edge up to next data output	t_{OD}	5	10	120	ns
Data throughput time (fall through time)	t_{PT}	3, 7	–	5	μs
Delay time from $\overline{MR}$ trailing edge to OR trailing edge	t_{MRORL}	9	–	100	ns
Delay time from $\overline{MR}$ trailing edge to IR leading edge	t_{MRIRH}	9	–	100	ns
IR "H" pulse width	t_{IPH}	3	18	–	ns
OR "H" pulse width	t_{OPH}	7	18	–	ns

Note: Load during measurement is CL = 20pF

DESCRIPTION OF OPERATION

Data input

The data input pins are D_0 thru D_3. When Input Ready (IR) is "H", the first word (word 0) is ready to accept data.

Data then present at the data inputs is entered into the first word when the SHIFT IN (SI) is brought "H". This causes IR to go "L". That data remains in word 0 until SI is brought "L", and IR is kept at "L". If no data is stored in word 1, and SI is brought "L", the word 0 data is transferred to word 1 and IR will go "H" indicating that the device is ready to accept new data.

If the FIFO is full, IR is kept at "L".

Data transfer

Once data is entered into the word 1, the transfer of any full word to the adjacent (preceding) empty word is automatic, activated by an internal FIFO control.

That is, while an empty word exists, data is filled up sequentially on the FIFO output side.

t_{PT} defines the time required for the first data to travel from the input to the output of a previously empty device.

Data output

The data output pins are Q_0 thru Q_3. When data is shifted through to word 63, OUTPUT READY (OR) goes "H", indicating the presence of valid data. When SHIFT OUT (SO) is brought "H", OR goes "L", and O_0 thru O_3 maintains the previous data.

When SO is brought "L", new data (stored in word 62) is shifted into word 63, then OUTPUT to Q_0 thru Q_3, and OR goes "H".

If the FIFO is empty, OR is kept at "L", and Q_0 thru Q_3 are kept at the previous status.

IR and OR may also be used as status signals indicating that the FIFO is completely full (IR stays "L" for at least t_{PT}) or completely empty (OR stays "L" for at least t_{PT}).

Master reset

When Master Reset ($\overline{MR}$) goes "L", the control logic is cleared. When $\overline{MR}$ returns "H", OR is kept at "L" and IR is kept at "H" if SI is "L". Since output data (Q_0 thru Q_3) is unaffected by $\overline{MR}$, data on Q_0 thru Q_3 should be considered valid only while OR is "H".

TIMING CHARTS

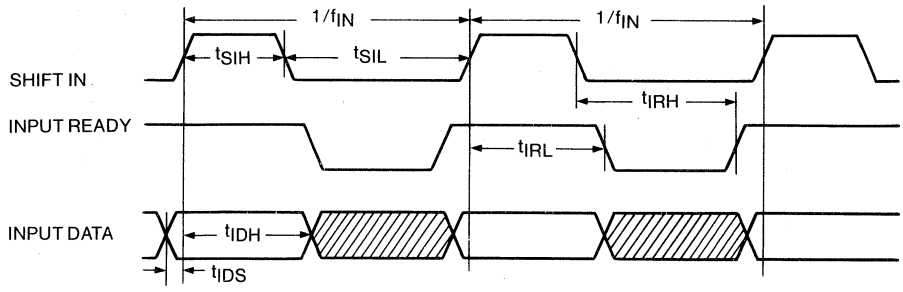


Fig. 1 Input timing

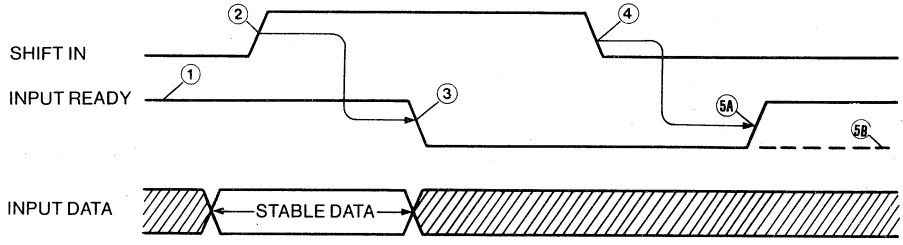


Fig. 2 Input timing descripion diagram

① IR at "H" level indicates that data can be stored by the SI pulse.
② Data is stored in the first word.
③ First word is full.
④ Data is transferred from first to second word.
⑤A First word reverted to ready status since data has been transferred from first to second word.
⑤B IR remains at "L" since second word is full.

Note: SI pulse is disregarded while IR is "L". (See Figure 4.)

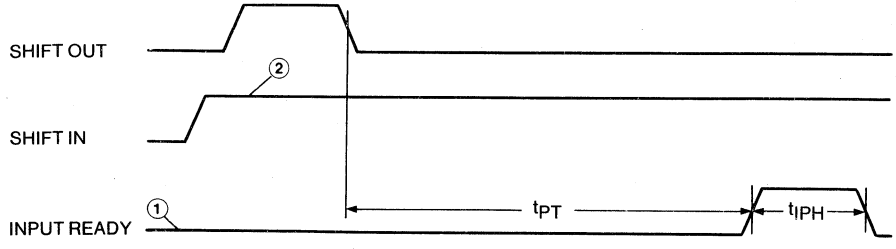


Fig. 3 t_{PT} and t_{IPH} specifications

① FIFO is already full.
② SI is kept at "H".

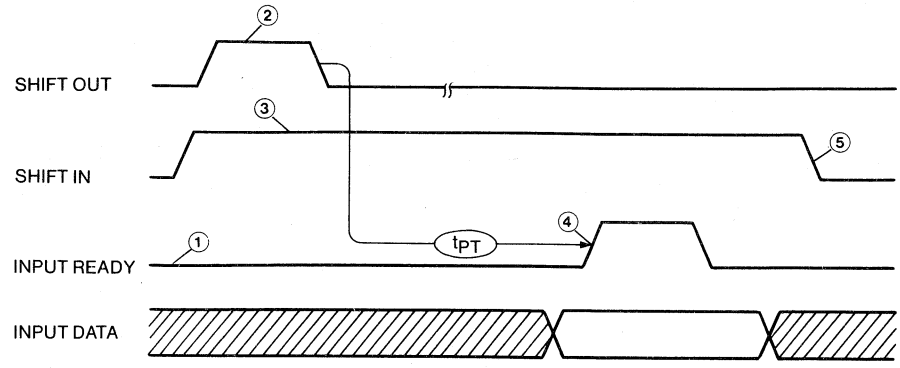


Fig. 4 Operation when SI and IR are both "H"

① FIFO is already full.
② Vacancy is formed in the FIFO due to output of last word data by SO pulse.
③ SI is kept at "H".
④ INPUT DATA is entered into first word immediately when IR goes "H".
⑤ First word data is transferred to second word when SI is brought "L".

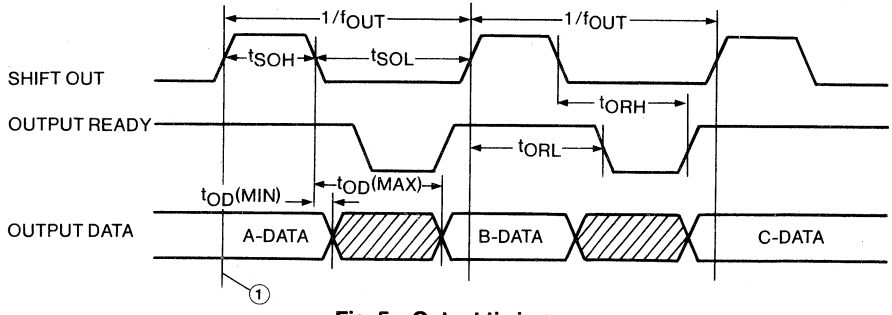


Fig. 5 Output timing

① The A-, B-, and C-DATA data denotes the data in words 63, 62, and 61 in this timing.

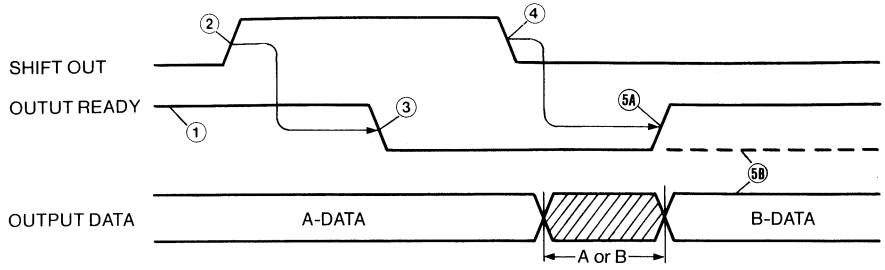


Fig. 6 Output timing description diagram

① SO at "H" level indicates that data output is possible by SO pulse.
② Proceed to next step when SI becomes "H".
③ OR goes "L".
④ Word 62 data (B) is transferred to word 63.
⑤A OR goes "H", and new data (B) is output by the FIFO.
⑤B If only a single item of data is stored in the FIFO, OR remains at "L", and no change occurs in the output (A-data).

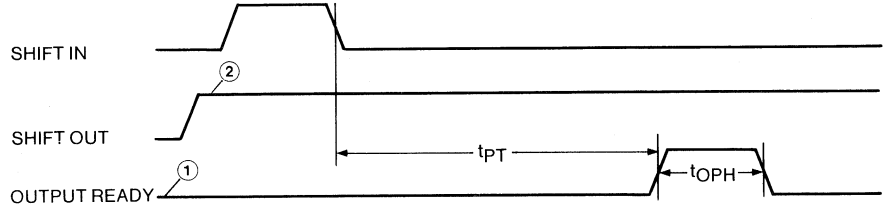


Fig. 7 t_{PT} and t_{OPH} specifications

① FIFO is already empty.
② SO is kept at "H".

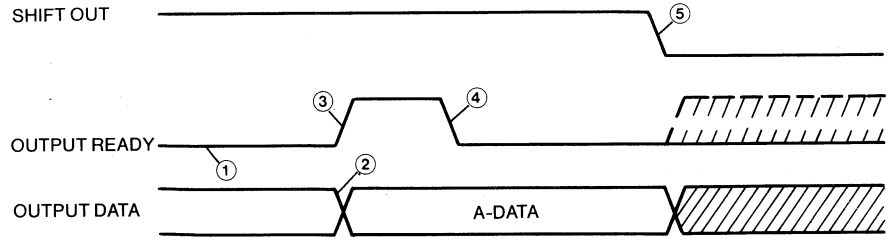


Fig. 8 Operation when SO and OR are both "H"

① Word 63 is empty.
② New data (A) reaches the output (word 63).
③ OR goes "H" to indicate that new data has arrived.
④ OR goes "L" immediately if SO remains at "H".
⑤ When OR goes "L", the output is changed immediately by the status of the OR dash line.

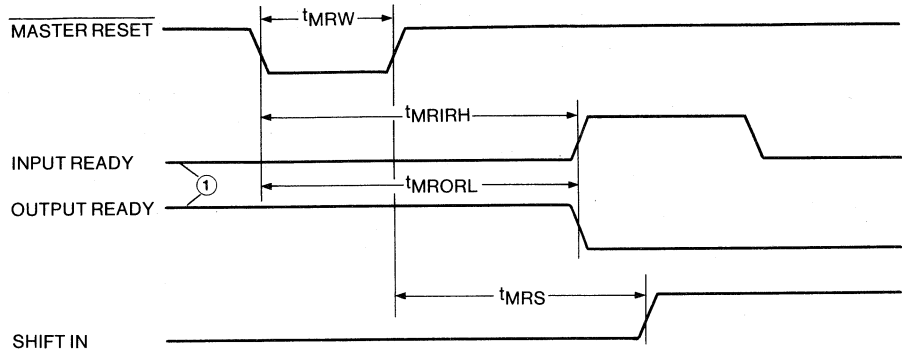
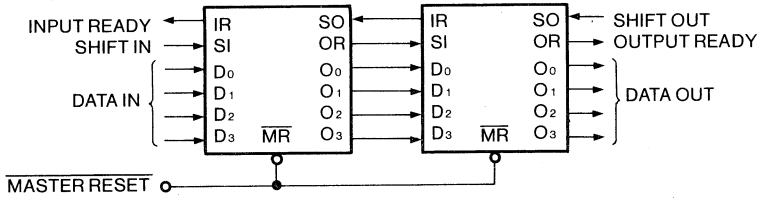


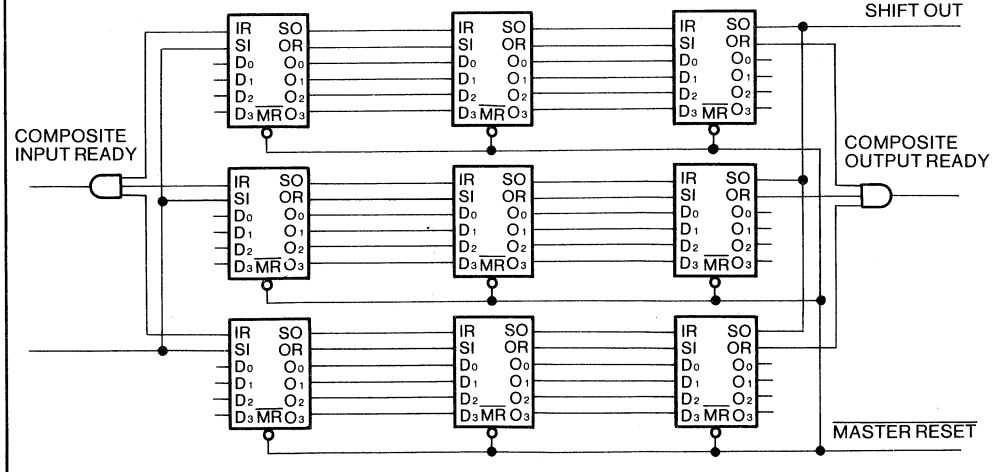
Fig. 9 Master reset timing

① FIFO is full.

CIRCUIT EXAMPLES (FIFO EXPANSION)



128 × 4 FIFO configuration example



192 × 12 FIFO configuration example

Note: The SO ← IR and OR → SI line capacitance should be less than 20pF.

MSM6920RS/6945RS

SINGLE CHIP DTMF DECODER

GENERAL DESCRIPTION

The MSM6920RS/6945RS are DTMF decoder LSIs which can decode 16 kinds of DTMF signals which consist of the combination of 4 high group frequency signals and 4 low group frequency signals.

The MSM6920RS is suitable for the application for End-to-Center equipment or PABX because it has filter characteristics to reduce the mistake in decoding.

The MSM6945RS is suitable for the application for End-to-End equipment because it has a wide detective range.

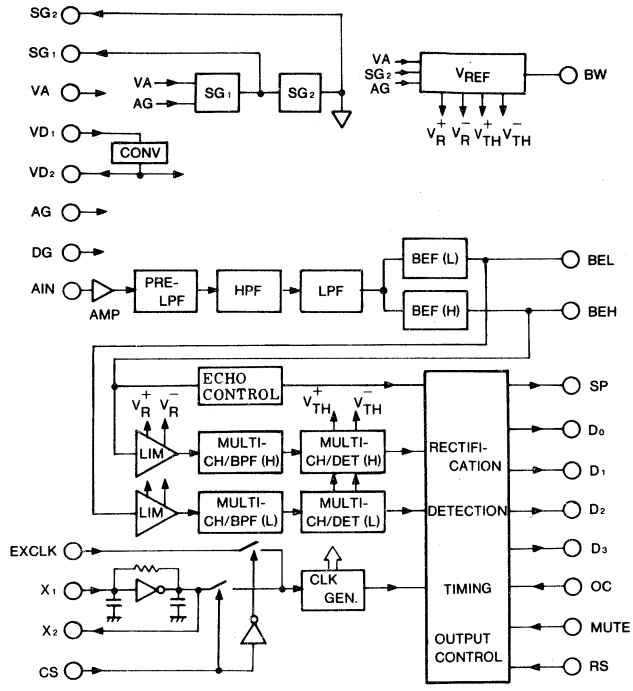
The MSM6920RS/6945RS provide all necessary filtering, detector, timer and miscellaneous logics required to implement the system.

The MSM6920RS/6945RS are fabricated by OKI's advanced CMOS technology which realizes high reliability and low power consumption.

FEATURES

- Power supply: +12V and +5V
- Low power consumption: 80 mV (TYP)
- Input signal level
  MSM6920RS: −5 ~ −32 dBm 600Ω/each tone
  MSM6945RS: −5 ~ −48 dBm 600Ω/each tone
- Built-in RC active pre-LPF
- 3 kHz emphasizing for prevention of the voice error (MSM6920RS only)
- Built-in echo control circuit (MSM6945RS only)
- 3.58 MHz crystal oscillation circuit on chip
- TTL compatible digital interface
- Signal present (SP) output capability
- Tri-state output
- CMOS silicon gate process
- 28-pin plastic DIP package

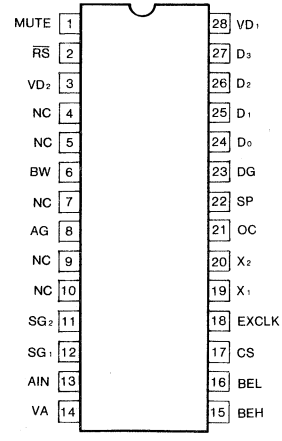
BLOCK DIAGRAM



III

PIN CONFIGURATION (Top View)

28-pin Plastic Package



ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Rating	Unit
Power Supply Voltage	V_A	Ta = 25°C With respect to AG or DG	−0.3 ~ 15	V
	V_D		−0.3 ~ 7	
Analog Input Voltage *1	V_{IA}		−0.3 ~ V_A+0.3	
Digital Input Voltage *2	V_{ID}		−0.3 ~ V_D+0.3	
Operating Temperature	T_{OP}	−	−30 ~ 70	°C
Storage Temperature	Tstg	−	−55 ~ 150	

*1 BW, AIN

*2 MUTE, $\overline{RS}$, CS, EXCLK, X1, OC

Recommended Operating Conditions

Parameter		Symbol	Conditions	Min	Typ	Max	Unit
Power Supply Voltage		V_A	With respect to AG or DG	10.8	12.0	13.2	V
		V_D		4.75	5.00	5.25	
Operating Temperature		T_{OP}	−	−30	−	70	°C
External Attached Parts	R_L	−	R_T = 600 Ω	−	600	−	Ω
		−	R_T = 10 kΩ	−	10	−	kΩ
	R_1	−	−	−	2.4	−	
	R_2	−	−	−	100	−	
	C_1	−	−	−	0.03	−	μF
	C_2	−	−	1	−	−	
	C_3	−	−	0.01	−	−	
	C_4	−	−	−	10	−	
	C_5	−	−	−	10	−	
	CRYSTAL	−	−	−	3.579545	−	MHz

Refer to Application circuit (Figure 4) for external attached parts.

DC and Digital Interface Characteristics
($V_A = 12V \pm 10\%$, $V_D = 5V \pm 5\%$, Ta = −30 ~ 70°C)

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Power Supply Current	I_A	–		–	7	14	mA
	I_D	–		–	0.2	1.0	
Input Leakage Current *1	I_{IL}	$V_I = 0V$		−10	–	10	μA
	I_{IH}	$V_I = V_D$		−10	–	10	
Input Voltage *1	V_{IL}	–		0	–	0.8	V
	V_{IH}	–		2.2 (0.7 VD)	–	VD	
Output Voltage *2	V_{OL}	$I_O = 0.36$ mA		0	–	0.4	
	V_{OH}	$I_{OH} = -20$ μA		0.8 VD	–	VD	
Output Leakage Current *2	I_{OLL}	MUTE ="H"	To D_G	−10	–	10	μA
	I_{OLH}		To V_D	−10	–	10	

*1 MUTE, $\overline{RS}$, CS, OC, (EXCLK)
*2 SP, D_0, D_1, D_2, D_3

III

Analog Interface Characteristics
(V_A = 12V±10%, V_D = 5V±5%, Ta = −30 ~ 70°C)

Parameter		Symbol	Conditions	Min	Typ	Max	Unit
Input (AIN) Resistance		RIN	$f_{IN} \leq 5$ kHz $v_{IN} \leq +1$ dBm	2	–	–	MΩ
Input Leakage Current	AIN	I_{LA1}	0V (AG) $\leq V_{IN} \leq V_A$	−10	–	10	μA
	BW	I_{LA2}	V_{IN} = 0V (AG)	−100	–	10	
Input (AIN) Signal Detection Level		V_{IN1}	For each tone	−32 / −48	–	−5 / −5	dBm
Input (AIN) Signal Non-detection Level		V_{IN2}		–	–	−40 / −56	
Tone Frequency Deviation Accept	Low Group	B_{WLD1}	BW is not connected	–	–	2.4	%
	High Group	B_{WHD1}		–	–	2.1	
Tone Frequency Deviation Reject	Low Group	B_{WLR1}		3.8	–	–	
	High Group	B_{WHR1}		3.6	–	–	
Tone Frequency Deviation Accept	Low Group	B_{WLD2}	BW = 0V (AG)	–	–	2.0 / –	
	High Group	B_{WHD2}		–	–	2.0 / –	
Tone Frequency Deviation Reject	Low Group	B_{WLR2}		3.3 / –	–	–	
	High Group	B_{WHR2}		3.3 / –	–	–	
Level Twist		V_{TW}	Between two tones	–	–	6	dB
Signal echo level ratio		S/E	Vsignal/Vecho	– / 18.2	–	–	dB
Signal Groud (SG2) Voltage		V_{SG2}	–	$\frac{VA}{2}$ −0.1	$\frac{VA}{2}$	$\frac{VA}{2}$ +0.1	V

MSM6920 / MSM6945

0 dBm = 0.775 Vrms

Band Split Filter Characteristics
(VA = 12V±10%, VD = 5V±5%, Ta = −30 ~ 70°C)

Parameter		Symbol	Conditions		Min	Typ	Max	Unit
Dial Tone Rejection		D_{TR}	Relative Value to 750 or 1500 Hz	0 ~ 420 Hz	43	–	–	dB
Low Group	Pass Band Gain	G_{L1}	Relative value to 750 Hz	677 ~ 967 Hz	−2.5 / −1.6	–	2.5 / 1.6	
	Rejection Band Gain	G_{L2}		1175 ~ 1678 Hz	–	–	−21	
High Group	Pass Band Gain	G_{H1}	Relative value to 1500 Hz	1175 ~ 1678 Hz	−2.5 / −1.6	–	2.5 / 1.6	
	Rejection Band Gain	G_{H2}		677 ~ 967 Hz	–	–	−21	

Above values can be defined and measured at the pin of BEL or BEH.

MSM6920 / MSM6945

III

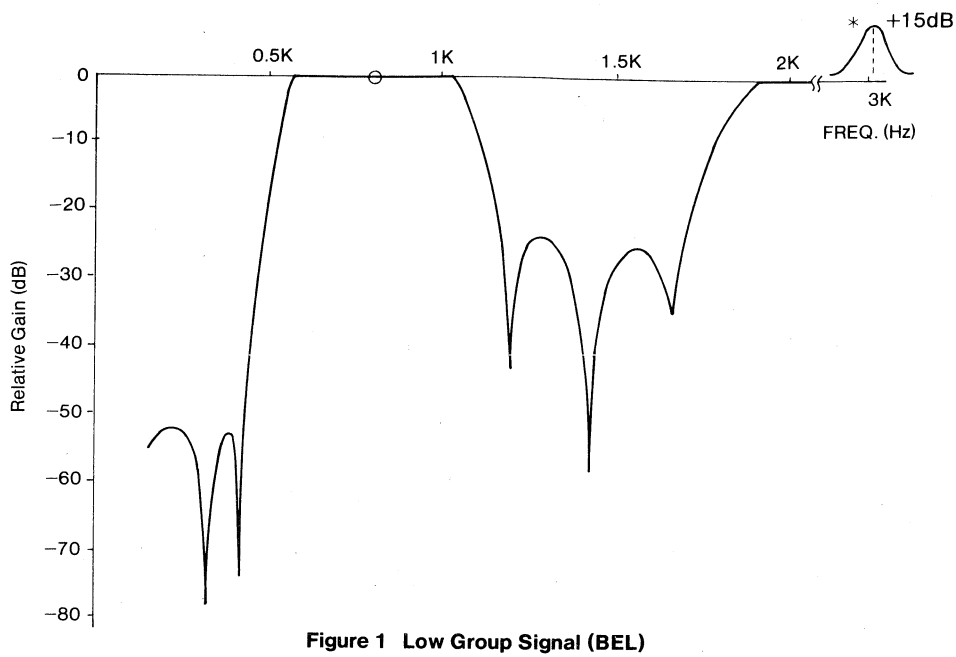
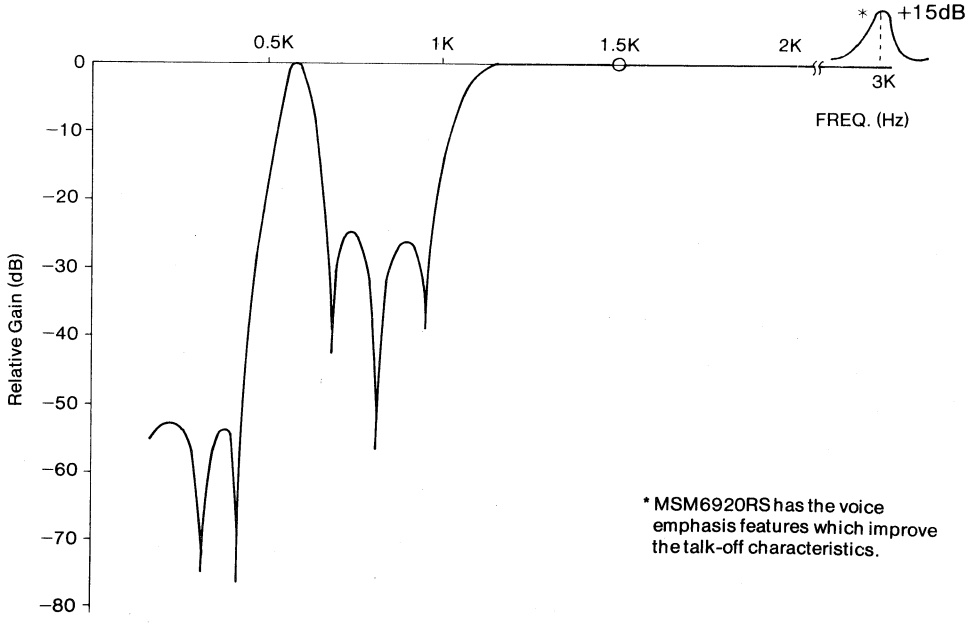


Figure 1 Low Group Signal (BEL)



* MSM6920RS has the voice emphasis features which improve the talk-off characteristics.

Figure 2 High Group Signal (BEH)

Signal Timing Characteristics
(V_A = 12V±10%, V_D = 5V±5%, Ta = −30 ~ 70°C)

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Signal Repetition Time	T_C			120	–	–	ms
Time to Receive	T_S			49	–	–	
Invalid Tone Duration	T_I			–	–	24	
Output Delay Time	T_G			24	–	49	
Interdigit Pause	T_P			30	–	–	
Acceptable Drop Out	T_B			–	–	2	
SP Delay Time	T_{SP}			6	–	10	
Output Continuation Time	T_O	OC	"Low"	40	–	45	
Output Trailing Edge Delay	T_D	OC	"High"	21	–	35	

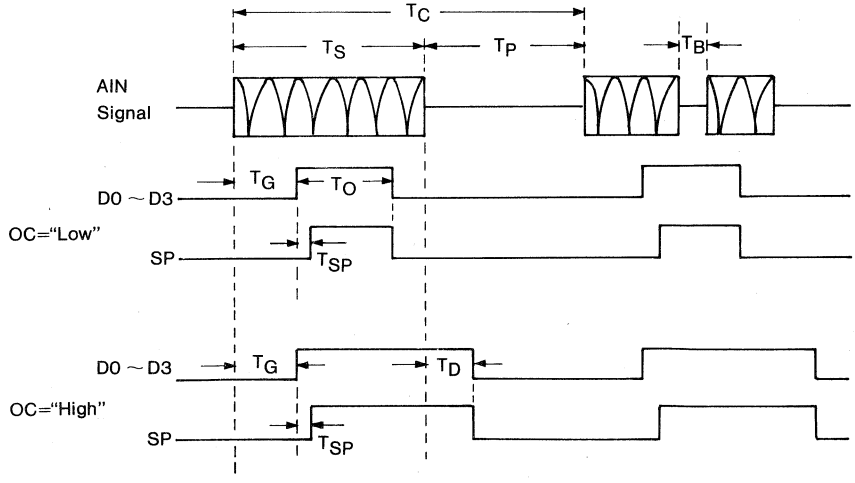


Figure 3 Timing Diagram

III

Hexa-Decimal Digital Output Truth Table

Key \ L/H	Low-Group				High-Group				Digital Output			
	L_1	L_2	L_3	L_4	H_1	H_2	H_3	H_4	D_3	D_2	D_1	D_0
0				○		○			0	0	0	0
1	○				○				0	0	0	1
2	○					○			0	0	1	0
3	○						○		0	0	1	1
4		○			○				0	1	0	0
5		○				○			0	1	0	1
6		○					○		0	1	1	0
7			○		○				0	1	1	1
8			○			○			1	0	0	0
9			○				○		1	0	0	1
A	○							○	1	0	1	0
B		○						○	1	0	1	1
C			○					○	1	1	0	0
D				○				○	1	1	0	1
*				○	○				1	1	1	0
#				○			○		1	1	1	1

1 ..... Digital High Level
0 ..... Digital Low Level

PIN DESCRIPTIONS

Pin Name	Pin No.	Function
MUTE	1	3-state output control input. If MUTE = digital "High", the outputs D_0, D_1, D_2, D_3 and SP are put in a high impedance state. If MUTE = digital "Low", these outputs are activated.
$\overline{RS}$	2	Power-ON Reset control input. If $\overline{RS}$ = digital "Low", the outputs D_0, D_1, D_2, D_3 and SP are put in a high impedance state whether Mute = digital "Low" or "High". Applying of this function is drawn in the following Application, Figure 5,6.
VD_2	3	This is used for "Power-ON Reset" function. Refer to Figure 5, 6.
NC	4	Non-Connection
NC	5	Non-Connection
BW	6	If BW is connected to AG, "Tone Frequency Deviation Accept and Reject" range are set to be fit for the PABX application. If BW is left opened, this device shows the characteristics that is fit for the End-to-Center application. In PABX application, the analog line interface circuit must be arranged according to Figure 8 to adjust the input DTMF signal level.
NC	7	Non-Connection
AG	8	Ground reference of VA. (Analog Ground) This pin should be common with DG at the System Ground point as close as possible.
NC	9	Non-Connection
NC	10	Non-Connection
SG_2	11	SG2 is built-in analog signal ground. This voltage is nearly VA/2 volts, so the analog line inteface of AIN must be implemented by AC-coupling as shown in Figure 4. To make its impedance lower over wide frequency range, it is necessary to be AC grounded for AG via a bypass capacitor of more than 1 μF.
SG_1	12	This is voltage reference for SG2 and is obtained by two-equal resistors devision among VA and AG. If VA has some noise and ripples, it is necessary to be AC grounded for AG via a bypass capacitor of more than 0.01 μF so as to keep SG2 silent. If the bypass capacitor is 0.01 μF, the rejection ratio at 500 Hz is kept more than 9 dB because of a high resistive impedance of SG1.
AIN	13	A DTMF signal input. For the interface with phone line, refer to Figure 4.

Pin Name	Pin No.	Function
VA	14	Power supply pin for the analog circuit. A +12V supply is recommended.
BEH	15	A High group signal output picked out from a DTMF signal by Band split filter. This pin is used for IC-Test only.
BEL	16	A Low group signal output picked out from a DTMF signal by Band split filter. This pin is also used for IC-Test only.
CS	17	If an external 3.58 MHz clock is required to use, CS must be connected to digital "Low" in order to input the clock to EXCLK. When crystal controlled oscillator on chip is required, this pin must be connected to digital "High".
EXCLK	18	If required to use an external 3.58 MHz clock, CS must be connected to EXCLK. When crystal controlled oscillator on chip is required, this pin should be connected to digital "Low" or "High". The interface condition of EXCLK is different from other digital inputs. Refer to Figure 7.
X_1	19	Crystal Sense. X_1 and X_2 connect to a 3.579545 MHz crystal to generate a crystal locked clock for the chip. If required to use a external clock, X_1 should be connected to digital "Low" or "High" and X_2 should be left opened.
X_2	20	Crystal Drive. Refer to pin 19 for details.
OC	21	The time length of digital outputs control input. If OC = digital "High", the digital outputs D0, D1, D2, D3 and SP follow the DTMF signal in the time length. If OC = digital "Low", D0, D1, D2, D3 and SP output the constant time length data regardless of the DTMF signal length. Refer to Figure 3.
SP	22	DTMF signal present output. SP is used for scanning detection of the data outputs D0, D1, D2 and D3, and so on.
DG	23	Ground reference of VD1. (Digital Ground) This pin should be common with AG at the system Ground point as close as possible.
D_0	24	Digital outputs with Hexa-decimal code. High output impedance is capable. Refer to "Digital Output Truth Table".
D_1	25	
D_2	26	
D_3	27	
VD_1	28	Power supply pin for the digital circuit. A +5V supply is recommended.

APPLICATION NOTE

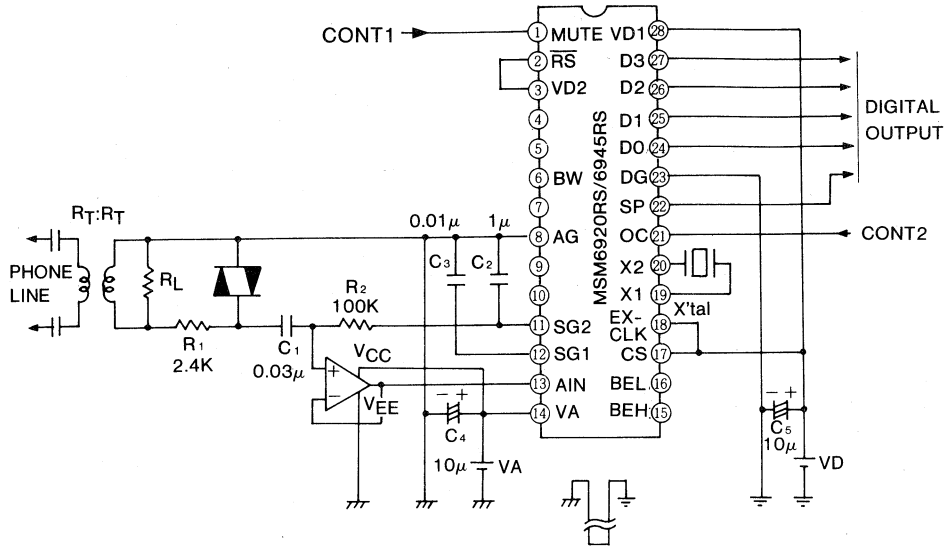


Figure 4 Application Circuit

	CONT 1		CONT 2	
	"H"	"L"	"H"	"L"
DIGITAL OUTPUT IMPEDANCE	Hi	Lo	–	–
DIGITAL OUTPUT LENGTH	–		Following AIN signal	Constant length

NOTICE
1. The crystal should be wired at a close physical proximity to the device.
2. High level signals should be avoided to route next to low level signals.
3. Bypass capacitors put on VA, SG1 and SG2 should be as close to the device as possible.
4. AG and DG should be connected at the point that is as close to the system ground as possible.
5. As for an application for PABX, refer to Figure 8.

- **Power ON Reset Function**

If required "Power ON Reset" function that is used for neglecting the invalid output data immediately after Power ON, the following circuit may be of use.

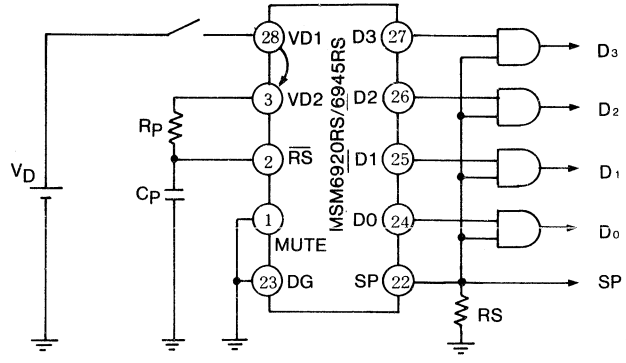


Figure 5

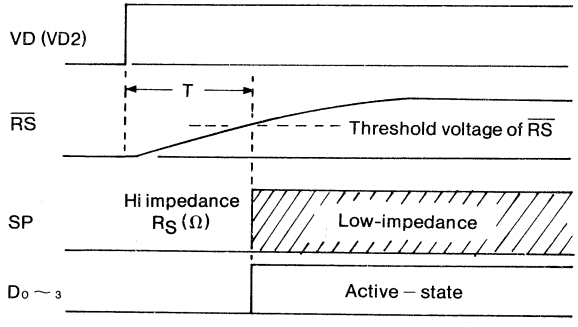


Figure 6

After Power ON, SP is hold at digital "Low" by the existence of resistor R_S during "T" seconds. Normal values of R_S, R_P and C_P are 100 kΩ, 5 MΩ and 0.47 μF respectively. In this case, "T" will be 1.6 second approximately. In this case, the gate which receives output should be CMOS.

Be careful to the fact that SP has not perfect Hi-output impedance by the existence of R_S even though MUTE is connected to digital "High" and other outputs are in the state of Hi-output impedance.

- **External Oscillator Connection**
  In case of using an external clock as a oscillation source, following circuit can be applied.

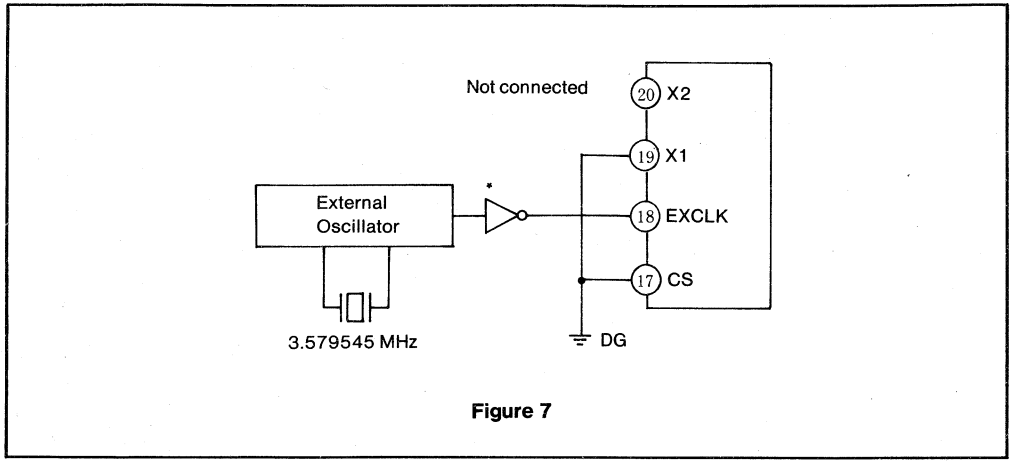
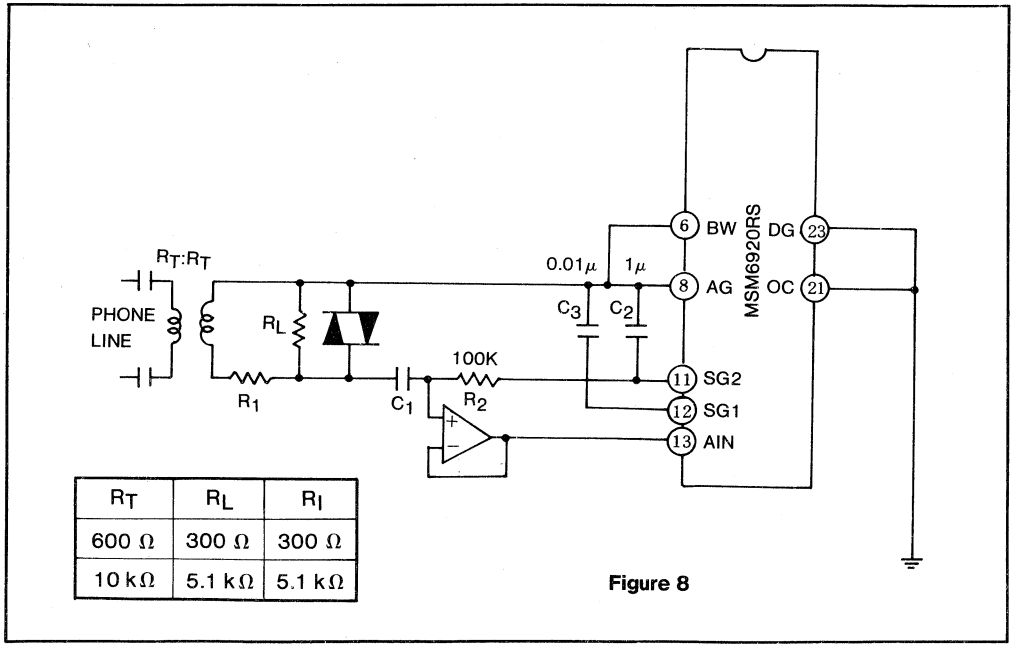


Figure 7

* TTL or High-Speed CMOS Gate with less than 50pF load capacitance

- **Application for PABX (MSM6920RS)**
  In PABX system, DTMF signal level is relatively high in comparison with the level of "End to Center". In case of Application for PABX, the signal detection level range should be 0 ~ −20 dBm and the Non-detection level must be less than −35dBm. So, the application circuit in Figure 4 cannot be applied. In this case following circuit can be applied. BW and OC should be connected to AG and DG respectively. Be careful to the position of R1.

III



R_T	R_L	R_1
600 Ω	300 Ω	300 Ω
10 kΩ	5.1 kΩ	5.1 kΩ

Figure 8

MSM6980-03

32K-BIT/SEC ADPCM CODEC

GENERAL DESCRIPTION

The MSM6980-03 is a 32K-bit/sec ADPCM CODEC which is fabricated by OKI's low power consumption CMOS silicon gate technology.

The MSM6980-03 is used for highly efficient digital-to-digital converting of PCM voice data with the transmission rate of 32K-bit/sec.

When MSM6980-03 is applied as the transcoder together with the common 64K-bit/sec PCM voice CODEC, the transmission line come to have double data transmission data capability as MSM6980-03 can code the 64K-bit/sec PCM code into the 32K-bit/sec ADPCM code or can decode the ADPCM data into the PCM data without losing the quality of the voice.

MSM6980-03 can be applied into various applications, like high speed data multiplexer used on a digital line, in the digital PBX or in the digital data terminal equipment.

FEATURES

- 9600 bps modem signal (CCITT V.29) transmission* capability by OKI's original coding algorism.
  Asynchronous tandem connection; capability within 2-link.
  Synchronous tandem connection; capability regardless of link number.
- Voice or tone signal transmission can be performed conforming to CCITT G.721 (ADPCM) recommendation.
- Lower data transmission rate (24K bit/sec) is capable in voice signal transmission.
- μ-law and A-law selectable.
- ADPCM coding or decoding selectable.
- Parallel and serial I/O terminals.
- Serial data output is possible to be Wired-OR connection within 32 channel for multiplexing.
- Serial I/O can interface with wide range of clock rate: 32 ~ 2048K bit/sec.
- Stabilized operation to the asynchronous interfacing timing signal and its jitter.
- Low power consumption; 70 mW (TYP).
- Extenally clock for operation; 20 MHz
- 42 pin plastic DIP package.

* : ADPCM system standard was recommended in 1984 as CCITT G.721. In this standard, 9600 pbs modem transmission is not guaranteed.

FUNCTIONS

The ADPCM CODEC LSI (MSM6980-03) can be used as a coder (conversion from PCM code to ADPCM code) or a decoder (conversion from ADPCM code to PCM code) by pin selection.

Coder Function

This function makes linear conversion to a PCM signal (8-bit code of 8 kHz sample) and then converts it to a 4-bit or 3-bit code signal by ADPCM coding.

Refer to the coder function in the BLOCK DIAGRAM.

(1) A serial (2 MHz–64 kHz) or parallel input signal is selected as a PCM input signal according to the IS/P pin setting.

(2) An input signal of μ-law or A-law PCM code is coded by ADPCM method according to the A/μ pin setting.

(3) 4-bit or 3-bit ADPCM coding is performed according to the 3BIT pin setting.

(4) Serial (2 MHz–64 kHz in bit rate) or parallel ADPCM signal is output according to the C/D and 3BIT pin setting.

(5) Input/output is made on receipt of an external input/output request signal. Input/output is also made without fail on receipt of an input/output request signal which is pseudo-synchronized.

(6) Output is multiplied by wired OR.

Decoder Function

This function performs ADPCM decoding process to a 4-bit or 3-bit ADPCM input signal and then converts the decoded signal to a PCM code signal.

Refer to the decoder function in the BLOCK DIAGRAM.

(1) A serial (2 MHz–32 kHz in bit rate) or parallel ADPCM input signal is selected according to the IS/P pin setting.

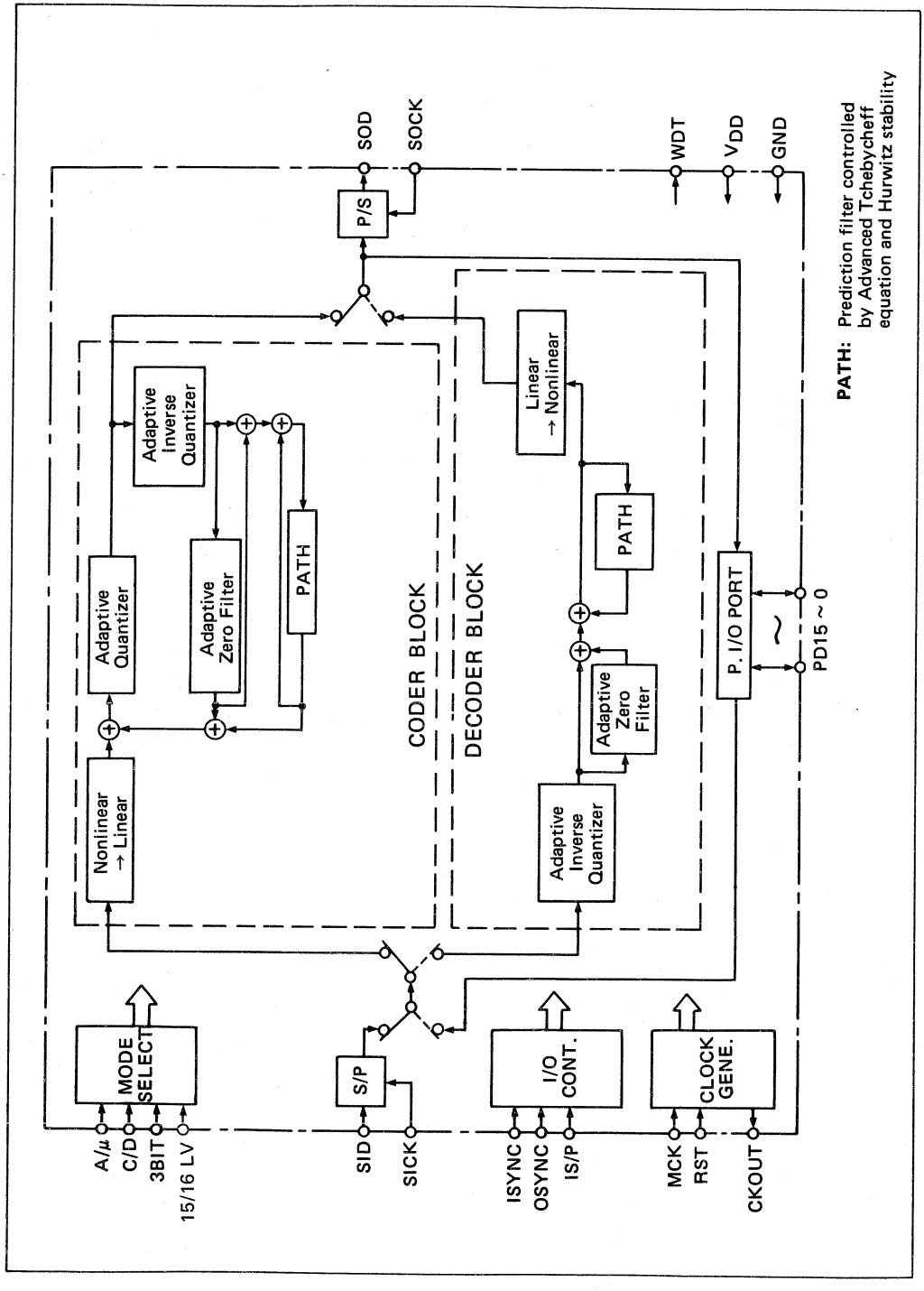
(2) Decoding into PCM code is conducted by setting the 3BIT pin according to the selection of the type of and ADPCM input, either 4-bit or 3-bit.

(3) μ-law or A-law is selected for PCM code by the A/μ pin setting.

(4) Serial (2 MHz–64 kHz) or parallel PCM output signal is selected according to the C/D and 3BIT pin setting

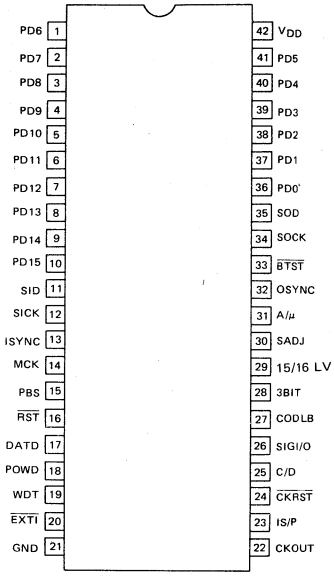
(5) Input/output is made on receipt of an external input/output request signal. Input/output is also made without fail on receipt of an input/output request signal which is psuedo-synchronized.

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)

42-pin Plastic DIP



III

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Supply Voltage	V_{DD}	Ta = 25°C	-0.3 ~ +7	V
Input Voltage	V_{IN}		-0.3 ~ V_{DD} + 0.3	V
Power Dissipation	P_D		1	Watt
Storage Temperature	Tstg	—	-65 ~ +150	°C
Storage Humidity	Hstg	—	5 ~ 95	%RH

Operating Conditions

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Ambient Temperature	Ta	—	0	—	70	°C
Supply Voltage	V_{DD}	—	+4.75	+5.00	+5.25	V
Ground	GND	—	—	0	—	V
Clock Frequency	Fc	—	19.998	20	20.002	MHz
InPut Rise or Fall Time	T_R, T_F	—	—	—	—	ns

III

DC Electrical Characteristics

V_{DD} = +5 V ±5%, Ta = 0 ~ 70°C

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Quiescent Current	I_{DD_1}	Clock is not input to work.	—	1.0	2.0	mA
Operating Supply Current	I_{DD_2}	Fc = 20 MHz	—	14	20	mA
Low Level Input Voltage	V_{IL}	—	—	—	0.8	V
High Level Input Voltage	V_{IH_1}	MCK, SICK, SOCK	2.4	—	—	V
	V_{IH_2}	Other Input pins	2.0	—	—	
Low Level Output Voltage	V_{OL_1}	SOD, I_{OL} = 6.0 mA	—	—	0.4	V
	V_{OL_2}	Other Output pins I_{OL} = 1.6 mA	—	—	0.4	
Low Level Output Voltage	V_{OL}	I_{OL} = 1.6 mA	—	—	0.4	V
High Level Output Voltage	V_{OH}	I_{OH} = 40 μA	4.2	—	—	V
Input Current	I_I	V_{IN} = V_{DD} or GND	-10	—	+10	μA
Input Capacitance	C_I	—	—	—	10	PF
Output Load Capacitance	G_{LOAD}	—	—	—	100	PF

PIN DESCRIPTION

Pin Name	Pin No.	Function
PD0 ~ PD15	1 ~ 10 36 ~ 41	These are bi-directional bus interface pins. PD15 is the MSB. Refer the specification to Table 1 and 2, and refer the timing in the Figure 1 and 3. During RST or OSYNC is being held on digital "0", all of PD0 ~ PD15 become at digital "1" state with output impedance of more than 100 kΩ.
SID	11	Serial data input pin. The bit length should be 4 or 8. Refer to Figure 2.
SICK	12	Input pin of a clock signal for serial input data. The maximum clock rate is 2048 Kbps and should be more than total data bit number. Refer to Figure 2.
ISYNC	13	8 kHz synchronizing pulse signal input pin. This is used for reading the parallel or serial input data.
MCK	14	System clock input pin. The clock frequency should be 20 MHz.
PBS	15	Chip test pin. Normally, PBS should be connected to digital "0".
$\overline{RST}$	16	Reset signal input pin. When MSM6980-03 is powered on, "L" level reset signal has to be applied to this pin. In the case of data comparison test, $\overline{RST}$ should be input according to Figure 6 $\overline{RST}$ Timing Chart in order to make the first output data valid. During $\overline{RST}$ is held on digital "0", all of PD0 through 15 become digital "1" state with output impedance of more than 100 kΩ and SOD has a high output impedance.
DATD	17	Chip test pin. Normally, DATD should be open.
POWD	18	Chip test pin. Normally, POWD should be open.
WDT	19	Supervisory signal output on internal function, i.e., Watch Dog Timer. When MSM6980-03 is operating normally, WDT synchronized with ISYNC is output. Refer to Figure 5.
$\overline{EXTI}$	20	Chip test pin. In normal operating modes, $\overline{EXTI}$ should be constantly set at digital "1".
GND	21	Ground pin.
CKOUT	22	Chip test pin. The clock pulse, the frequency of which is divided by 4 of MCK, is output. Normally, it is 5 MHz.
IS/P	23	Data input format select pin. By inputting digital "1" or "0" to IS/P, parallel or serial data input format is determined. Digital "1": Serial input Digital "0": Parallel input Refer to Table 1.
$\overline{CKRST}$	24	Chip test pin. Normally, $\overline{CKRST}$ should be connected to digital "1".
C/D	25	Operating mode select pin. The condition of C/D determines the operation of MSM6980-03, coding operation or decoding operation. Digital "1": Coding operation Digital "0": Decoding operation Refer to Table 1.

Pin Name	Pin No.	Function
SIG I/O	26	Chip test I/O pin. Normally, SIG I/O should be open.
CODLB	27	Chip test pin. Normally, CODLB should be connected to digital "0".
3 BIT	28	ADPCM data bit length select pin. Digital "1": 3 bits Digital "0": 4 bits Refer to Table 2.
15/16 LV	29	ADPCM data format select pin. Digital "1": 15 levels without "0000" Digital "0": 16 levels
SADJ	30	Chip test pin. Normally, SADJ should constantly set at digital "0".
A/μ	31	PCM code select pin. Digital "1": A-law Digital "0": μ-law
OSYNC	32	8 kHz synchronizing signal input pin to control the parallel or serial outputs. Refer to Figure 3 and 4.
$\overline{\text{BTST}}$	33	Chip test pin. Normally, $\overline{\text{BTST}}$ should be connected to digital "1".
SOCK	34	Clock signal input pin to control the serial data output. Maximum data rate is 2.048 Mbps. Refer to Figure 4.
SOD	35	Serial data output pin. The bit length can be 4 or 8. After the determined bit number has been output, SOD becomes the high output impedance terminal. Refer to Figure 4.
V_{DD}	42	+5 V power supply.

Table 1 Input/Output Setting Status Table

Operating Mode	Input		Output		Control Pins	
	Bit Length	P/S	Bit Length	P/S	C/D	I S/P
ADPCM Decoder	4 (3)	P	8	P*2 and S	0	0
		S				1
ADPCM Coder	8	P	4 (3)	P and S	1	0
		S				1

*1 P: Parallel Format
S: Serial Format

*2: Both P and S are output

Table 2 Parallel I/O Application Table

I/O	Input			Output		
	Coder	Decoder		Coder		Decoder
		4 bit	3 bit	4 bit	3 bit	
PD15 ~ 12				MSB ⟨ LSB	MSB ⟨ LSB	MSB
PD11 ~ 8						LSB
PD7 ~ 4	MSB ⟨ LSB					
PD3 ~ 0		MSB ⟨ LSB	MSB ⟨ LSB			

III

TIMING CHART

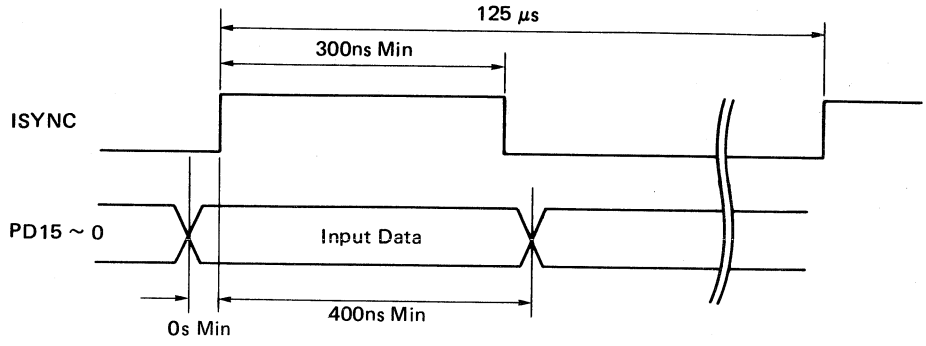


Figure 1 Parallel Input

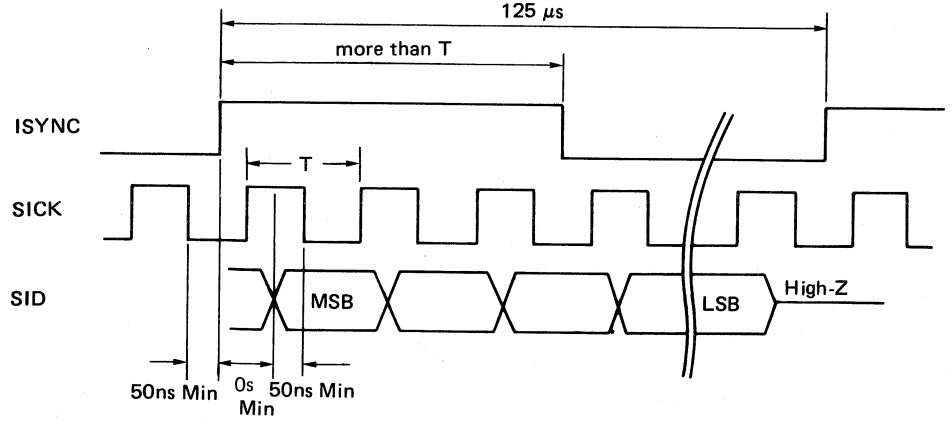


Figure 2 Serial Input

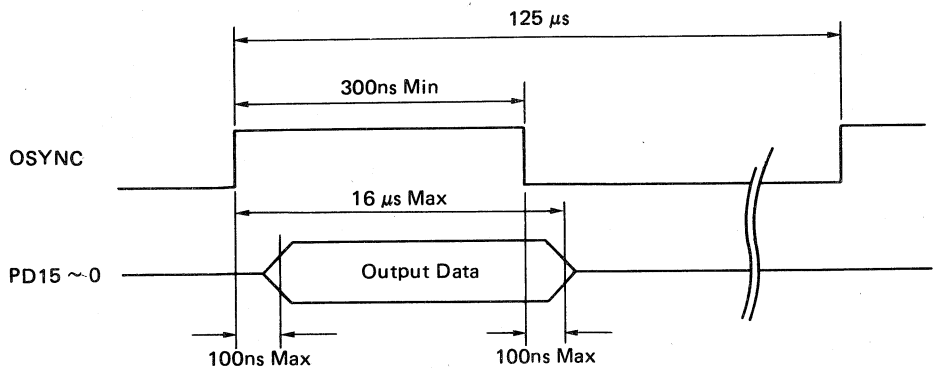


Figure 3 Parallel Output

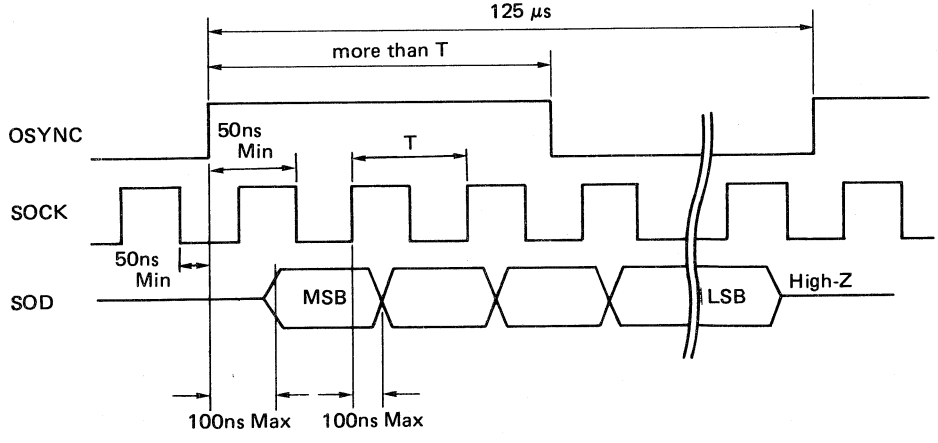
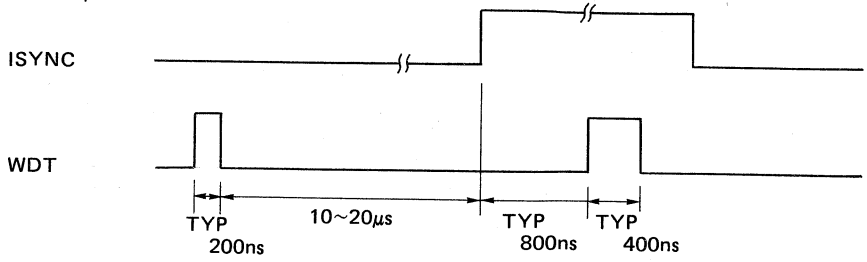
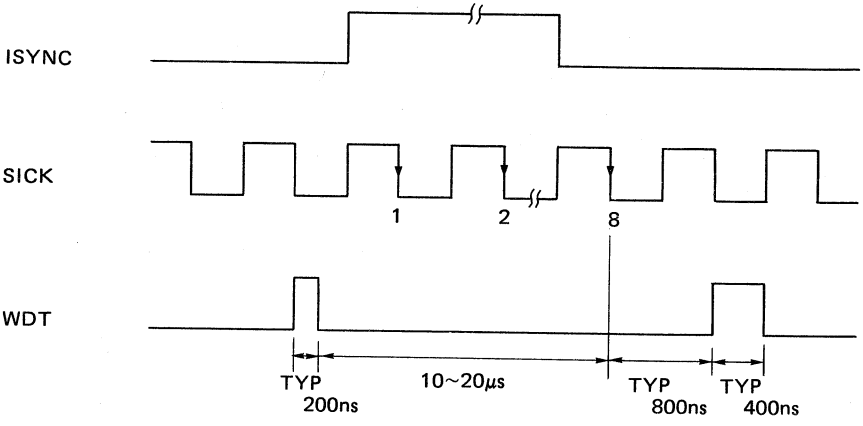


Figure 4 Serial Output

(1) Parallel Input



(2) Serial Input Coder Function



(3) Serial Input Decoder Function

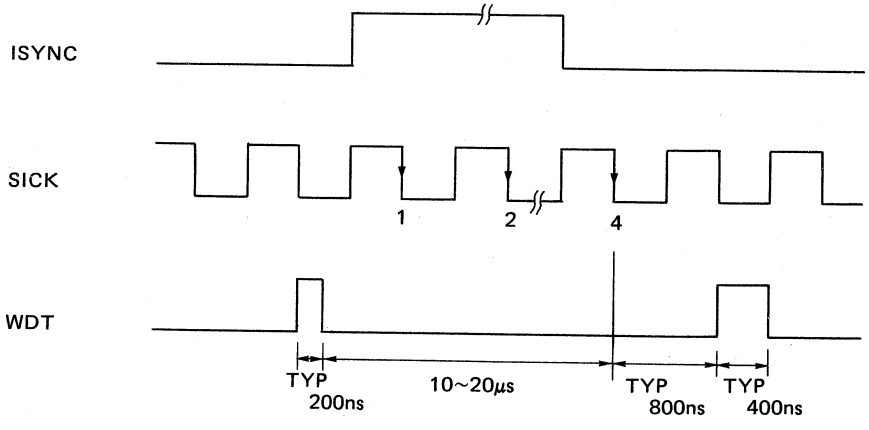


Figure 5 WDT

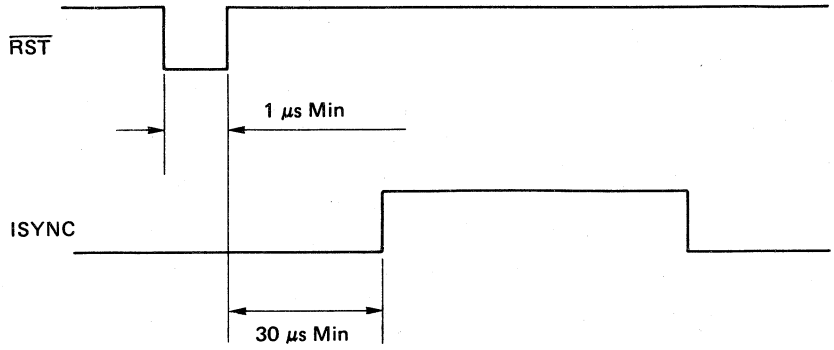


Figure 6 $\overline{\text{RST}}$

APPLICATION CIRCUIT

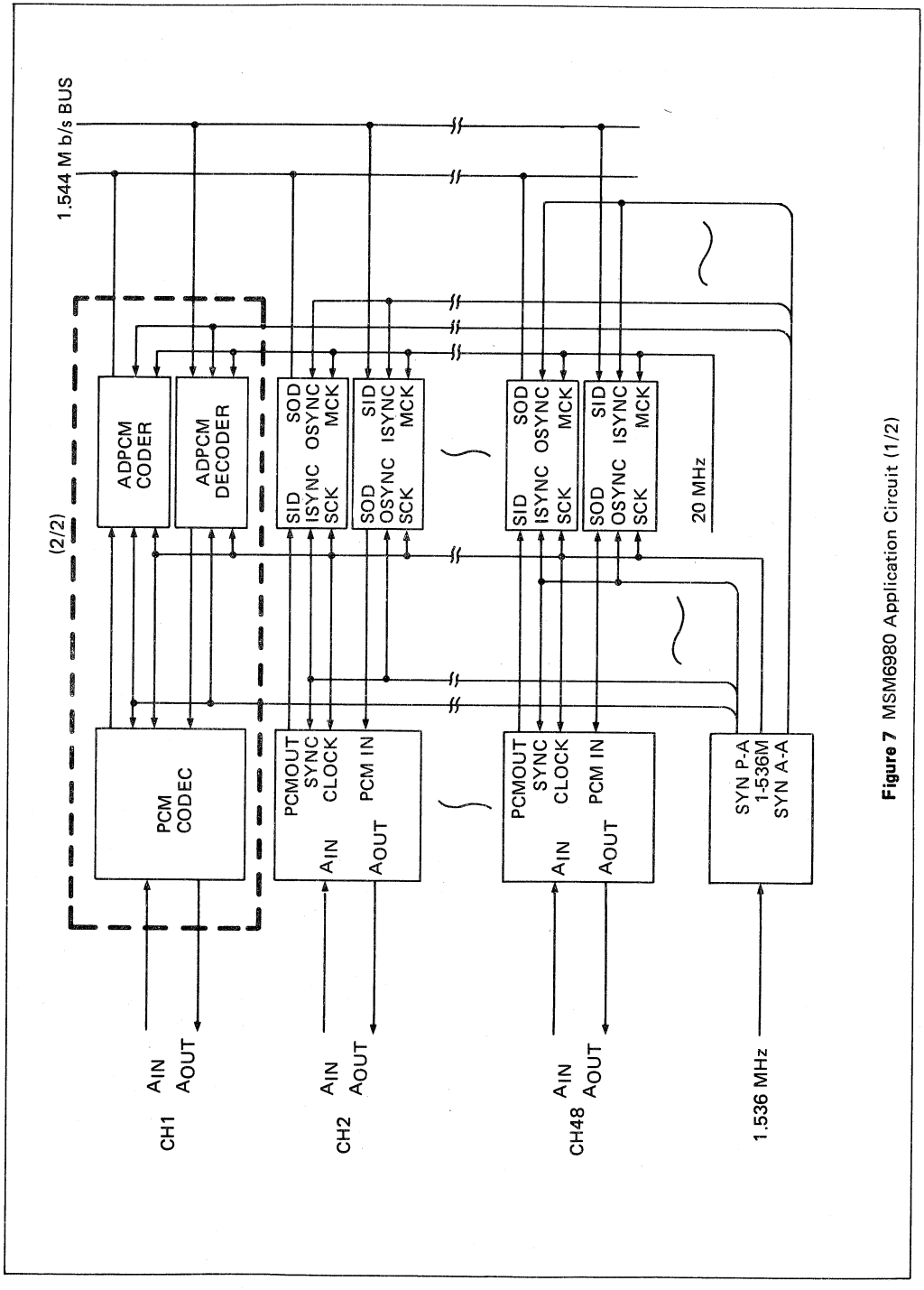


Figure 7 MSM6980 Application Circuit (1/2)

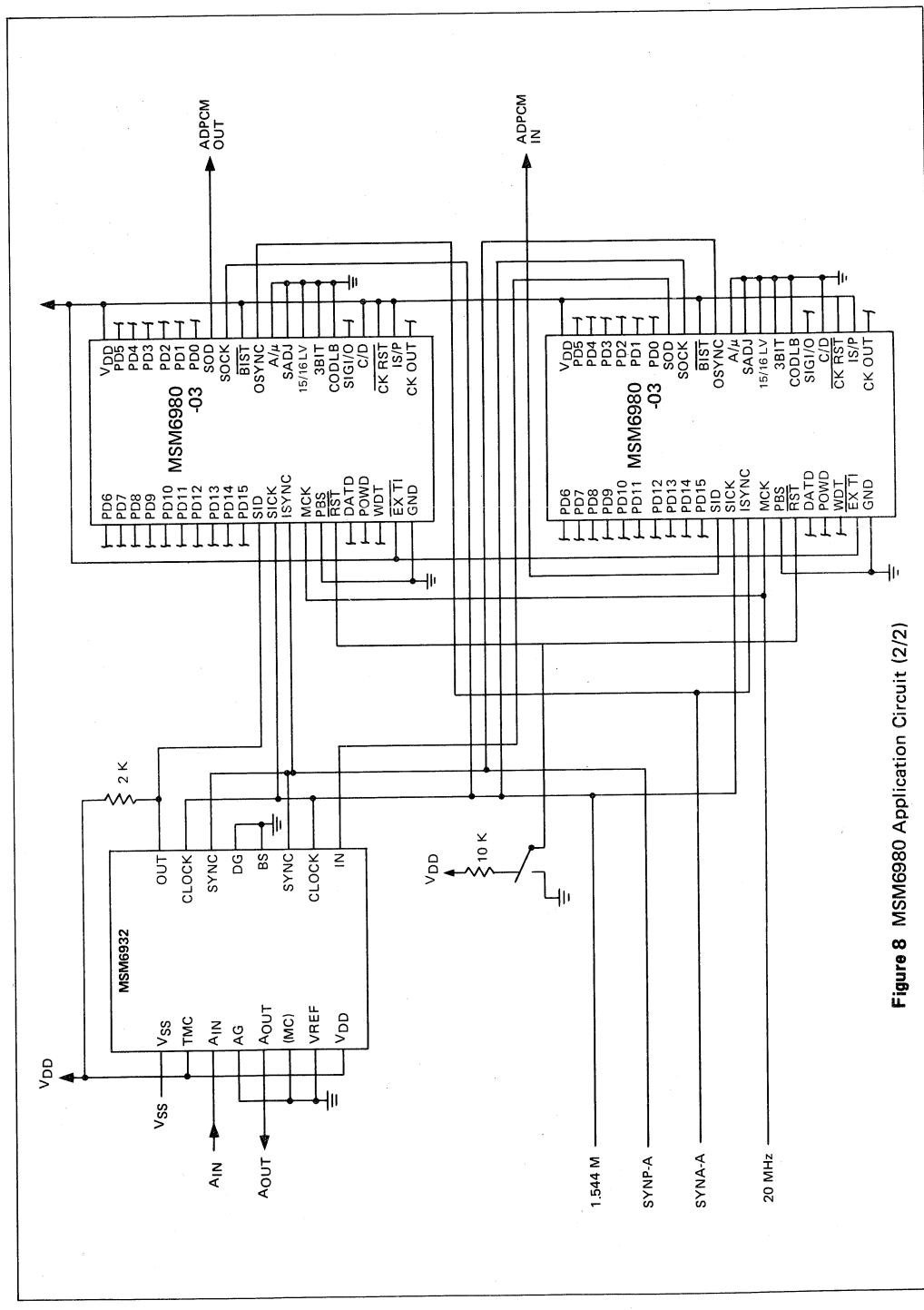


Figure 8 MSM6980 Application Circuit (2/2)

IV
APPLICATION NOTE FOR SINGLE CHIP MODEM

APPLICATION NOTE

1. AN INTRODUCTION TO THE MODEM

These days reflect our so-called communication era, and the data processing industry has been growing at a tremendous rate, particularly in the area using the existing telephone networks. The modems are playing an important role as an interface to computer systems which communicate by a public or dedicated data transmission networks. Taking early notice of the significance of data communications, OKI has been engaged since many decades in the development and manufacturing of data communication-related equipments. This application note introduces and explains OKI's latest development in this field, the CMOS Single-chip modem series, MSM6926, MSM6927, MSM6946, and MSM6947. Before entering details of this new series, let us first see what a modem is all about.

1) What is a modem?

2) Modem communication systems

3) Modem types and modulation/demodulation methods

1) What is a modem?

Figure 1-1 shows a typical data communication system using modems. The basic role of a modem is to convert digital logic signals "1" and "0" into analog equivalent that can be passed through a telephone line, and vice versa.

A data signal (digital signal) from a data terminal is once converted into an analog audio signal, and transmitted to the modem of a receiving terminal utilizing the public telephone network. At the receiving end, the analog audio signal thus received is then converted by its modem into a corresponding digital signal and conveyed to the receiving data terminal.

In this way, two distant data terminals can communicate for the exchange of data by means of modems.

The telephone line allows transmission of analog audio signals exclusively, but the digital data signal, as such, cannot be passed through. For this reason, modems are required as interface to existing analog transmission lines.

Referring to Figure 1-1, modulation and demodulation means the conversion of digital signals into analog and vice-versa, and will be detailed in the chapter "MODES TYPES AND MODULATION/DEMODULATION METHODS". The duplexer transmits a signal to the telephone line or receives it from the telephone line, and is not designed to receive a previously transmitted signal. Usually, it uses a hybrid transformer or hybrid resistor circuit consisting of two operational amplifiers, resistors and a line transformer.

2) Modem communication systems

The modem communication systems are largely divided into modes of operation. One is called the full duplex system, and the other the half-duplex system. The telephone line is a balanced two-wire circuit, and usually is called the 2-Wire (2W) line. The full-duplex and half-duplex are terms which conform to the common use of this 2-Wire line.

a) 4-Wire full-duplex communication

The 4-Wire full-duplex communication is another widely practiced method in which two dedicated telephone lines are used for transmission and reception, respectively. This method provides transmission and reception simultaneously, but requires two telephone lines.

b) 2-Wire half-duplex communication

The 2-Wire half-duplex communication is a method which links two terminals in either direction, but only one direction at a time. Namely, when one terminal is transmitting, the other must operate in the receiving mode. This limitation may be a drawback for certain applications.

c) 2-Wire full-duplex communication

The 2-Wire full-duplex communication is a method in which duplexers or the like are used to permit two distant termnals to work in both directions simultaneously through a 2-Wire line. This method is more economical compared with 2-Wire half duplex.

The above three methods are schematically shown in Figure 1-2.

3) MODEM types and modulation/demodulation methods

Table 1-1 shows a classification of modems.

The modems can also be classified by transmission speeds. Within 300 bps to 9600 bps, low-speed modems usually employ FSK (frequency shift keying) method, medium-speed modems PSK (phase shift keying), and high-speed modems QAM (phase quadrature amplitude modulation).

The CCITT and BELL in the table stand for European and U.S. standards, respectively.

What are FSK, PSK and QAM, then?

Figure 1-3 shows the operating principles of FSK and PSK. In the FSK system, logic data signals "1" and "0" are modulated with frequencies; for example, "1" is modulated with a lower frequency (f_L), while "0" is modulated with a higher frequency (f_H).

In the PSK system, the frequency is constant, and the modulation is carried out by assigning phase 0° to say "1" and phase -180° to "0". (Two-phase phase shift keying) The QAM system is a complex one in which PSK and AM are combined. By way of example, frequencies and phase angles assigned in FSK and PSK are shown in Table 1-2.

When referring to the modem modulation systems, we must speak of two important terms. One is the modulation rate (baud rate) and the carrier frequency. In the FSK system, the transmission speed and modulation rate are equal. This is because carrier frequencies are in one to one correspondence to logic values "1" and "0".

Where four phase angles are assigned to two data digits (that is, four 2-bit values) as in the 4-phase PSK system, the modulation rate becomes half of the transmission speed.

In the 4-phase PSK system (1200 bps), for example, the modulation rate is 600 bauds. In the FSK system (300 bps), on the other hand, the modulation rate is 300 bauds.

You remember that the 2-Wire full-duplex communication is subject to limitations in its implementation. This is because a group-wise communication system using the originate mode and answer mode as shown in Table 1-2 must be employed. In any modulation system, whether FSK or PSK, a number of harmonics are produced by modulation.

In case of FSK, for example, if logic states "1" and "0" – these are called mark and space, respectively – are modulated in the originate mode specified in CCITT V.21, one is easily tempted to consider that 980 Hz and 1180 Hz alone appear. In actuality, however, there can appear many other frequency components, and their range is called the frequency band. The bandwidth of signal allowed to pass through a public telephone line is limited to a range of 0.3 kHz to 3.4 kHz.

This bandwidth is called the voice band. In the group-wise communication system, this voice band is divided into two bands: the lower frequency band which is assigned to the originate mode channel and the higher frequency band which is assigned to the answer mode channel. These two bands can be used independently each other. For each of these bands, a modulation rate and a carrier frequency are selected so that the resultant frequency components will be included in its frequency band.

In the FSK system, the maximum allowable modulation rate is ordinarily 300 baud. Should it be set at 1200 baud, the frequencies developed will occupy too wide a band to be accommodated in the voice band.

Namely, the 1200 baud FSK system cannot be realized in the full-duplex transmission form.

All these are summed up in Figure 1-4.

Full-duplex transmission cannot be made if bands are overlapped as shown in Figure 1-4(b). As shown in Figure 1-4(c), the 1200-baud FSK system is allowed to have only one channel.

As explained above, the 2-Wire full-duplex communication system is one in which the bi-directional data transmission between two terminals is carried out simultaneously by using channels assigned to transmission and reception previously.

Figure 1-5 shows a typical group-wise full-duplex communication system, which is common to both FSK and PSK systems. In the QAM system, frequency components are spread over a wide range, and the group-wise full-duplex communication system cannot be used. At present, efforts are being made to implement the QAM full-duplex communication system by the echo cancelling technique.

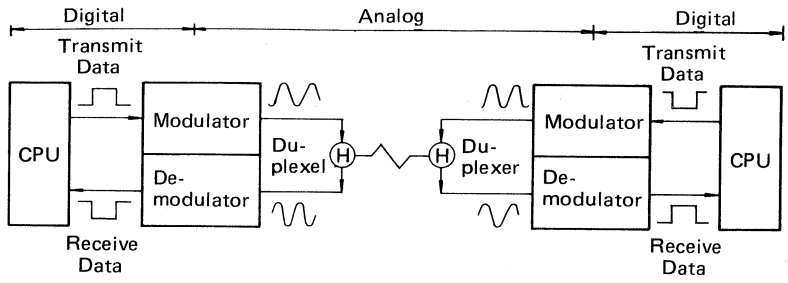


Figure 1-1 Typical Modem System

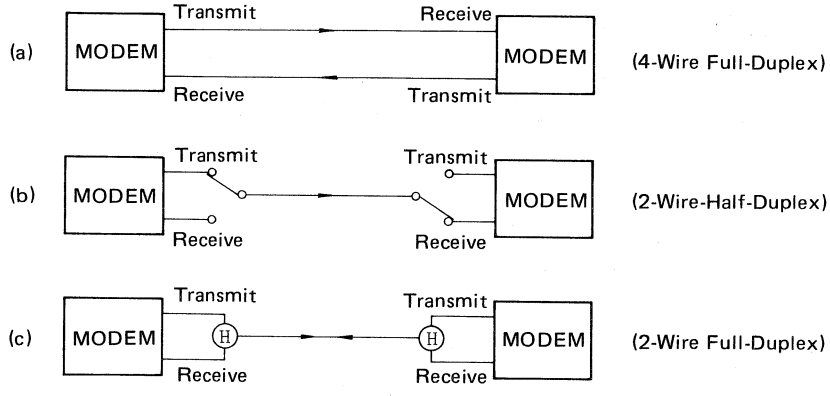


Figure 1-2 Modem Communication System

IV

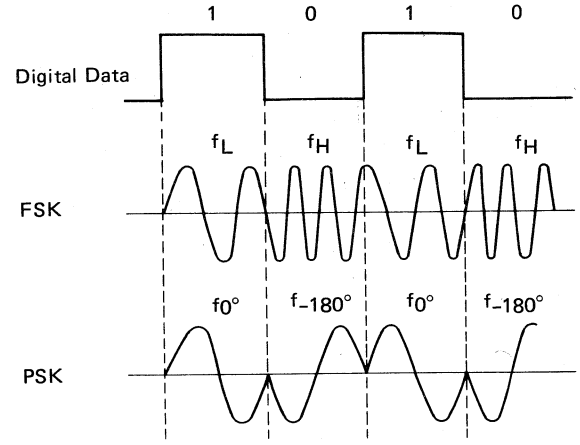


Figure 1-3 Modulated Waveforms

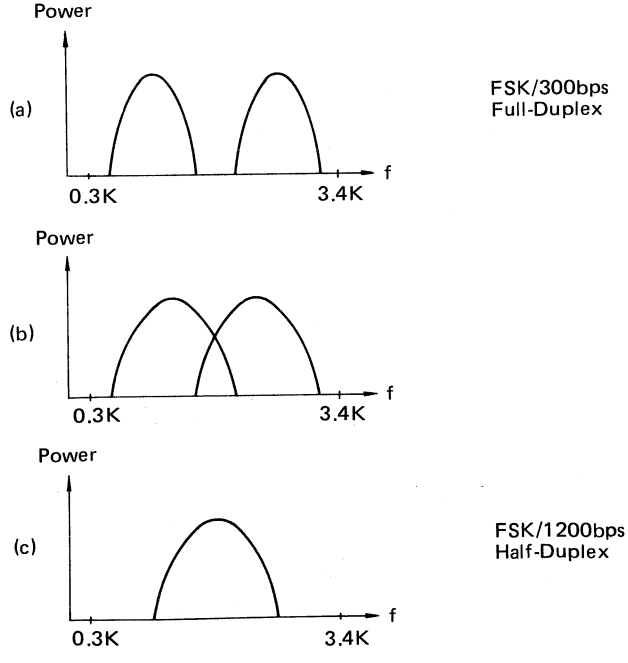


Figure 1-4 Division of Voice Frequency Band

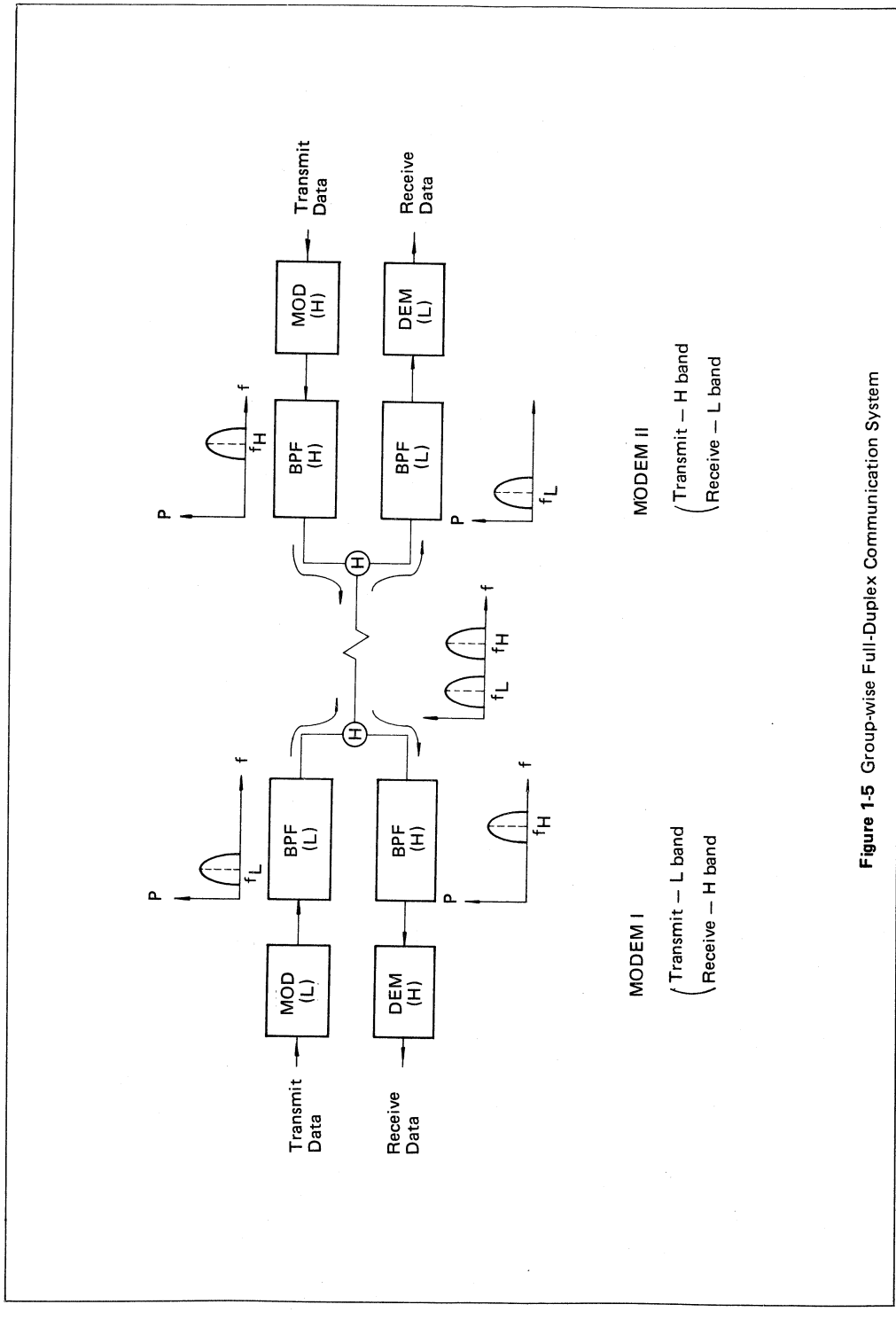


Figure 1-5 Group-wise Full-Duplex Communication System

Table 1-1 Transmission speeds and modulation systems
(Voice-band modem according to CCITT Recommendations)

Data Rate	Modulation	Baud Rate	Carrier Frequency	Bandwidth	Synchronization	Equalizer	CCITT V-series	Similar BELL Standard
300 bps	FSK	300 baud	1080±100Hz 1750±100Hz	300Hz	Asynchronous (Full Duplex)	Fixed	V.21	103
1200	4-phase PSK	600	1200Hz 2400Hz	1200Hz	Synchronous/ Asynchronous (Full Duplex)		V.22	212
1200	FSK	1200	1700±400Hz	1200Hz	Asynchronous (Half Duplex)		V.23	202
2400	4-phase PSK	1200	1800Hz	1200Hz (3dB down)	Synchrouns (Half Duplex)		V.26 V.26 bis	201
4800	8-phase PSK	1600	1800Hz	1600Hz (3dB down)		Automatic	V.27 V.27 bis V.27 ter	208
9600	16-phase QAM	2400	1700Hz	2400Hz (3dB down)			V.29	209

Note: In practice, the occupied bondwidth for 2400-9600 bps are as follows to improve the receiving performances.

2400 bps --- 2400Hz (100% Roll-off)
4800 bps --- 2400Hz (50% Roll-off)
9600 bps --- 2640Hz (10% Roll-off)

Table 1-2 Correspondence of Digital Data to Analog Value

FSK (300 bps)				4-phase PSK (1200 bps)				
MODE	Transmit Data bit	CCITT V.21	Bell 103	Carrier Frequency	Data bit pair	CCITT V.22		Bell 212A
						MODES 1-4	MODE 5	
ORIGINATE	Mark "1"	980Hz	1270Hz	2400Hz 1200Hz	0 0	90°	270°	90°
	Space "0"	1180Hz	1070Hz		0 1	0°	180°	0°
ANSWER	Mark "1"	1650Hz	2225Hz		1 0	180°	0°	180°
	Space "0"	1850Hz	2025Hz		1 1	270°	90°	270°

IV

2. MODEM DESIGN AND OPERATION

1) Modem design

Illustrated here is a modem designed with MSM6946.
A block diagram of modem is shown in Figure 2-1.
It is provided with an automatic answering function in addition to basic functions. The automatic answering function performs ringing signal detection, control logic operation, and dc loop current control.

Figure 2-2 shows an elementary circuit design using MSM6946, and Table 2-1 is a parts list.

U2 is a dual operational amplifier, and provides an interface circuit with the telephone line.

U3 and U4 are level converters. They perform mutual conversions of the TTL level to and from the ±12V level required for RS-232C.

U5 is used to drive indicators showing four statuses (power ON, carrier detect, received data, transmit data).

There are five switches in the circuit. SW1 is a power switch; SW2 is an originate (calling) mode/answer (called) mode selector switch; SW3 is used to turn the modem into a (remote) digital loopback mode, in which the transmit data (XD) and the request to send ($\overline{RS1}$) are looped back to the received data (RD) and the clear to send ($\overline{CS}$) respectively, and at the same time the serial data obtained by demodulating of the received FSK signal is input to the transmitter as a transmit data within the chip, subjected to FSK modulation and sent back to the telephone line; SW4 is used to switch the telephone line to either the telephone handset or the transformer for modem operation; and SW5 is used to enable the automatic answering mode.

LED comes alight when both the established call connection and off-hook states are detected.

U6 is a photo coupler used to detect a ringing signal, and protects the modem circuit from surge voltages which may appear in the telephone line.

U7 is used for dc loop current control.

U8 is a dual D type flip-flop; one half is used to latch the dc loop current control signal, and another half to latch the data for which the off-state of the received carrier is detected.

IV

U9 is a dual one-shot multivibrator, which is used to squelch the modem output for about 2 seconds (billing delay) necessary in the automatic answering and call connecting sequence and also to provide a sequence to turn off DSR (off-hook) and cut off the dc loop when the received carrier is not detected in about 10 seconds after connection of the modem to the telephone line.

U10 is a quad two input AND gate used in the automatic answering control circuit.

U11 is a dual one-shot multivibrators, one half is a 0.1-sec retriggerable one-shot that is part of the ring detect circuit, while the other half is a 0.1-sec one-shot that is used to clear the latch to disconnect the telephone line.

Figure 2-2 shows a modem directly connected to a telephone line. Note that the illustrated scheme is not approved by the authority for the purpose of test or development. A typical direct connection scheme (called DAA — direct access arrangement) is shown in Figure 2-3.

2) Modem operation

In case of manual calling, the modem is placed in the originate and voice mode (telephone line connected to the telephone handset), and a call is made using the telephone handset.

When an answer is detected (i.e. an answer mark tone is heard), the modem is placed in the data mode (the telephone line connected to the modem), and the indicator will light up showning that a carrier signal from the answering modem is received.

In the automatic answering mode, the modem is required to follow the procedures before starting transmission and reception. The following shows a call establishment sequence. See Figure 2-4.

(1) A call is placed to remote modem.

(2) Ringing is detected at answering end.

(3) Answering modem enables DSR and goes off-hook upon completion of ringing.

(4) Answering modem waits two seconds for billing delay.

(5) Then, the transmitter is turned on, and an answer mode mark tone (2225 Hz) is sent forward toward the originating modem.

(6) The mark answer tone is received by the originating modem and the originating modem is placed in a data mode where DSR is enabled.

(7) At the originating modem, CD (carrier detect) is turned on after a carrier detect on-delay time.

(8) Then, the originating modem releases the squelch for the transmitter, initiates the transmission of mark tone in the originate mode, and starts counting CS (clear to send) delay time. (Data transmit state is not yet achieved here).

(9) Upon reception of the mark tone (1270 Hz) from the originating modem, the answering modem turns on CD after a carrier detect on-delay time.

(10) Then, CS is turned on, enabling the answering modem to start data communication.

(11) The originating modem enters into a data communication state after a CS delay time.

In the automatic answering mode, the call connection is aborted when no response is obtained within a specified time or when the received carrier is lost for more than a specified time.

A power supply for the modem is easily available with an AC adaptor for stepping down 100 Vac to 12 Vac.
In Figure 2-2, three power supplies (+12V, -12V and +5V) are used. The -12V power supply is used for the level converter only, and can be dispensed with if the modem is to be connected to a computer via UART.

One of the most important performances of the modem is the bit error rate, which represents the ratio of number of error bit to the total number of data bit. The bit error rate is measured using the test circuit illustrated in Figure 2-5 and the S/N ratio as a parameter defined at the receiver input.

A transmit data in a 511 bit pseudo-random bit pattern is applied to the transmitter to generate an FSK signal. The signal is added with noise from a white noise source via attenuators, and is connected to the received signal input terminal of the modem to be measured.

The noise level (N) is usually measured through a voice frequency band-pass filter (BPF) to determine an S/N ratio.

The bit error rate is determined by comparing transmitted data and received data with each other and by counting the error bit in the serial received data stream.

An example of measured bit error rate characteristics is shown in Figure 2-6.

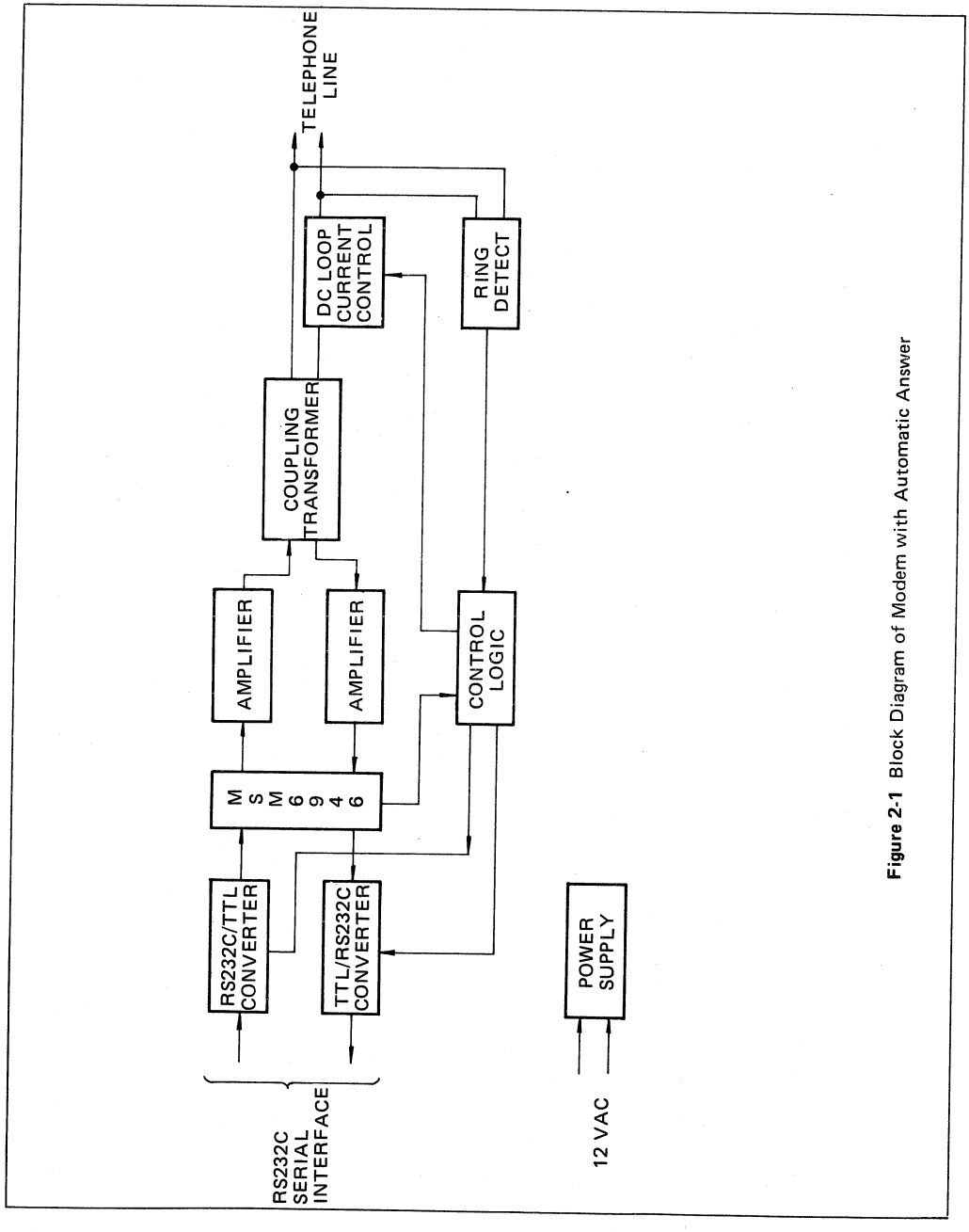


Figure 2-1 Block Diagram of Modem with Automatic Answer

Table 2-1 Parts Table for Figure 2-2

U_1	MSM6946RS	U_6	4N25	$V_{1,2}$	V39Z
U_2	LM747CN HA17458PS	U_7	RRD51A05(D)	T	TAMURA SEISAKUSHO DP101
U_3	DS1488N SN75188 HD75188	U_8	MM74C74	$Z_1 \sim_4$	IN5242
U_4	DS1489N SN75189 HD75189	$U_{9,11}$	CD4538BC MSM4538RS	Z_5	IN5231
U_5	CD4049C MSM4049RS	U_{10}	MM74C08 MSM4081RS	CRYSTAL	KINSEKI HC-43/U

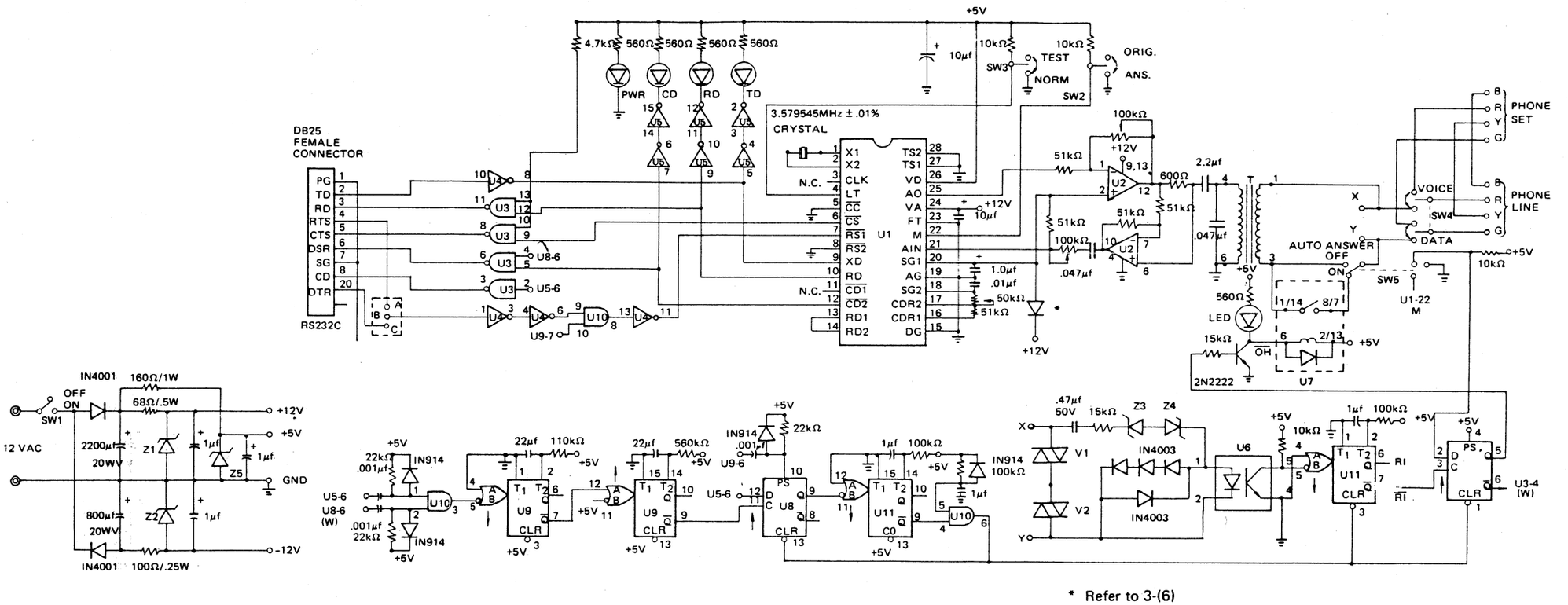


Figure 2-2 An Circuit Design Using Single-Chip Modem (with Automatic Answer)

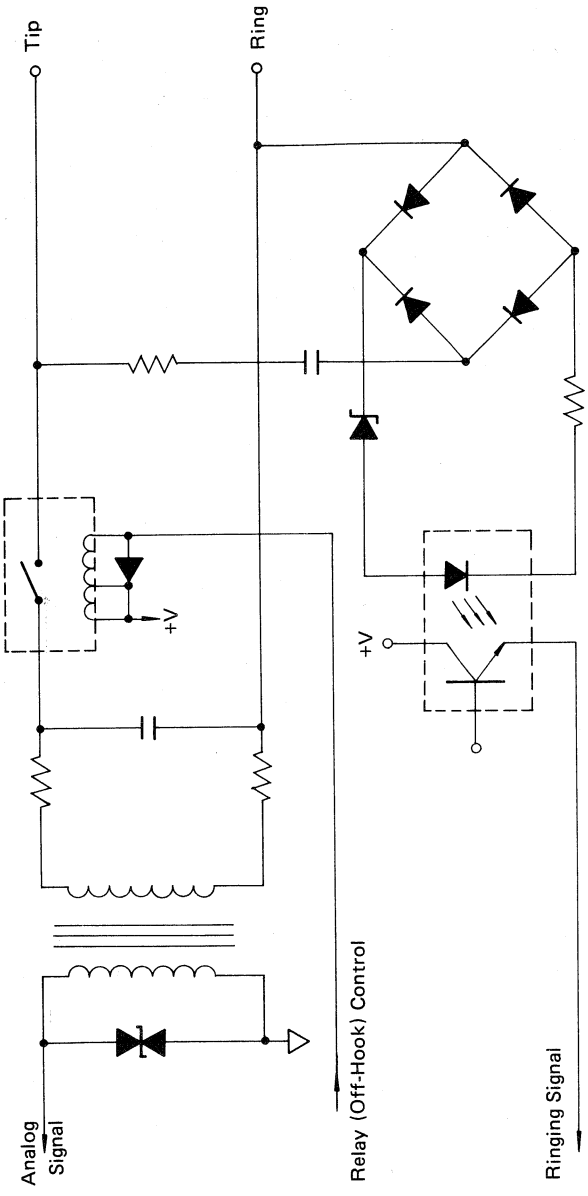


Figure 2-3 A Schematic Diagram of a Typical DAA

IV

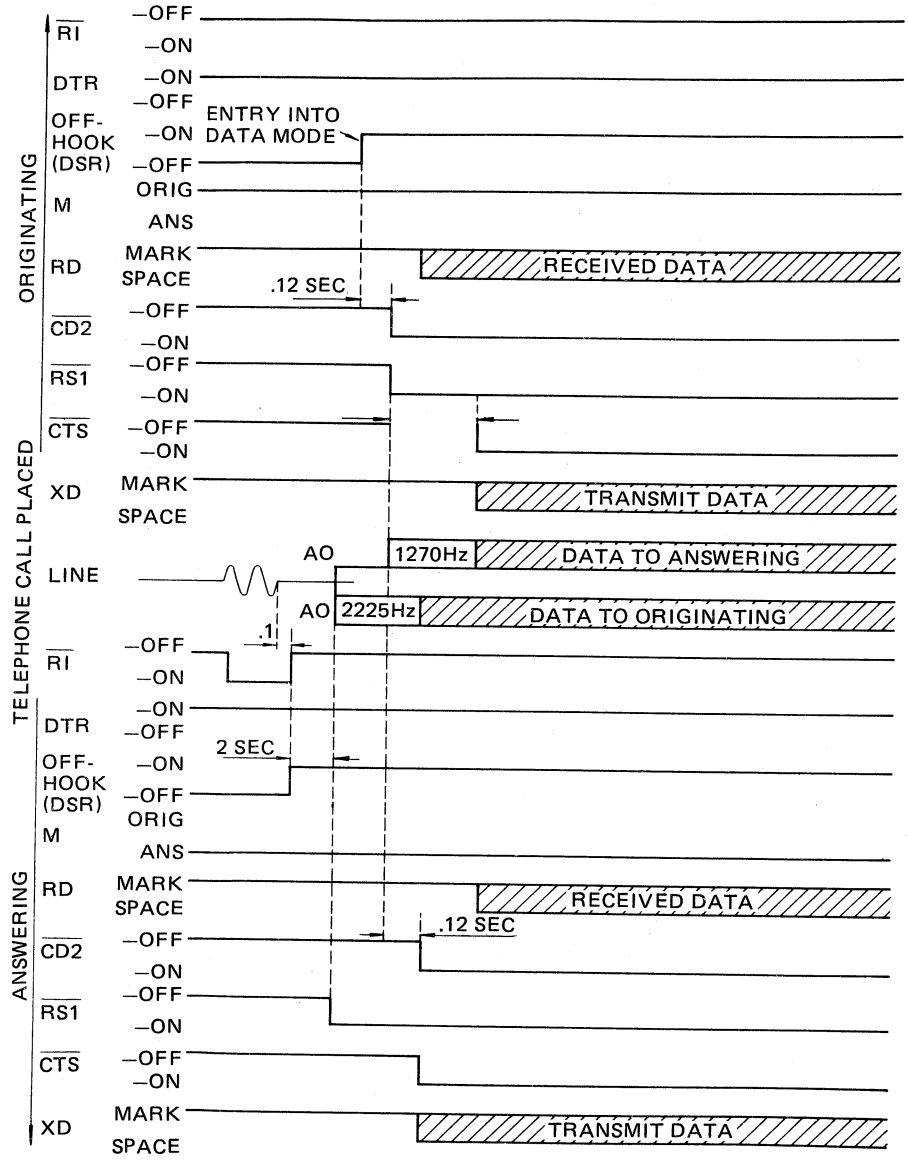


Figure 2-4 Call Establishment Sequence with Automatic Answer

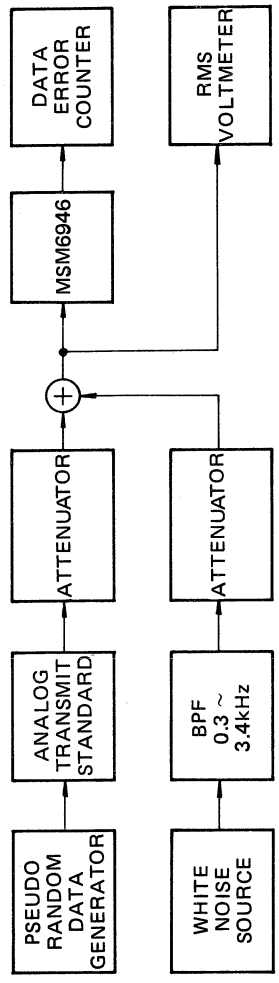


Figure 2-5 Modem Test Set

IV

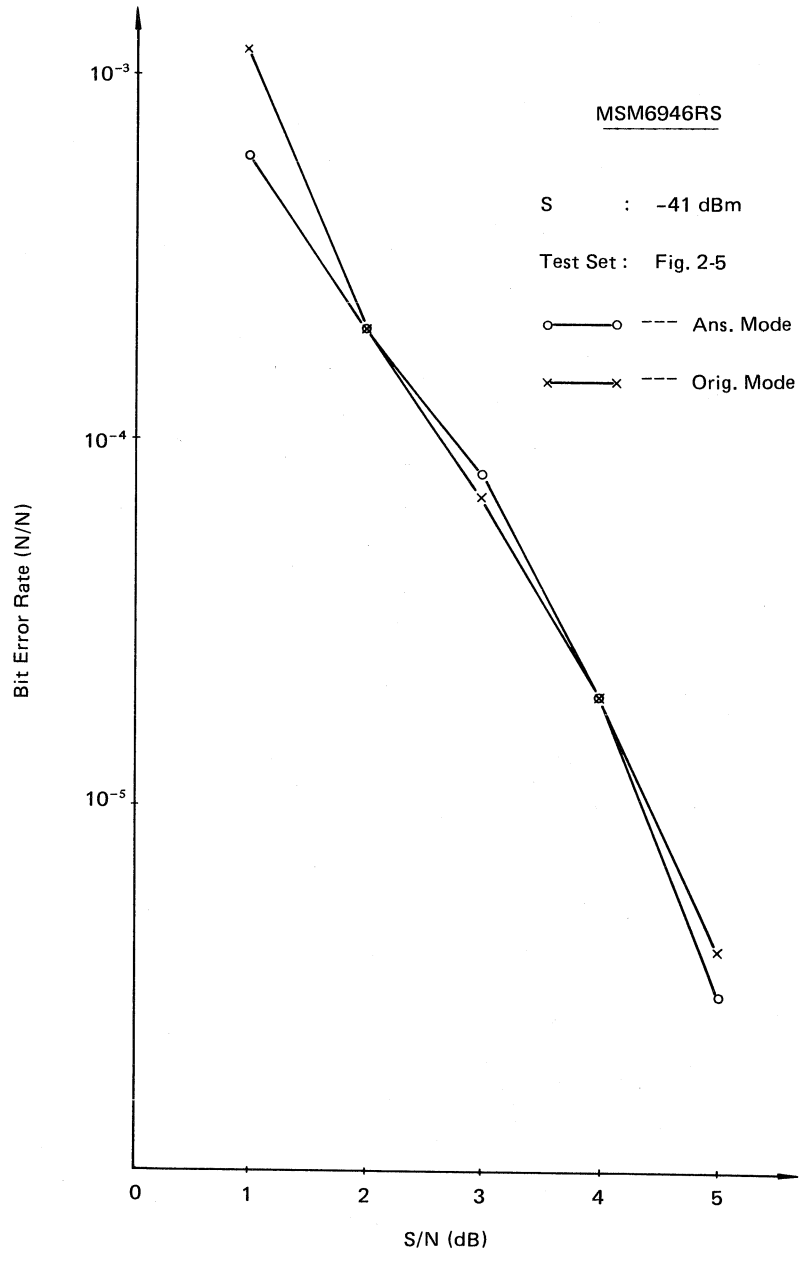


Figure 2-6 Measured Bit Error Rate Characteristics

APPENDIX

<Standard interface, and the control of modems used for public switched network>

Table 2-2 shows typical interface circuit for usual low speed asynchronous full-duplex modem.

The clear-to-send signal is slightly different in meaning from modem to modem. In BELL 103, this signal means that a carrier signal from a remote modem is received; namely, that the transmission channel is in good working order. It is used synonymous with CD (carrier detect). On the other hand, when a half-duplex modem like a 1200 bps FSK modem is used on a public switched network at which the full-duplex communication is capable, the clear-to-send signal serves just as a delayed signal of the request-to-send.

In this case, the clear-to-send signal remains to be an indication that the data communication is likely to be capable. When applying a modem on a public switched network, interface circuits — data terminal ready (DTR) and ringing indicator (RI) — are necessary.

These two circuits plus carrier detect circuit (CD) are a minumum requisite to the control of public switched network by a modem.

These functions will be well understood when compared with the operating sequence of a usual telephone.

Usual telephone		Low-speed asynchronous full-duplex modem	
Ringing	⟷	(RI)	Ringing Indicator
Going off-hook	⟷	(DTR)	Data Terminal Ready ON
Response by far-end calling party	⟷	(CD)	Received Carrier Detect ON

The data terminal ready (DTR) shows a state that the modem is powered on, connected to the data transmission line, and is not in the test mode, and that it is ready to operate.

DTR is rarely used for asynchronous transmission in North America, but is used widely in Europe.

- Except from "Technical Aspects of Data Communication", written by John E. McNamara, the copyright is under Digital Equipment Corporation.

Interface Circuit		Function	Symbol In Fig. 2-2
EIA	CCIT		
AA	101	Protective Ground	PG
AB	102	Signal Ground	SG
BA	103	Transmitted Data	TD
BB	104	Received DATA	RD
CA	105	Request to Send	RTS
CB	106	Clear to Send	CTS
CC	107	Data Set Ready	DSR
CD	108/1	Connect Data Set to Line	DTR
	108/2	Data Terminal Ready	
CF	109	Received Line Signal Detector	CD
CE	125	RING Indicator	RI

Note 1: In the case of full-duplex modem used for public switched network, the request-to-send (RTS) circuit is usually unnecessary.

Note 2: Unless otherwise specified by the Post, Telephone and Telegraph Authority (PTT), the low speed asynchronous modem interface is enough with either CD or CTS circuit, whichever is available.

Note 3: Unless otherwise specified by the PTT, the modem interface with the minimum equipped functions need not to be provided with DSR circuit.

Table 2-2. Typical Interface Circuits for Low Speed Modem

3. HINTS AND PRECAUTIONS ON USE

Unlike to general-purpose memories and logical gates, the single-chip modem LSI is hard to use. For example ...

- Handling of analog quantity over a wide range of signal levels.
- Use of functions which defy standardization or common applications.
- Full use of the technology for switched capacitor whose characteristics are highly susceptible to deterioration due to power noise.

Accordingly, its use is accompanied by limitations and at the same time special know-how.
These are explained hereunder, and additional information will be published in due course.

Whenever designers look at an IC, most of them are too readily tempted to associate it with digital operations. As a result, they are liable to set its operating conditions in a rough manner. However, the LSI for this modem series has highly delicate functions which in the past have been implemented with discrete components or hybrid-ICs provided with adjust circuits or trimmers, and utmost attention should be paid to its using conditions so as to elicit its maximum performance.

1) Pin connections for MSM6926/6946/6927/6947

The following shows the terminals with different functions.

Device	Pin 22	Pin 27	Pin 28
MSM6926	M (Answer/Originate)	TS1 (Timer Selection)	TS2 (Timer Selection)
6946			
6927	$\overline{SQ}$ (2-Wire/4-Wire)		
6947		TS (Timer Selection)	$\overline{ATE}$ (Answer Tone)

Table 3-1. Different Pin Functions for 4-kind of Modem LSIs.

IV

The operating conditions are assumed as follows.

- Use of internal timers.
- 2-Wire use (as in the public switched network)

In this case, the differences in connection between the devices are as follows.

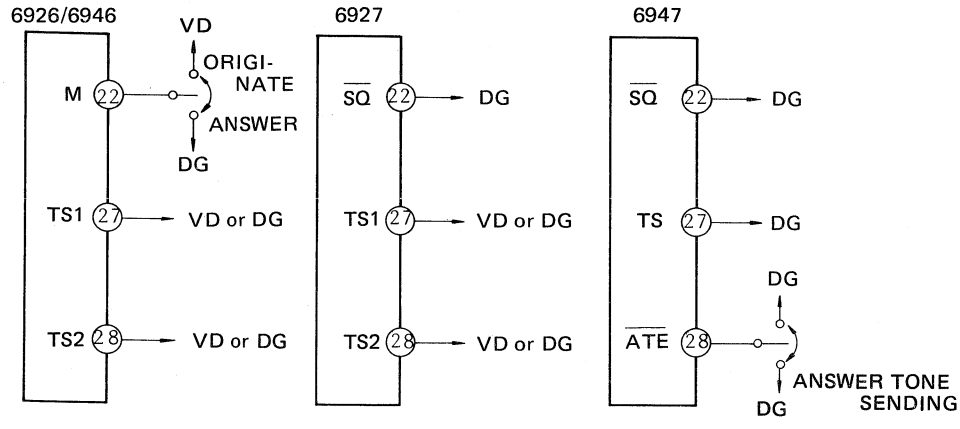


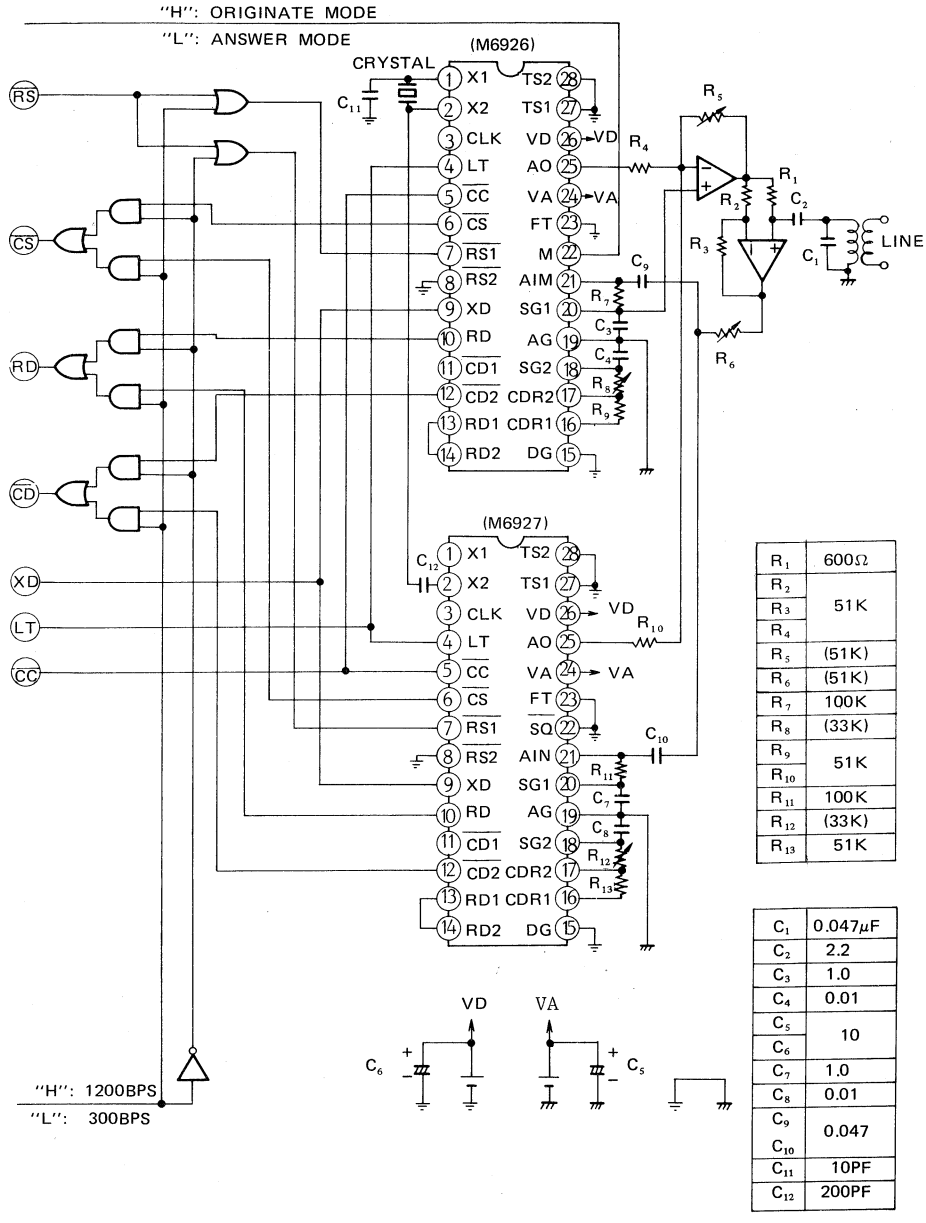
Figure 3-1 The Differences in Connection between the Devices

For other pins, the devices are used in the same manner.

IV

2) MSM6926 and MSM6927 for 2-speed operation

Figure 3-2 introduces a circuit employing a 6926 and a 6927 for 2-speed operation.



R_1	600Ω
R_2	51K
R_3	
R_4	
R_5	(51K)
R_6	(51K)
R_7	100K
R_8	(33K)
R_9	51K
R_{10}	
R_{11}	100K
R_{12}	(33K)
R_{13}	51K

C_1	0.047μF
C_2	2.2
C_3	1.0
C_4	0.01
C_5	10
C_6	
C_7	1.0
C_8	0.01
C_9	0.047
C_{10}	
C_{11}	10PF
C_{12}	200PF

Figure 3-2

3) Setting of the carrier detect level

In an single-chip modem LSI, the receive carrier detect ON and OFF levels can be set within the range of -43 to -48 dBm by adjusting the ratio of the external resistors R_8 and R_9.

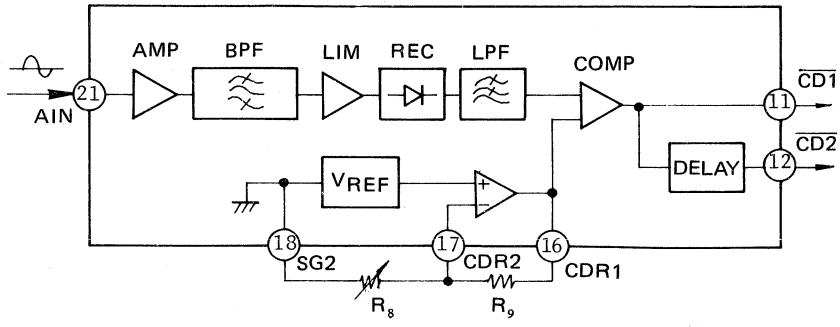


Figure 3-3

After adjustment, the voltage between Pin 16 (CDR1) and Pin 18 (SG2) will be about 3V. Since the input signal level refers to LSI Pin 21 (AIN) of the LSI, it may have to be amplified when attenuated by a line transformer, etc.

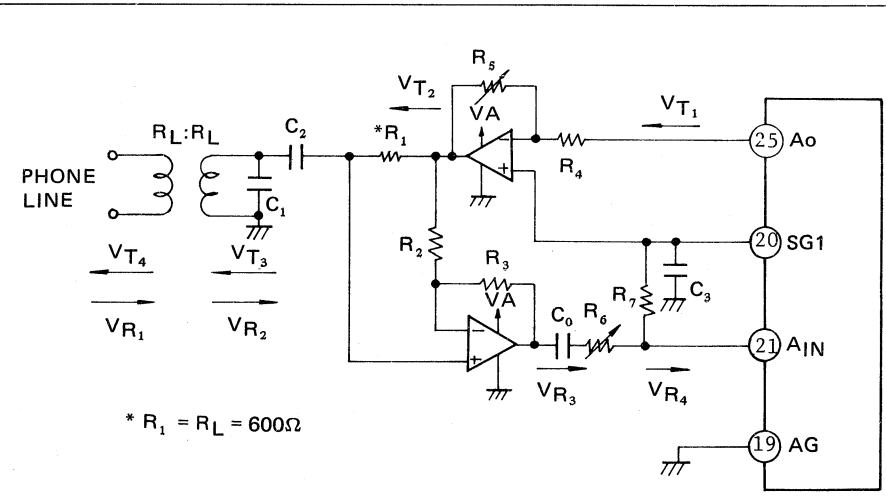
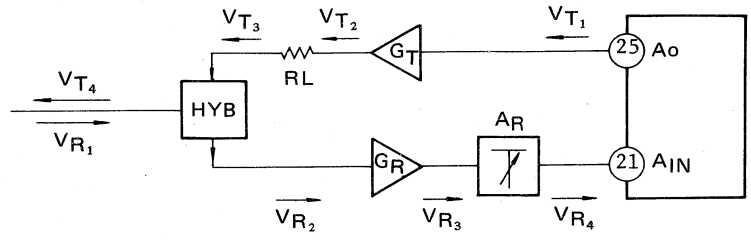


Figure 3-4

Figure 3-5 is a simplified drawing of Figure 3-4.

IV



G_R	$1+\frac{R_3}{R_2}$	2 ≡ +6 dB
A_R	$\frac{R_7}{R_6+R_7}$	1/2 ≡ -6 dB
G_T	$\frac{R_5}{R_4}$	1 ≡ 0 dB

Typical Design Values

Figure 3-5

Accordingly, if the loss across the line transformer is 0 dB, the following equation applies;

$$V_{R4} = V_{R1} \cdot G_R \cdot A_R = V_{R1}$$
$$V_{T4} = V_{T1} \cdot G_T \cdot 1/2 = V_{T1} - 6\,dB$$

If the maximum received signal level is -6 dBm, the level at AIN terminal is -6 dBm. The transmit level will be 0 dBm because it is attenuated by 6 dB by R_1 and the transformer impedance R_L (both 600 ohm).

If the line transformer produces a loss of 2 dB in both directions, it is required to reduce R_6 (from the typical value of 51 kohm to about 30 kohm) to compensate the received level at AIN.

Additionally in order to keep the transmit signal level at the typical value of 0 dBm, it is required to increase R_5 (from the typical value of 51 kohm to approx. 64 kohm).

Note:

$$20 \log \frac{R_7}{R_6' + R_7} = 20 \log \frac{51}{30 + 51} \simeq -4.0 \text{ dB} = (-6) + \underline{\underline{2 \text{ dB}}}$$

$$20 \log \frac{R_5'}{R_4} = 20 \log \frac{64}{51} = 2.0 \text{ dB} = (0) + \underline{\underline{2 \text{ dB}}}$$

If R_6 is fixed at the typical value of 51 kohm, and if the line transformer causes a 2 dB loss, the received signal level of -6 to -48 dBm is shifted by 2 dB to -8 to -50 dBm at AIN terminal. It is therefore only required to lower the carrier detection level (by increasing R_8 from the typical value of 33 kohm to 51 kohm) by 2 dB.

In this case, the maximum received signal level at AIN is -8 dBm, and the carrier detect ON/OFF level is within the range of -45 to -50 dBm. This method, however is not recommendable because the S/N ratio will be slightly deteriorated. Anyway, operation is possible, although hysteresis width, etc. cannot be warranted. It should also be noted that the carrier detect ON delay time becomes longer and the OFF delay time shorter.

4) Transmission and reception timing

The operation timing is shown below.

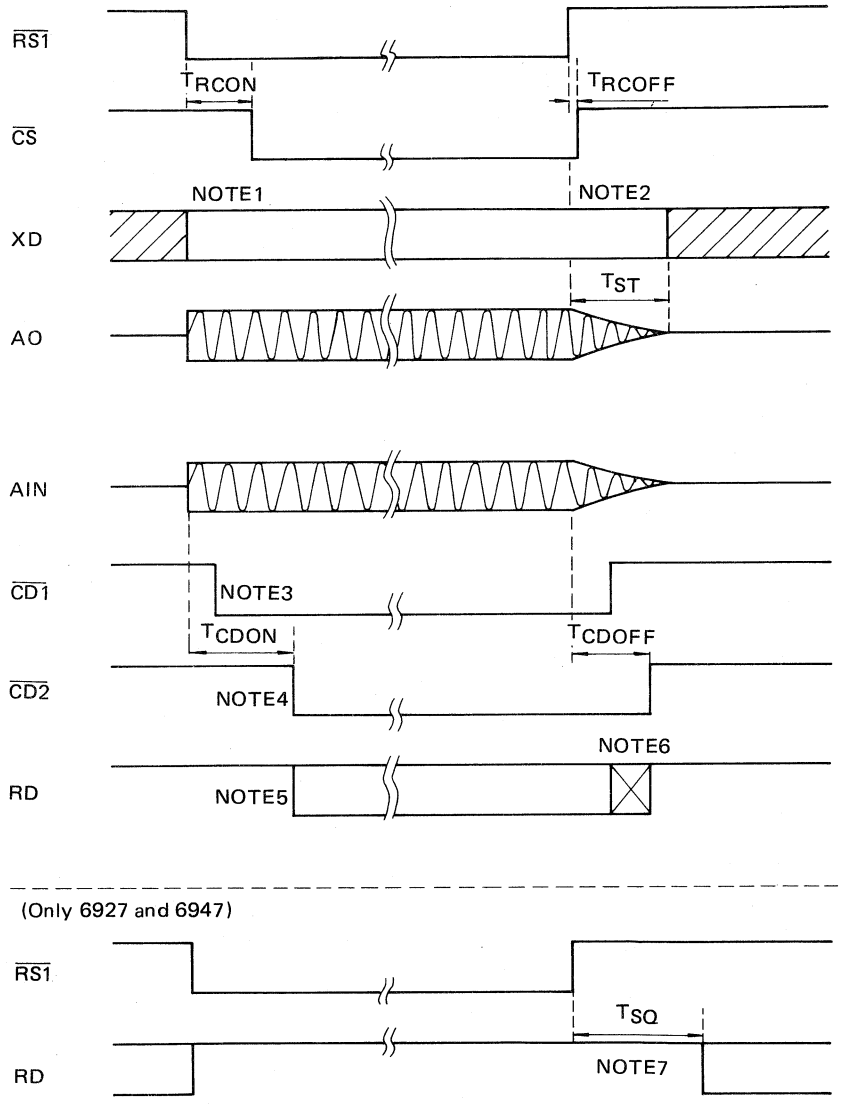


Figure 3-6 Timing Waveform Chart

Note 1: From the time when $\overline{RS1}$ has become "L", a modulated waveform is generated at $\overline{AO}$ in accordance with "H" or "L" at XD.

Note 2: Even when $\overline{RS1}$ has attained "H", the modulated waveform maintains at $\overline{AO}$ during the soft turn-off period (T_{ST}) in accordance with "H" or "L" at XD, while its amplitude gradually attenuates.

Note 3: $\overline{CD1}$ is the terminal where the carrier detect signal is output without logical delay.

The ON and OFF delay times at $\overline{CD1}$ change depending on the received signal level (AIN) and the differential voltage of the comparator in the detection circuit (VR =CDR1 terminal voltage – SG2 terminal voltage), etc. This is the reason for which the response characteristics of analog reception filter, limiter and carrier detector are significant factors. Typical characteristics are shown in Figure 3-7 through 3-10.

Note 4: $\overline{CD2}$ is the terminal where the output carrier detect signal is logically delayed by the internal delay circuit. The delay time provided by the internal delay circuit depends on the clock frequency, and is stable. Typical delay times are shown in Table 3-3.

T_{CDON} and T_{CDOFF} values are indicated in Figure 3-7 through 3-10 and Table 3-3.

Note 5: When $\overline{CD2}$ is "H", RD is hold at "H" level (Mark hold).

Note 6: When the input level decreases after $\overline{CD1}$ goes "H" and the carrier detect circuit turned off, the demodulator will stop its operation.

During the period from the suspension of demodulation to the point of time when $\overline{CD2}$ becomes "H", the RD output becomes "H" in case of MSM6926, 6927 and 6947, and "L" in case of MSM6946 respectively.

Note 7: MSM6927 and MSM6947 has a built-in receive squelch delay timer, which is enabled by setting SQ terminal to "L". (It is used for the 2-Wire communication).

During transmission in the half-duplex mode ($\overline{RS1}$ = "L"), RD and $\overline{CD2}$ are fixed at "H", and even after $\overline{RS1}$ changes to "H", RD and $\overline{CD2}$ are kept at "H" during the squelch time (T_{SQ}) to avoid data errors in the demodulated data stream due to transient response at the time of sudden cut-off transmit signal. Table 3-4 shows the actual measurements.

MSM6926

TS2	TS1	T_{RC} ON	T_{RC} OFF
0	0	402 ms	0.2 μs
0	1	30 ms	0.2 μs
1	0	350 ms	0.2 μs
1	1	External	External

MSM6927

TS2	TS1	T_{RC} ON	T_{RC} OFF
0	0	201 ms	0.3 μs
0	1	29 ms	0.3 μs
1	0	73 ms	0.2 μs
1	1	External	External

MSM6946

TS2	TS1	T_{RC} ON	T_{RC} OFF
0		198 ms	0.2 μs
1		External	External

MSM6947

TS	T_{RC} ON	T_{RC} OFF
0	180 ms	0.2 μs
1	External	External

Table 3-2. RS/CS Timing Measurement by Devices ($\overline{RS1} \rightarrow \overline{CS}$)

MSM6926

TS2	TS1	$\overline{CD2}$/ON	$\overline{CD2}$/OFF
0	0	301 ms	21 ms
0	1	4 ms	21 ms
1	0	152 ms	4 ms
1	1	External	External

MSM6927

TS2	TS1	$\overline{CD2}$/ON	$\overline{CD2}$/OFF
0	0	7.5 ms	5.2 ms
0	1	7.5 ms	5.2 ms
1	0	7.5 ms	5.2 ms
1	1	External	External

MSM6946

TS2	TS1	$\overline{CD2}$/ON	$\overline{CD2}$/OFF
0		102 ms	8 ms
1		External	External

MSM6947

TS	$\overline{CD2}$/ON	$\overline{CD2}$/OFF
0	14.5 ms	9.9 ms
1	External	External

Table 3-3. CD Timing Measurements by Devices ($\overline{CD1} \rightarrow \overline{CD2}$)

MSM6927

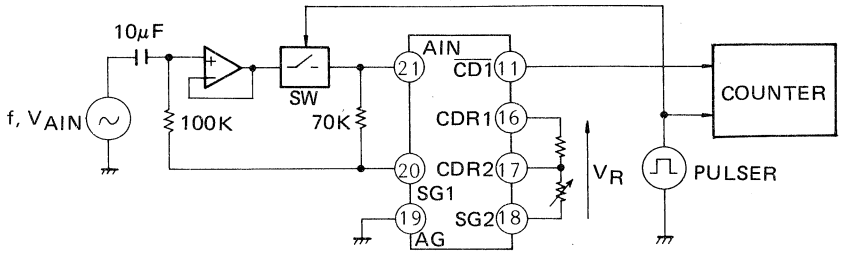
$\overline{SQ}$	TS2	TS1	TSQ
0	0	0	150 ms
0	0	1	150 ms
0	1	0	40 ms

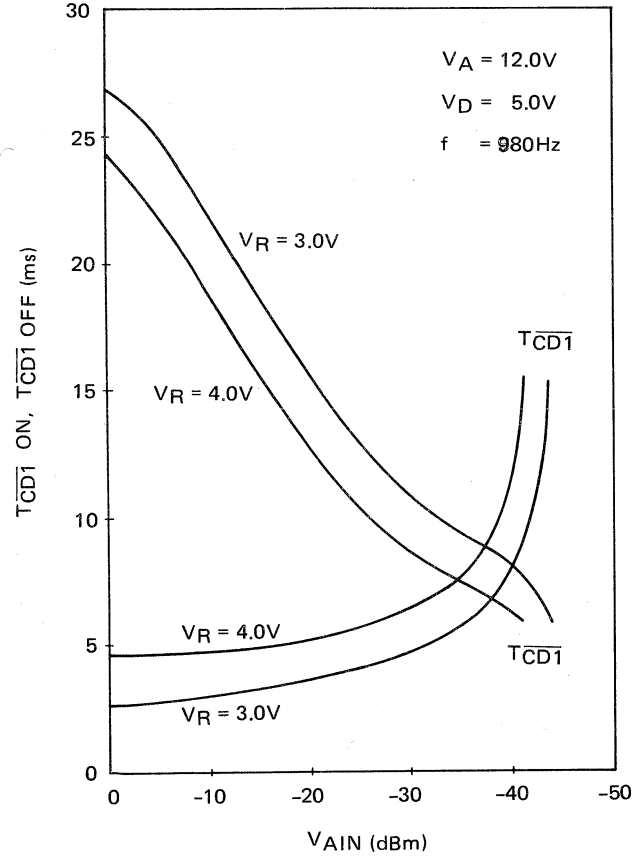
MSM6947

$\overline{SQ}$	TS	TSQ
0	0	151 ms

Table 3-4. MSM6927/6947 Received Data Squelch Delay Timing Measurements

Measuring Circuit





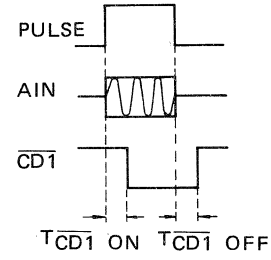


Figure 3-7 MSM6926 $\overline{CD1}$ Delay Time Characteristics

IV

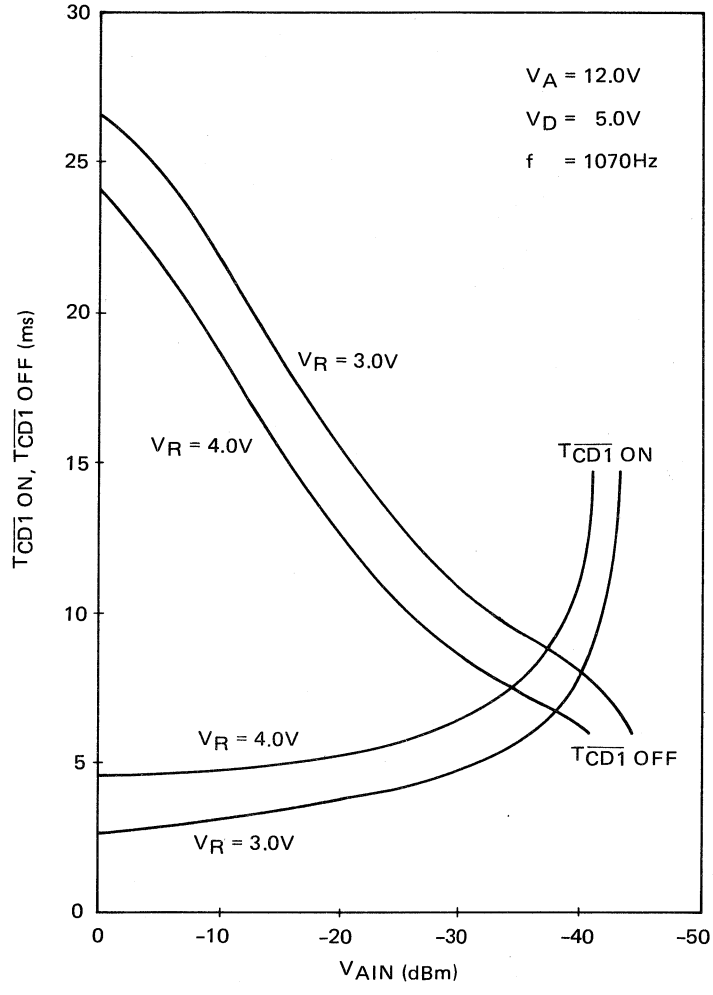


Figure 3-8 MSM6946 $\overline{CD1}$ Delay Time Characteristics

IV

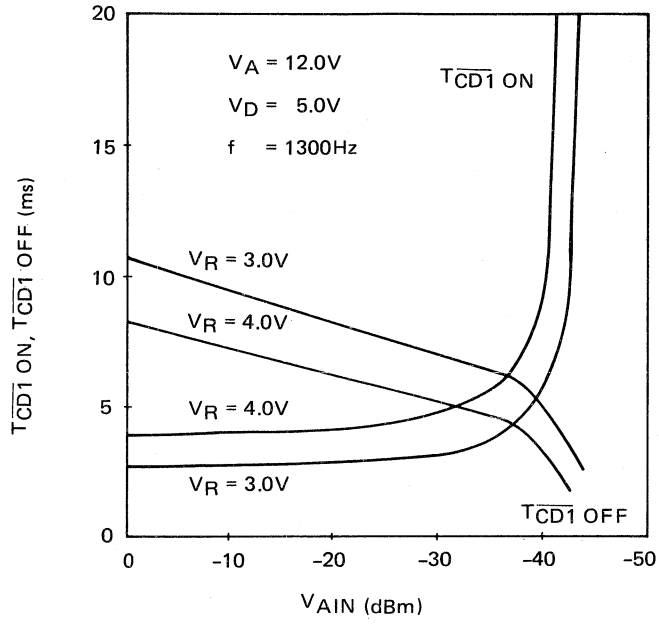


Figure 3-9 MSM6927 $\overline{CD1}$ Delay Time Characteristics

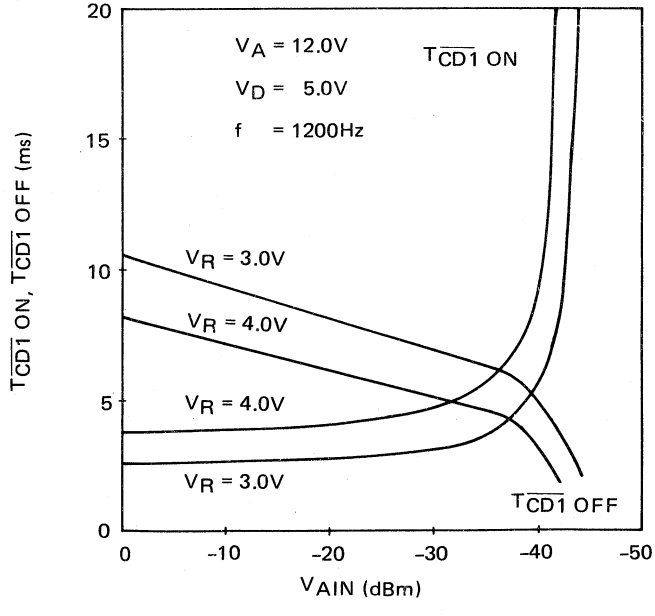


Figure 3-10 MSM6947 $\overline{CD1}$ Delay Time Characteristics

IV

5) A simple configuration example of external timer

The external timers shown in the data sheet have many gates. For a simple configuration of a timer circuit, refer to Figures 3-11 and 3-12. When using MSM6926, 6946 or 6927, apply an "H" level to TS1 (Pin 27) and TS2 (Pin 28). When using MSM6947, apply an "H" level to TS (Pin 27). In this mode, external timer circuits can be added.

a) 300BPS (MSM6926/6946)

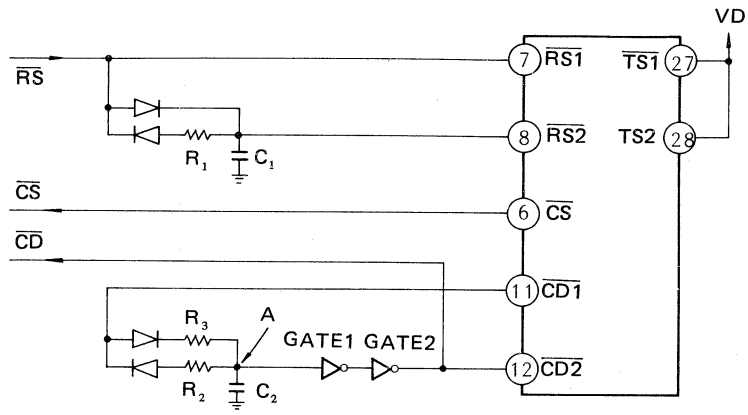
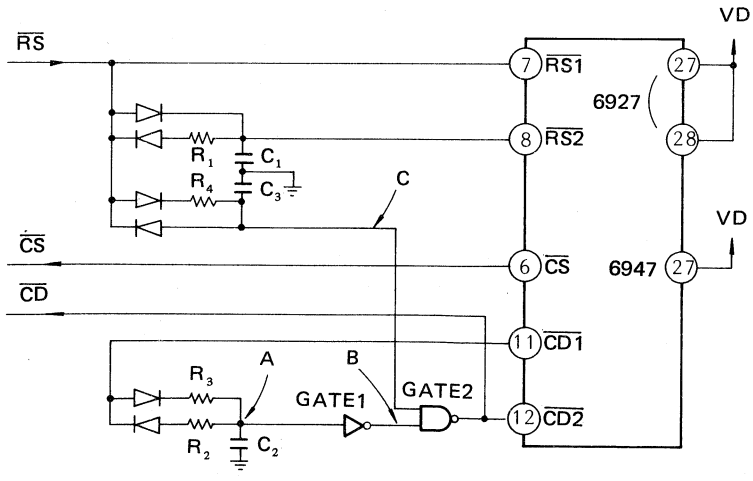


Figure 3-11

b) 1200PBS (MSM6927/6947) – 2-Wire circuit

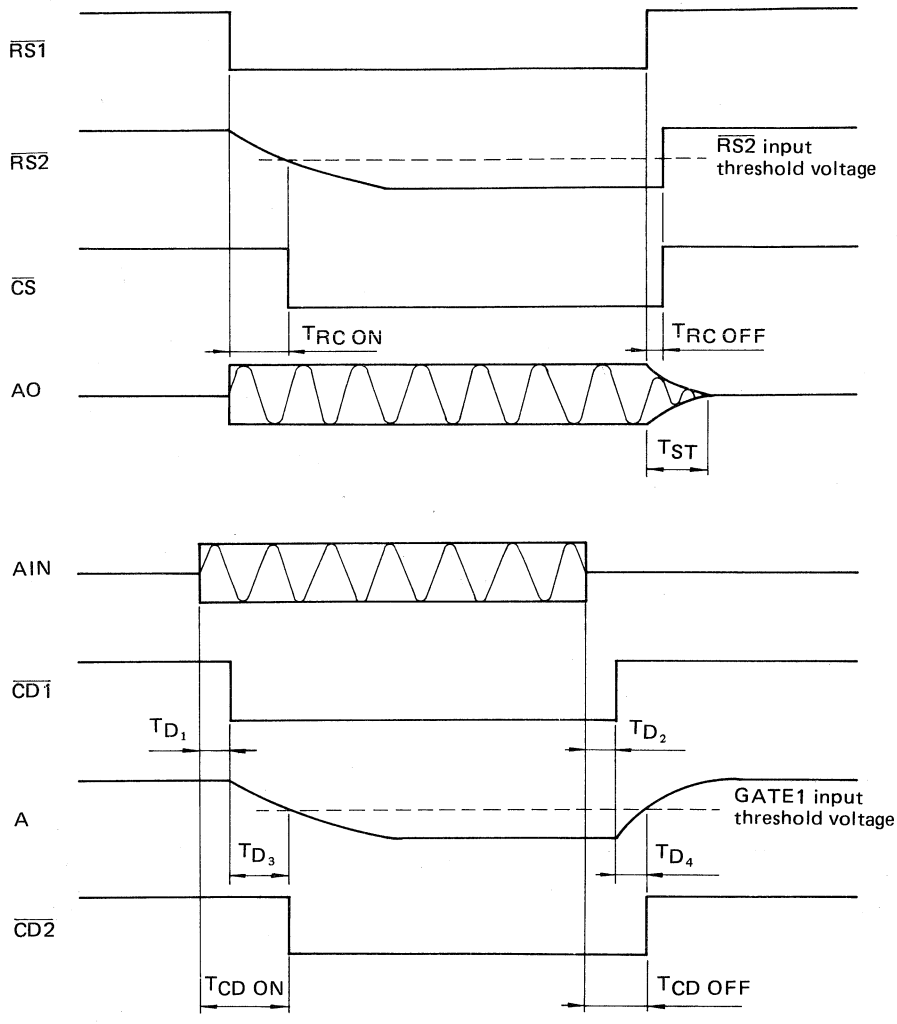


Note: Same as (a) in case of 4-Wire circuit

Figure 3-12

IV

c) MSM6926/6946 Timing Chart



NOTE 1: Transmission and reception are perfectly independent from each other.

NOTE 2: $T_{RC\ ON} \propto R_1 \cdot C_1$, depends also on $\overline{RS2}$ input threshold voltage.

$T_{RC\ OFF} \simeq 0$

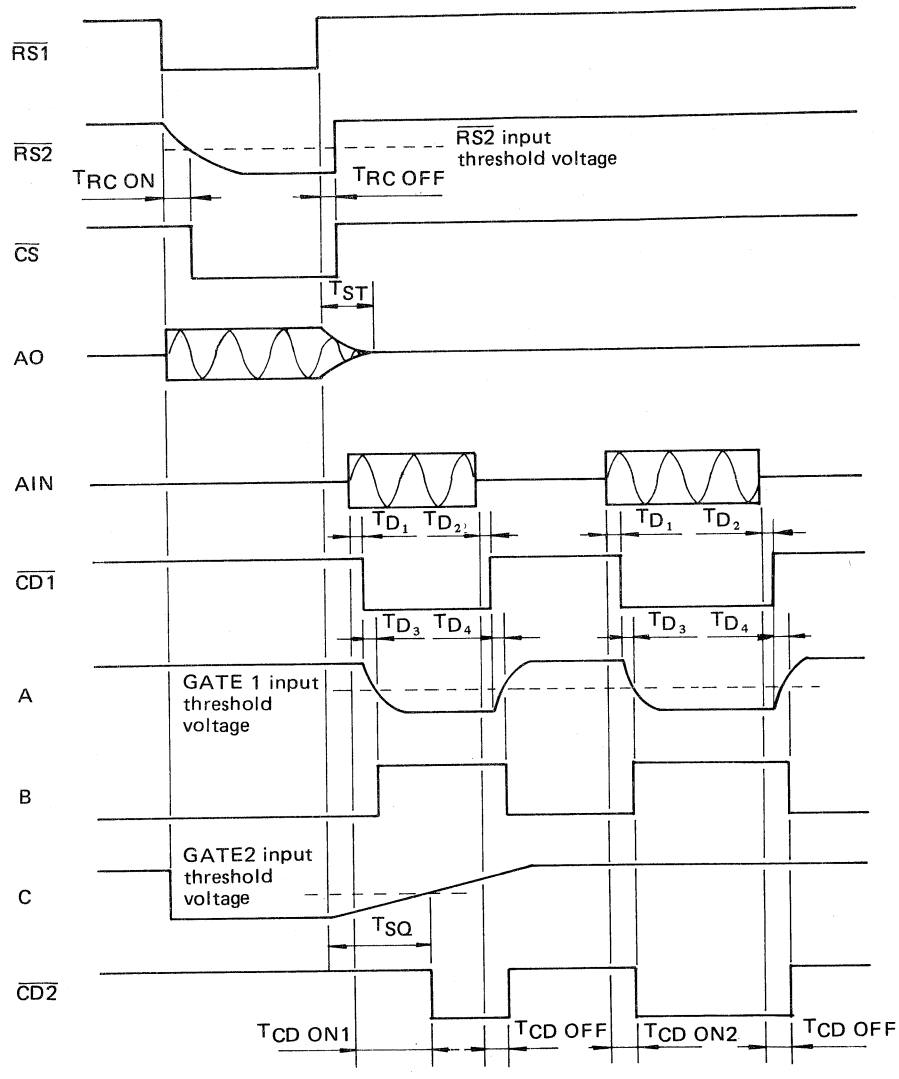
T_{D_1}, T_{D_2}: depend on the transient response of analog circuits such as reception filter, especially on the received signal level.

$T_{D_3} \propto R_2 \cdot C_2$, $T_{D_4} \propto R_3 \cdot C_2$, both depend on the threshold voltage at Gate1 input.

$T_{CD\ ON} = T_{D_1} + T_{D_3}$, $T_{CD\ OFF} = T_{D_2} + T_{D_4}$

Figure 3-13

d) MSM6927/6947 Timing Chart (2-Wire facilities)



NOTE: $T_{RC\ ON} \propto R_1 \cdot C_1$, depends on $\overline{RS2}$ input threshold voltage.

$T_{RC\ OFF} \fallingdotseq 0$

T_{D_1}, T_{D_2}, depend on the transient response of analog circuits such as reception filter, especially on the received signal level.

$T_{D_3} \propto R_2 \cdot C_2$, $T_{D_4} \propto R_3 \cdot C_2$, both depend on GATE1 input threshold voltage.

$T_{SQ} \propto R_4 \cdot C_3$, depends on GATE2 input threshold voltage.

$T_{CD\ ON_2} = T_{D_1} + T_{D_3}$, $T_{CD\ OFF} = T_{D_2} + T_{D_4}$.

Figure 3-14

IV

6) Circuit to prevent latch-up due to power supply noise

The LSIs for single chip modem series have a high immunity against latch-up, but are vulnerable against severe noise in the power supply.

Add a diode as illustrated in Figure 3-15.
For best protection, provide a zener diode (~15V) and a choke coil.

There is no restriction in whether to apply the 12V source or 5V source first.

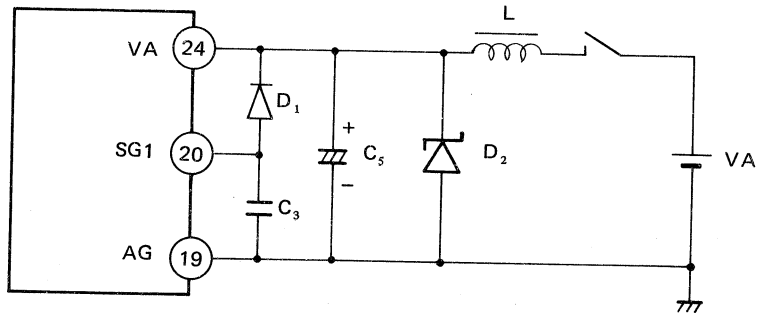


Figure 3-15

7) How to apply clock pulses

a) Clock circuit when two one-chip modems are used

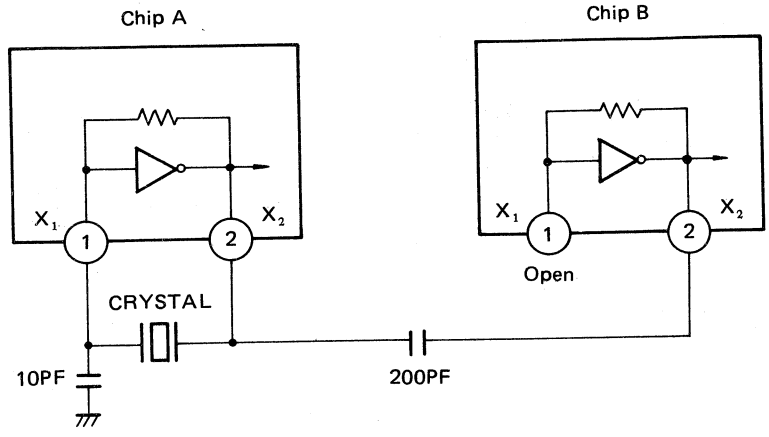


Figure 3-16

b) How to use an external clock circuit

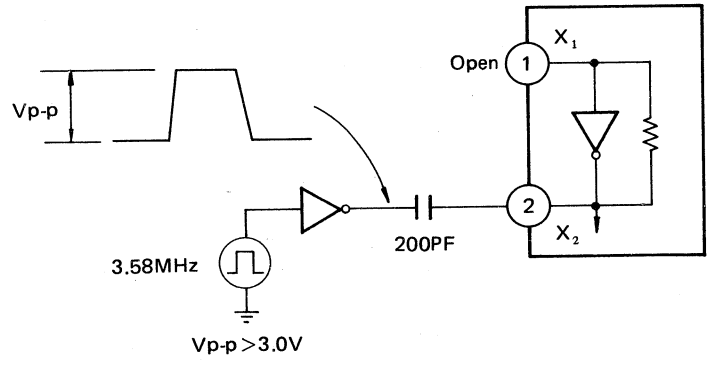


Figure 3-17

IV

8) Line equalization circuit for 1200 bps FSK modem

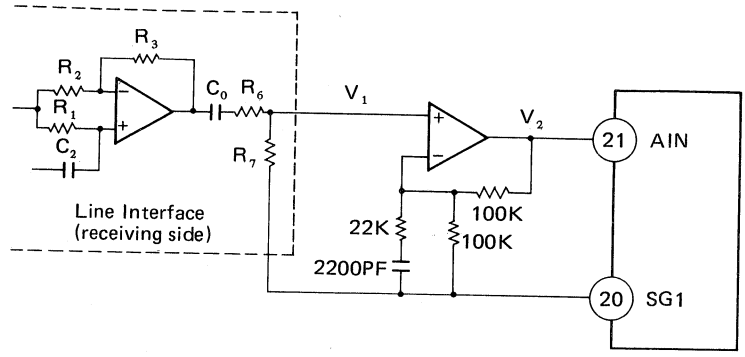


Figure 3-18 An Example of Line Equalization Circuit

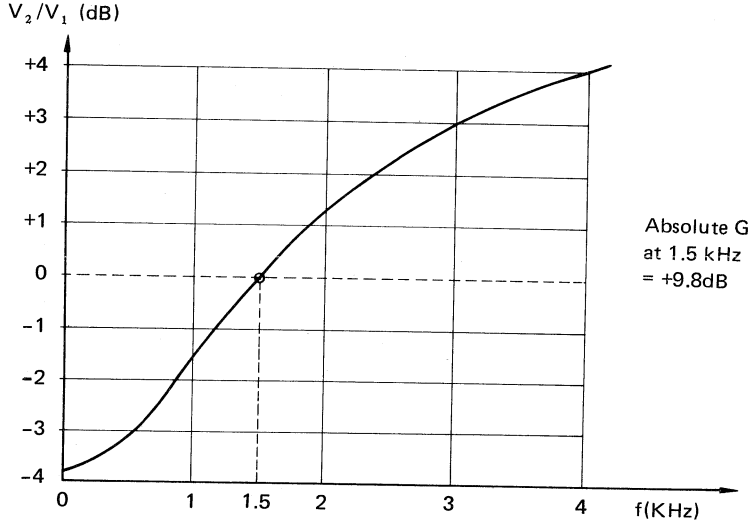


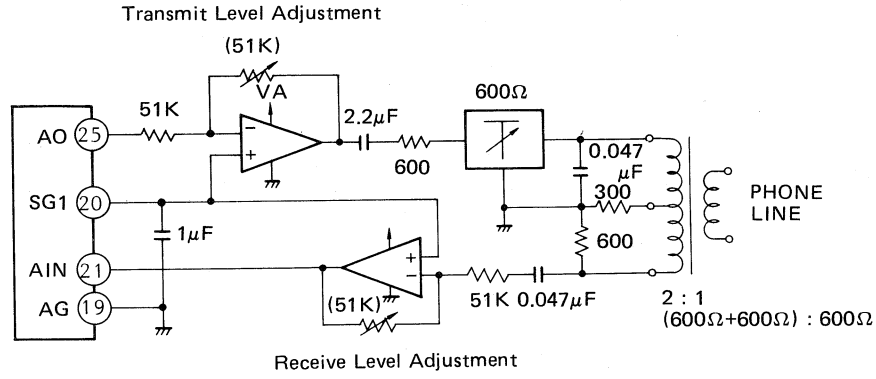
Figure 3-19 Frequency Characteristics of Line Equalization Circuit

The line equalization circuit shown in Figure 3-18 has a gain of +9.8 dB at 1.5 kHz. The input level at AIN terminal is adjusted by varying R_6 and R7, which have a typical value of 51 kohms. R_6 is set at 91 kohms, and R_7 at 15 kohms respectively. ($R_7/R_6 + R_7$) ≒ 1/7)

This line equalization circuit can also be used on the transmitting side, but its frequency characteristics should be selected case by case.

9) Circuit interfacing using a variable analog attenuator

a) In case of hybrid transformer.



NOTE 1: AIN signal level should not exceed -6dBm.

NOTE 2: The value of resistors and capacitors are recommended values.

Figure 3-20 Circuit Using an Attenuator (No. 1)

b) In case of a line transformer plus hybrid circuit consisting of resistors and OP amps.

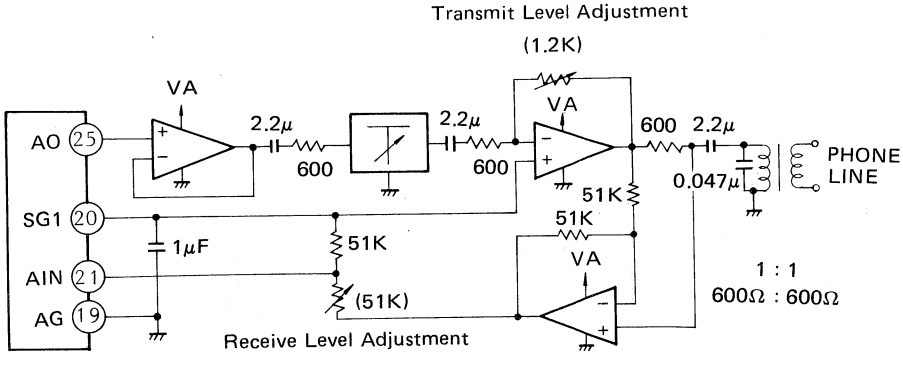


Figure 3-21 Circuit Using an Attenuator (No. 2)

IV

c) 1200 bps 2-Wire half-duplex communication

In this case, transmission and reception are not carried out simultaneously, the circuit becomes simpler than that compared with a) and b).

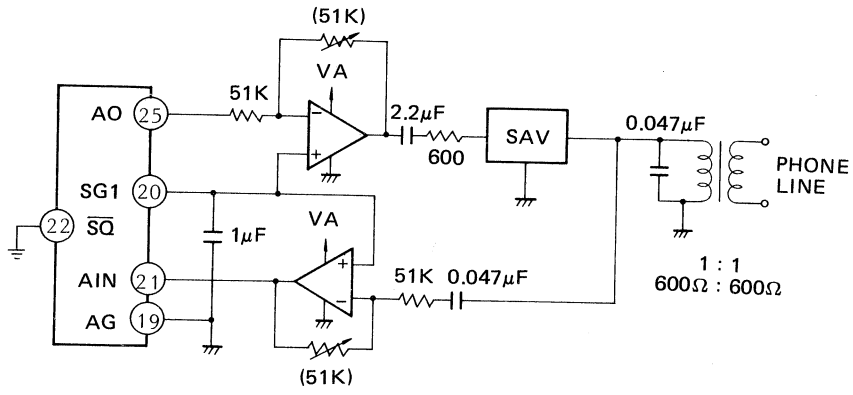


Figure 3-22 Circuit Using an Attenuator (No. 3)

In 2-Wire operation, $\overline{SQ}$ (Pin 22) is set to digital "L".
Under this condition, when sending the transmission carrier ($\overline{RS1}$ = digital "0"), the carrier detection is disabled and the received data is held in the "mark" state, independent of the signal entering AIN (received analog signal input).

Reference

In the half-duplex oepration, the preceding hybrid circuit is unnecessary. The circuit using a variable analog attenuator has been shown in Figure 3-22, and a circuit without an attenuator is shown in Figure 3-23.

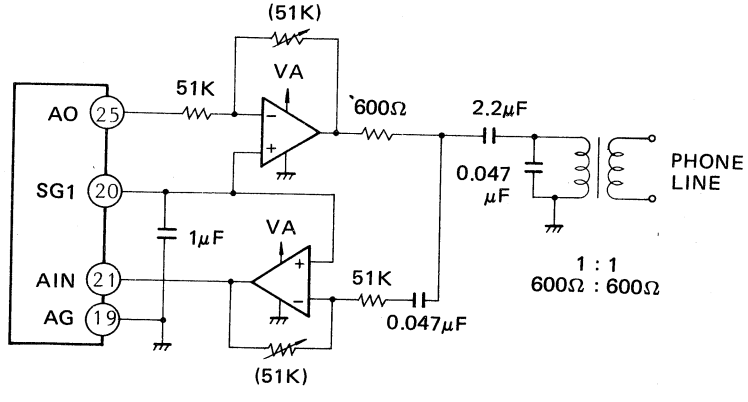


Figure 3-23 Line Interface Circuit for Half-duplex Operation

10) Deterioration of characteristics due to power supply noise

If both power supplies and particularly the VA supply contain noise, degraded characteristics are as follows.

1 Narrowing in the range of received signal levels
2 Narrowing of the hysteresis width of the carrier detect level
3 Increased bit error rate

There are two major reasons for these phenomena.

a) The internal signal ground is provided as a VA/2 potential.
Accordingly, half of the noise amplitude VN, superimposed on VA, appears on the signal ground, and IC internal analog signal processing is carried out with reference to SG1 (Pin 20) containing this $V_{N/2}$ noise.

Both the transmit and received signals are connected to the telephone line via a transformer. Usually, the transformer operates with reference to 0V, which is euqal to the potential of AG. Please refer to the circuit in figure 3-24.

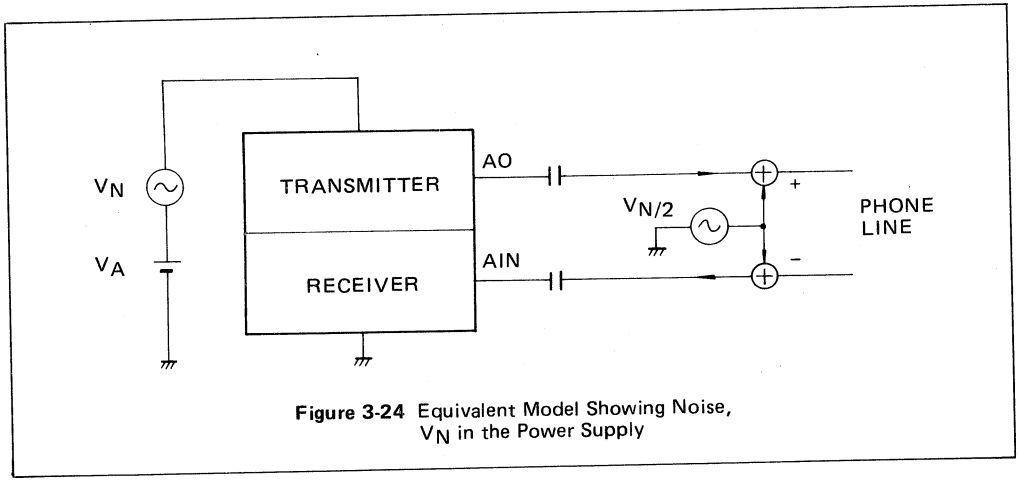


Figure 3-24 Equivalent Model Showing Noise, V_N in the Power Supply

b) Deterioration of characteristics due to crosstalk noise voltage from VA into the operational amplifier output, etc. via the power line of the operational amplifier and capacitor switches on the chip.

The problems do not only result in increase in noise level, but also the noise level in the voice band may be increased significantly because of the aliasing effect inherent in the switched capacitor method that plays a key role in the modem chip. The degree of deterioration in characteristics due to the combined appearance of noise and aliasing effect depends on the noise frequency, as demonstrated by the frequency characteristics in Figure 3-25 measured on MSM6926. In Figure 3-25, a sinusoidal noise voltage was superimposed on VA, and its levels (Vp-p) at which erroneous operations came up were measured and plotted. At around 1.5 to 2 kHz deterioration occurred, because that noise frequency band interfaces with the received carrier frequency band. The modem chip uses 56 kHz as a sampling clock signal for the switched capacitor filter, and it is found that the aliasing effect makes it liable for the erroneous operations caused with respect to the superimposed signals represented by nearly all multiples of the clock frequency.

It is therefore necessary to minimize VA noise through a bypass capacitor, etc. Noise superimposed on the digital circuit power supply, V_D (+5V), does not lead directly to this kind of deterioration. In the modem chip, however, analog and digital circuits are resident together, and noise on V_D may enter into the analog circuit via the reverse bias junction.

Accordingly, it is also important to reduce the noise level at V_D.

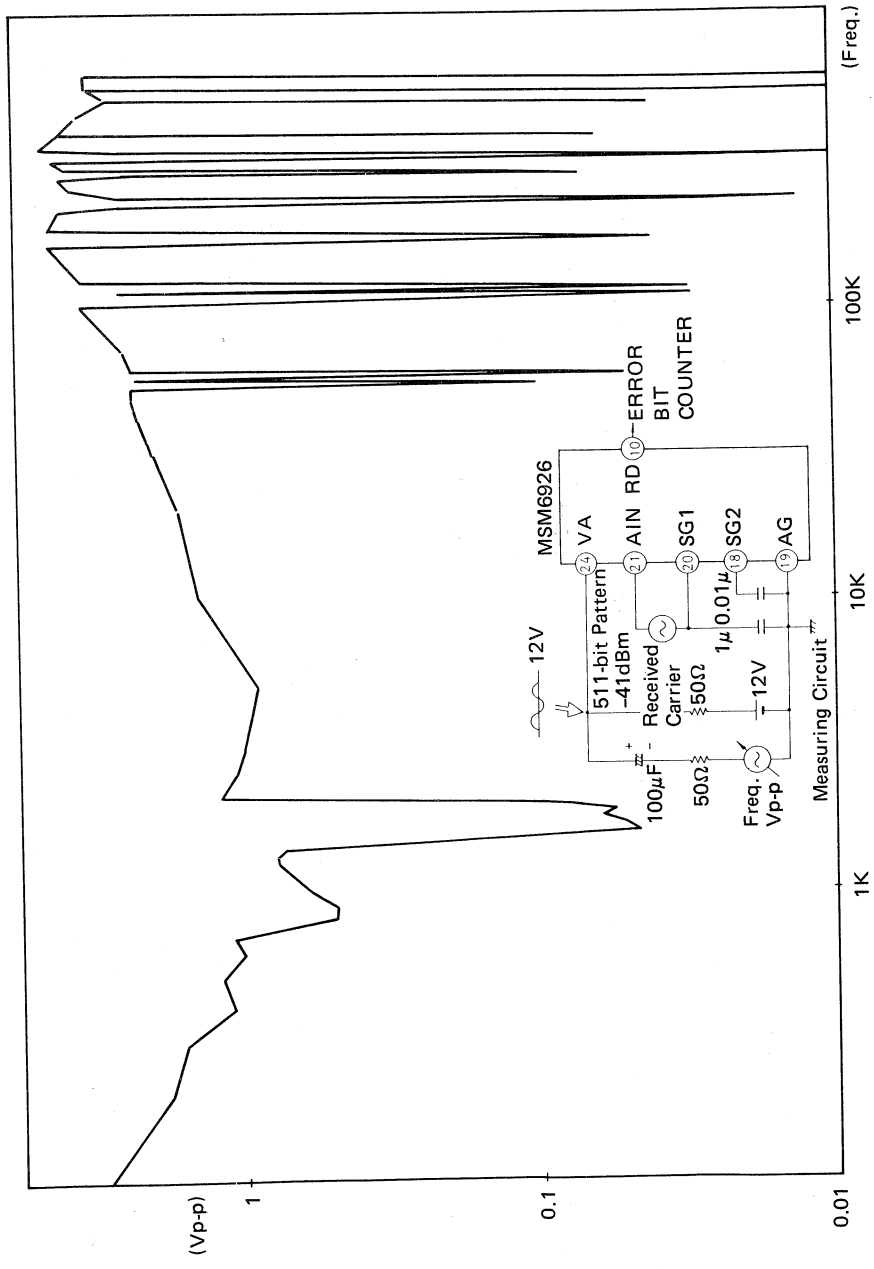


Figure 3-25 Frequency Characteristics of Power Supply Noise Level Responsible for Erroneous Operations

IV

11) Tone dialer connection circuit

Connect the tone dialer MK5089 (Mostek), MSM6234 (OKI), etc. as illustrated in Figure 3-26.

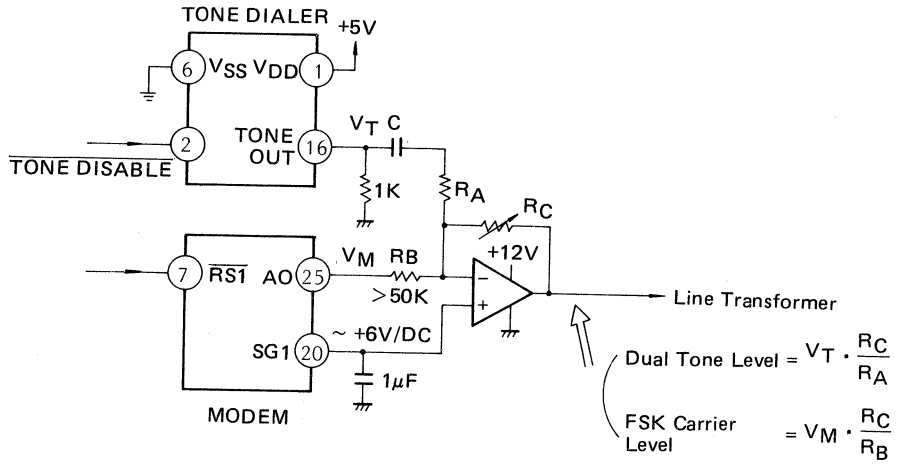


Figure 3-26 Tone Dialer Connection Circuit

The operational amplifier operates with SG1 potential (approx. +6V) as a signal ground, therefore requires an AC coupling. If our-of-voice band noise in the tone dialer output is so serious as to require its elimination, a circuit as illustrated in Figure 3-27 works effectively.

C_T must be selected to obtain a proper time constant.

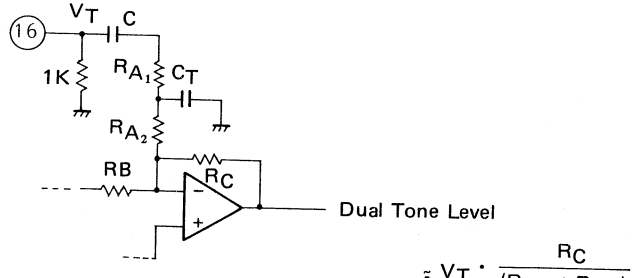


Figure 3-27 Circuit for Eliminating Noise Outside of Dual Tone Band

IV

12) Considerations for duplexer (Line Hybrid Circuit)

In case of full-duplex systems, a duplexer plays a important role. Its purpose is to help reject transmit signal energy from the receive signal.

Theoretically, a duplexer can be adjusted to achieve infinite rejection (no existence of cross-talk) — where the phase and amplitude of the inverting and non-inverting signals cancel through the duplexer OP-Amps. In practice, however, telephone line impedances vary enough such that only about 10 ~ 15 dB of rejection can be expected. To attain this rejection, it is recommended that the duplexer components (R_1, R_2, R_3 and C_1 in Figure 3-28) be tuned for the impedance and loss characteristics of the particular type of transformer being used. This will minimize the impedance variation of the line.

Once these component values have been determined for a particular transformer type, further trimming is usally unnecessary on a board-to-board basis. A recommended procedure for balancing the duplexer which was used in finding the values in Figure 3-28, is as follows.

a) A recommended procedure for balancing the duplexer

① First, put the $\overline{RS1}$ input to VD (transmit squech). Next, connect a 600 ohm signal source to points A and B (in case of MSM6926, 0 dBm and 980 Hz.) Tune R_1 until the loss at point A and B is exactly 6 dB. This allows maximum power transfer through the transformer.

② With R_1 at this new value, replace the signal source with a 600 ohm resistor at point A and B. Now output the transmit signal from A_0 (V_0) via OPA1 at the same frequency.

③ Now tune R_3 until the signal out of A_0 reaches a minimum at OPA2 output terminal (V_2). Then tune C_1 until a new, lower minimum is reached which should be around 30 dB.

The phase and amplitude of the two signal components have now been matched for the best rejection over the spread of telephone lines.

A crosstalk characteristic of the duplexer adjusted in steps ① through ③ is shown in Figure 3-29. It was obtained by measuring the V_0-to-V_2 transfer characteristic with the modem chip and the duplexer disconnected from each other.

The duplexer has the attenuation pole at about 1420 Hz when a line impedance is ideal 600 ohm.

b) Characteristics on a practical line

Figure 3-29 also shows the practical characteristics of the duplexer connected to existing telephone lines.

These are represented by V_0-to-V_2 transfer characteristics; it should be noticed that the receive signal level at AIN terminal (V_3) will be lower than V_2 by about 6 dB typically because of the existence of R_6 and R_7.

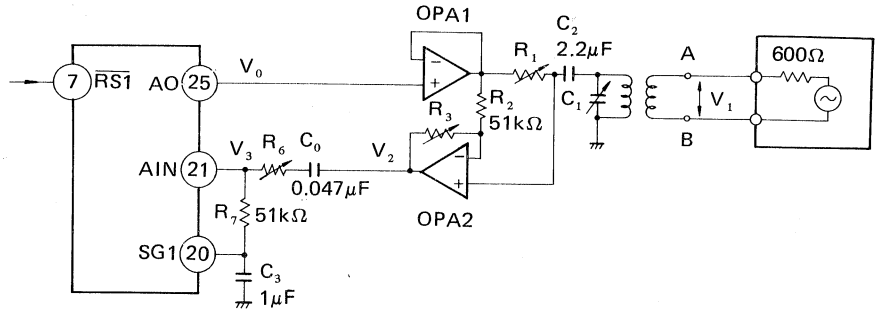
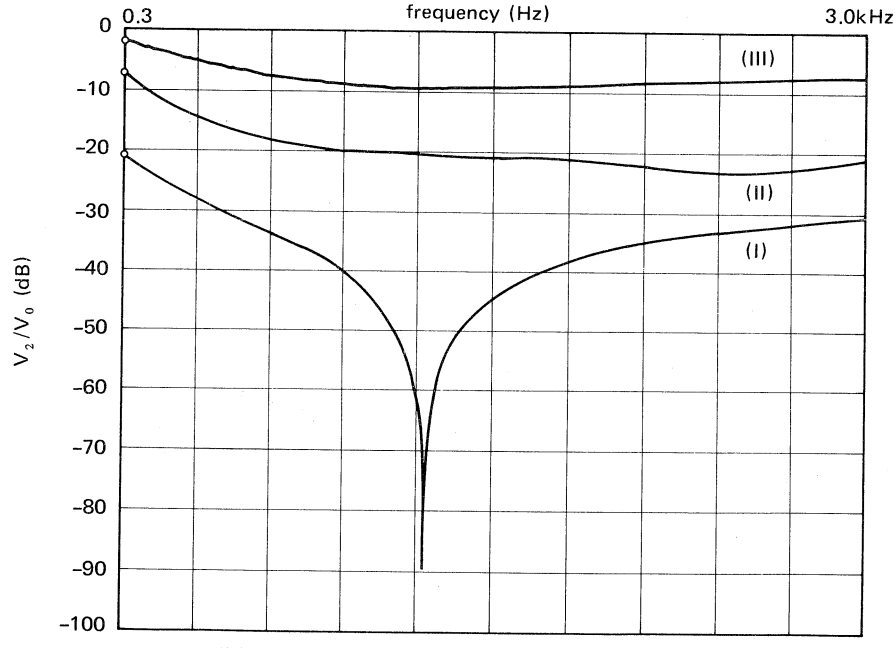


Figure 3-28 Deplexer (Line Hybrid Circuit) Considerations



(I) Terminal by 600Ω pure resistor

(II) Connected to a private phone line

(III) Connected to a public switched network

Figure 3-29 Experimental Cross-Talk Characteristics

IV

c) Allowable crosstalk level

We investigated how the receiver characteristics would be affected by crosstalk. The measuring circuit used is shown in Figure 3-30, and the characteristics obtained are shown in Figures 3-31 and 32. For example, if MSM6946 (Bell 103) is to operate in originate mode (M = 1) with a bit error rate (BER) of 10^{-4} or less for a receive signal level of -43 dBm or greater, these figures argue that the crosstalk level should be held down below -3 dBm.

Next, it should be noticed that not only the AC signal crosstalk, but also the DC voltage on AIN terminal deteriorate the performance, because the DC voltage makes the receiver's dynamic range to be narrow.

This is the reason for which capacitor C_0 shown in Figure 3-28 is necessary. Capacitor C_0 prevents the DC offset voltage on A_0 from being conveyed to AIN terminal.

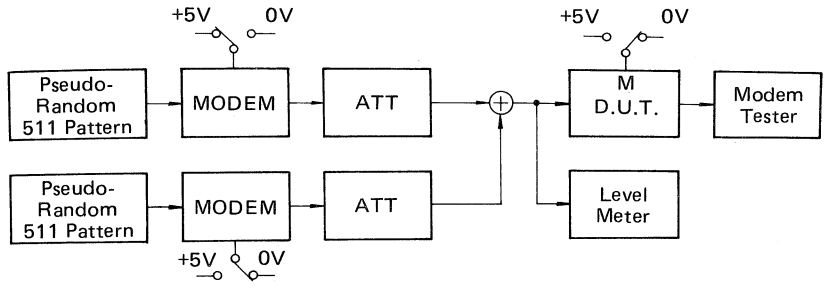


Figure 3-30 Test Set Examining the Influence of Cross-Talk

IV

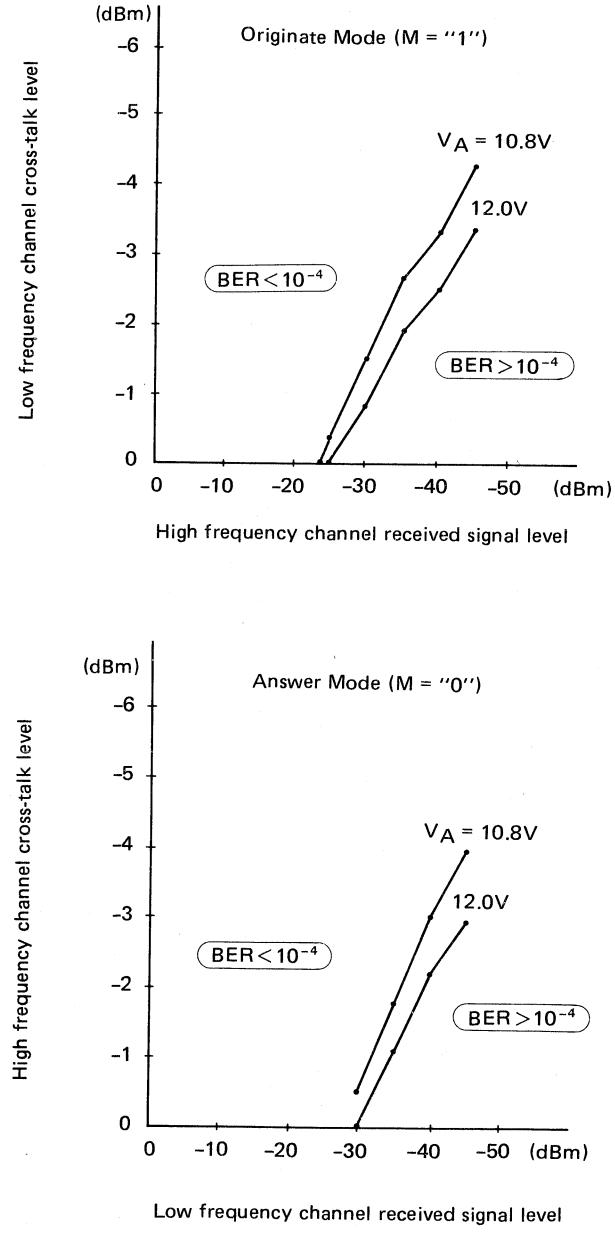
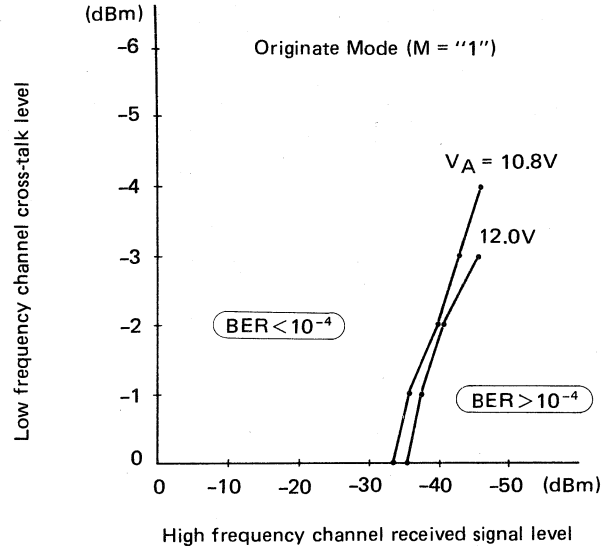


Figure 3-31 Deterioration of Bit Error Rate by Cross-Talk (MSM6926)



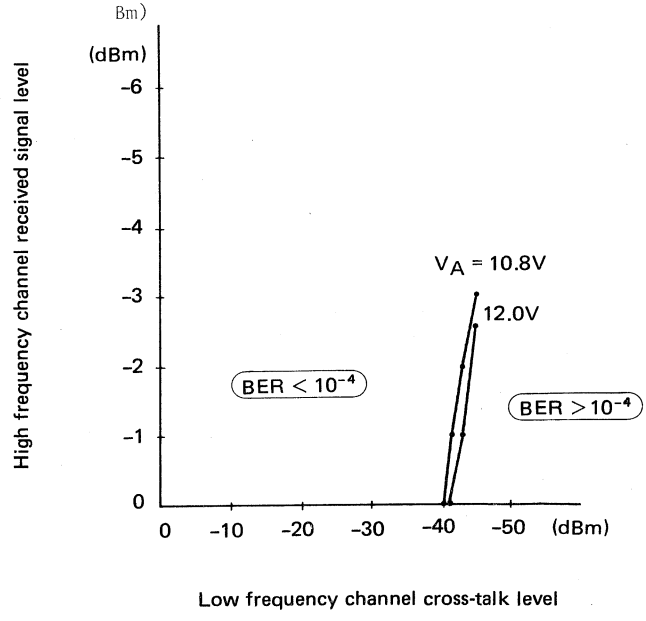


Figure 3-32 Deterioration of Bit Error Rate by Cross-Talk (MSM6946)

IV

d) Consideration

① With reference to the circuit shown in Figure 3-28, if no transformer loss is present, the receive signal will be amplified twice (+6 dB) at the output of OPA2. Accordingly, it is reduced to a half (-6 dB) through R_6 and R_7 before input to AIN terminal. Assuming that the V_0-to-V_2 transfer ratio is -8 dB (See Figure 3-29), the crosstalk level at AIN terminal is calculated as follows, because V_0 is +6 dBm.

$$+6\ \text{dBm}^{*1} - 8\ \text{dB}^{*2} - 6\ \text{dB}^{*3} = -8\ \text{dBm}^{*4}$$

*1: transmit level at A_0 terminal, V_0

*2: V_0-to-V_2 transfer ratio

*3: attenuation by R_6 and R_7

*4: crosstalk signal level at AIN terminal

According to Figure 3-32, it can be seen that the cross-talk of -8 dBm is not a problem for the system performance.

② In case a series resistance or other detrimental impedance in the telephone line causes a signal transmission loss through the transformer, the performance will be degraded as compared with the case discussed in ① above.

For example, if a both-way transmission loss is 4 dB and V_0-to-V_2 transfer ratio remains to be -8 dB, the crosstalk level at AIN terminal is calculated as follows.

$$(+6\ \text{dBm} + 4\ \text{dB}^{*1}) - 8\ \text{dB} - 6\ \text{dB} + 4\ \text{dB}^{*2} = 0\ \text{dBm}$$

*1: compensation for loss through transformer in the transmit direction (an additional gain of 4 dB to be given to OPA1)

*2: compensation for loss through transformer in the receive direction (loss through the R_6-R_7 attenuator to be reduced by 4 dB)

When MSM6946 (Bell 103) is operated in the high-frequency channel receiving mode (M = 1), Figure 3-32 tells that if the crosstalk level is 0 dBm, the bit error rate will run in excess of 10^{-4} unless the receive signal level is greater than -33 dBm.

③ The greater the ratio of the transmit signal level to the maximum receive signal level is, the more will be aggravated the degradation of the system performance due to crosstalk.

4. CHECK POINTS FOR TROUBLE SHOOTINGS

1) Basic Examinations

- V pin 15, V pin 19 = 0 volt
- V pin 24 = +12 V ±10%
- Are there any noise on pin 24? If the noise is not negligible, modem performances are easy to be deteriorated.
- V pin 26 = +5 V ±5%
- V pin 20 = 1/2 · (V pin 24)
  The load resistance connected to pin 20 must be more than 50 Kohms and any other voltage potentials must not input to this pin.
- V pin 18 = V pin 20 + 0.7
- V pin 16 = V pin 18 + 3.0
- VDC (pin 21) = V pin 20
- Any external components should not be connected to pin 1 and pin 2 except a 3.58 MHz crystal resonator.
- Pin 3 outputs a pulse train of which frequency is about 874 Hz.
- Pin 13 should be connected to pin 14.
- Pin 23 should be connected to digital "0" level.
- The analog transmit signal on pin 25 swings keeping its DC potential at about half of VA (pin 24).
  The load resistance connected to pin 25 must be more than 50 Kohms.
- The fun-out number of digital output pins are less than two.

NOTE) Checks should be performed with direct touching to pins.

2) Checks for Signal Transmiting

2-1. Common checks

- Pin 4 and Pin 7 should be connected to digital "0" level.
- Pin 6 outputs digital "0" level.
- Transmit data is input to the chip through pin 9 (XD).

2-2. MSM6926 and MSM6946

- Operating mode is determined using pin 22-originate or answer mode.
- Pin 27 and Pin 28 should be connected to digital "0" level.

2-3. MSM6927

- Pin 27 and Pin 28 should be connected to digital "0" level.

2-4. MSM6947

- Pin 27 should be connected to digital "0" level.
- Pin 28 should be connected to digital "1" level.

Signal transmiting ought to be performed after checks shown above if the chip is not out of order.

3) Checks for Signal Receiving

3-1. Common checks

- Pin 4 and Pin 27 should be connected to digital "0" level.
- The receive signal level should be within -6 and -43 dBm at the point of Pin 21 (AIN).
- Pin 11 and Pin 12 output the digital "0" state during the chip operates as a receiver.
- Pin 10, Pin 13 and Pin 14 show the same digital output data.

3-2. MSM6926 and MSM6946

- Confirm the carrier frequencies transmited through Pin 25 according to the operating modes.

3-3. MSM6927 and MSM6947

- Pin 7 should be connected to digital "1" level.
- Pin 22 should be connected to digital "0" level.
- Pin 22 ($\overline{SQ}$) is connected to digital "1" level when the operation on 4-wire facilities or the self test is required.

Signal receiving ought to be performed after checks shown above if the chip is not out of order.

Note : Product data and specification information herein are subject to change without advance notice for the sake of technical improvements in performance and reliability since OKI is permanently endeavoring to supply the best products possible. The manufacturer does not assume responsibility for customer product designs and for the fitness to any particular application, nor for patent rights or other rights of third parties and infringements thereof resulting from the use of his products. This publication does not commit immediate availability of the products(s) described by it. If in doubt, please contact your nearest OKI representative. The information furnished by OKI is believed to be accurate and reliable. However, no responsibility is assumed for inaccuracies that may not have been detected prior to printing, and for those which occur beyond our contral. This issue substitutes and supersedes all publications previously supplied by OKI for the captioned product(s). This document may not, in whole or part, be copied, photocopied, reproduced, translated, or converted to any machine readable form, without prior written consent from OKI.

OKI Electric Europe GmbH

Niederkasseler Lohweg 8, D-4000 Düsseldorf 11, Fed. Rep. of Germany
□ Tel : 0211-59550 □ Fax : 0211-591669 □ Telex : 858-4312

FOR FURTHER INFORMATION PLEASE CONTACT :

OKI ELectric Industry Co., Ltd,
Head Office Annex
10-3, Shibaura, 4-chome,
Minato-ku, Tokyo 108, Japan
Tel : 3-454-2111
Fax : 3-798-7643
Telex : J22627
Electronic Devices Group
Overseas Marketing Dept.

OKI Semiconductor
650 North Mary Avenue,
Sunnyvale, CA #94086, U.S.A.
Tel : (408) 720-1900
Fax : (408) 720-1918
Telex : 296687 OKI SNTA

OKI Electric Europe GmbH
Niederkasseler Lohweg 8,
D-4000 Düsseldorf 11,
Fed. Rep. of Germany
Tel : 0211-59550
Fax : 0211-591669
Telex : 858-4312

OKI Electronics (Hong Kong) Ltd.
16th Floor, Fairmont House,
8 Cotton Tree Drive, Hong Kong
Tel : 5-263111
Fax : 5-200102
Telex : 62459 OKIHK HX

OKI

OKI SINCE 1881

Printed in West Germany

REF NO : TOM02-1A106